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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 320K Logic Elements |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FBGA, FC (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as032e3f29e2lg |



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Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

| Market | Applications |
|-----------------------|---|
| Wireless | <ul style="list-style-type: none"> • Channel and switch cards in remote radio heads • Mobile backhaul |
| Wireline | <ul style="list-style-type: none"> • 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation |
| Broadcast | <ul style="list-style-type: none"> • Studio switches • Servers and transport • Videoconferencing • Professional audio and video |
| Computing and Storage | <ul style="list-style-type: none"> • Flash cache • Cloud computing servers • Server acceleration |
| Medical | <ul style="list-style-type: none"> • Diagnostic scanners • Diagnostic imaging |
| Military | <ul style="list-style-type: none"> • Missile guidance and control • Radar • Electronic warfare • Secure communications |

Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



| Feature | Description | |
|-----------------------------------|--|---|
| Embedded Hard IP blocks | Variable-precision DSP | <ul style="list-style-type: none">Native support for signal processing precision levels from 18 x 19 to 54 x 54Native support for 27 x 27 multiplier mode64-bit accumulator and cascade for systolic finite impulse responses (FIRs)Internal coefficient memory banksPadder/subtractor for improved efficiencyAdditional pipeline register to increase performance and reduce powerSupports floating point arithmetic:<ul style="list-style-type: none">Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.Dynamic accumulator reset control.Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks. |
| | Memory controller | DDR4, DDR3, and DDR3L |
| | PCI Express* | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port |
| | Transceiver I/O | <ul style="list-style-type: none">10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)PCS hard IPs that support:<ul style="list-style-type: none">10-Gbps Ethernet (10GbE)PCIe PIPE interfaceInterlakenGbps Ethernet (GbE)Common Public Radio Interface (CPRI) with deterministic latency supportGigabit-capable passive optical network (GPON) with fast lock-time support13.5G JESD204b8B/10B, 64B/66B, 64B/67B encoders and decodersCustom mode support for proprietary protocols |
| Core clock networks | <ul style="list-style-type: none">Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none">667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface800 MHz LVDS interface clocking with 1,600 Mbps LVDS interfaceGlobal, regional, and peripheral clock networksClock networks that are not used can be gated to reduce dynamic power | |
| Phase-locked loops (PLLs) | <ul style="list-style-type: none">High-resolution fractional synthesis PLLs:<ul style="list-style-type: none">Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)Support integer mode and fractional modeFractional mode support with third-order delta-sigma modulationInteger PLLs:<ul style="list-style-type: none">Adjacent to general purpose I/OsSupport external memory and LVDS interfaces | |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none">1.6 Gbps LVDS—every pair can be configured as receiver or transmitterOn-chip termination (OCT)1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing | |
| External Memory Interface | <ul style="list-style-type: none">Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none">DDR4—speeds up to 1,200 MHz/2,400 MbpsDDR3—speeds up to 1,067 MHz/2,133 MbpsSoft memory controller—provides support for RLDRAM 3⁽²⁾, QDR IV⁽²⁾, and QDR II+ | |
| continued... | | |



| Feature | Description | |
|---|---|--|
| Low-power serial transceivers | <ul style="list-style-type: none">• Continuous operating range:<ul style="list-style-type: none">— Intel Arria 10 GX—1 Gbps to 17.4 Gbps— Intel Arria 10 GT—1 Gbps to 25.8 Gbps• Backplane support:<ul style="list-style-type: none">— Intel Arria 10 GX—up to 12.5— Intel Arria 10 GT—up to 12.5• Extended range down to 125 Mbps with oversampling• ATX transmit PLLs with user-configurable fractional synthesis capability• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module• Adaptive linear and decision feedback equalization• Transmitter pre-emphasis and de-emphasis• Dynamic partial reconfiguration of individual transceiver channels | |
| HPS (Intel Arria 10 SX devices only) | Processor and system | <ul style="list-style-type: none">• Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability• 256 KB on-chip RAM and 64 KB on-chip ROM• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers• Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)• ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage |
| | External interfaces | <ul style="list-style-type: none">• Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller• Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I²C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os) |
| | Interconnects to core | <ul style="list-style-type: none">• High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write• HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa• Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port• FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller |
| Configuration | <ul style="list-style-type: none">• Tamper protection—comprehensive design protection to protect your valuable IP investments• Enhanced 256-bit advanced encryption standard (AES) design security with authentication• Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3 | |
| continued... | | |

⁽²⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|------------------------------|----------------------|--------------|-----------|-----------|-----------|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO ⁽³⁾ | | 696 | 696 | 768 | 768 |
| LVDS Pair ⁽⁴⁾ | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

Package Plan

Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|--------------|---|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|-------------|------|--|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

Available Options

Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Maximum Resources

Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

| Resource | | Product Line | | | | | | |
|--------------------------------|----------------------|--------------|---------|---------|---------|---------|---------|-----------|
| | | SX 160 | SX 220 | SX 270 | SX 320 | SX 480 | SX 570 | SX 660 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 | 570 | 660 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 | 217,080 | 251,680 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 | 36,000 | 42,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 | 5,096 | 5,788 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 | 1,523 | 1,687 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 | 3,046 | 3,374 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| | I/O | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 | 48 | 48 |
| GPIO ⁽⁸⁾ | | 288 | 288 | 384 | 384 | 492 | 696 | 696 |
| LVDS Pair ⁽⁹⁾ | | 120 | 120 | 168 | 168 | 174 | 324 | 324 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| ARM Cortex-A9 MPCore Processor | | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

Package Plan

Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|--------------|--|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 160 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 220 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| SX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| continued... | | | | | | | | | | | | |

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ Each LVDS I/O pair can be used as differential input or output.



I/O Vertical Migration for Intel Arria 10 Devices

Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

| Variant | Product Line | Package | | | | | | | | | | |
|---------------------|--------------|---------|-----|-----|-----|-----|------|------|------|------|------|------|
| | | U19 | F27 | F29 | F34 | F35 | KF40 | NF40 | RF40 | NF45 | SF45 | UF45 |
| Intel® Arria® 10 GX | GX 160 | ↑ | ↑ | ↑ | | | | | | | | |
| | GX 220 | ↓ | ↓ | ↓ | | | | | | | | |
| | GX 270 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | GX 320 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | GX 480 | | | ↓ | ↑ | ↑ | | | | | | |
| | GX 570 | | | | ↑ | ↑ | ↑ | ↑ | | | | |
| | GX 660 | | | | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GX 900 | | | | ↑ | | | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GX 1150 | | | | ↑ | | | ↑ | ↑ | ↑ | ↑ | ↑ |
| | GT 900 | | | | | | | | | | ↑ | ↑ |
| | GT 1150 | | | | | | | | | | ↑ | ↑ |
| Intel Arria 10 SX | SX 160 | ↑ | ↑ | ↑ | | | | | | | | |
| | SX 220 | ↓ | ↓ | ↓ | | | | | | | | |
| | SX 270 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | SX 320 | | ↓ | ↓ | ↑ | ↑ | | | | | | |
| | SX 480 | | | ↓ | ↑ | ↑ | | | | | | |
| | SX 570 | | | | ↑ | ↑ | ↑ | ↑ | | | | |
| | SX 660 | | | | ↑ | ↑ | ↑ | ↑ | | | | |
| | | | | | | | | | | | | |

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
| | | | 18 x 19 Multiplier | 27 x 27 Multiplier | | |
| | SX 320 | 984 | 1,968 | 984 | 984 | 984 |
| | SX 480 | 1,368 | 2,736 | 1,368 | 1,368 | 1,368 |
| | SX 570 | 1,523 | 3,046 | 1,523 | 1,523 | 1,523 |
| | SX 660 | 1,687 | 3,374 | 1,687 | 1,687 | 1,687 |

Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160 | 156 | 156 | 156 | 156 | 140 |
| | GX 220 | 192 | 192 | 192 | 192 | 173 |
| | GX 270 | 830 | 830 | 830 | 830 | 747 |
| | GX 320 | 984 | 984 | 984 | 984 | 886 |
| | GX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | GX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | GX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |
| | GX 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GX 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 GT | GT 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GT 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 SX | SX 160 | 156 | 156 | 156 | 156 | 140 |
| | SX 220 | 192 | 192 | 192 | 192 | 173 |
| | SX 270 | 830 | 830 | 830 | 830 | 747 |
| | SX 320 | 984 | 984 | 984 | 984 | 886 |
| | SX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | SX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | SX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB | 32 | x16, x18, or x20 |
| | 64 ⁽¹⁰⁾ | x8, x9, x10 |
| M20K | 512 | x40, x32 |
| | 1K | x20, x16 |
| | 2K | x10, x8 |
| | 4K | x5, x4 |
| | 8K | x2 |
| | 16K | x1 |

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.

- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Related Information

[External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|-----------------|--------------|-----------------------|-------------------------|
| DDR4 SDRAM | Quarter rate | Yes | 1,067 |
| | | — | 1,200 |
| DDR3 SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 1,067 |
| | | — | 1,067 |
| DDR3L SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 933 |
| | | — | 933 |
| LPDDR3 SDRAM | Half rate | — | 533 |
| | Quarter rate | — | 800 |

Table 21. Memory Standards Supported by the Soft Memory Controller

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|-----------------------------|--------------|-------------------------|
| RLDRAM 3 ⁽¹¹⁾ | Quarter rate | 1,200 |
| QDR IV SRAM ⁽¹¹⁾ | Quarter rate | 1,067 |
| QDR II SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ Xtreme SRAM | Full rate | 333 |
| | Half rate | 633 |

Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|-----------------|--------------|-------------------------|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,067 |
| DDR3L SDRAM | Half rate | 933 |

⁽¹¹⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Related Information

[Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

Related Information

[PCS Features](#) on page 30

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

Related Information

[PCS Features](#) on page 30

10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

[PCS Features](#) on page 30

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

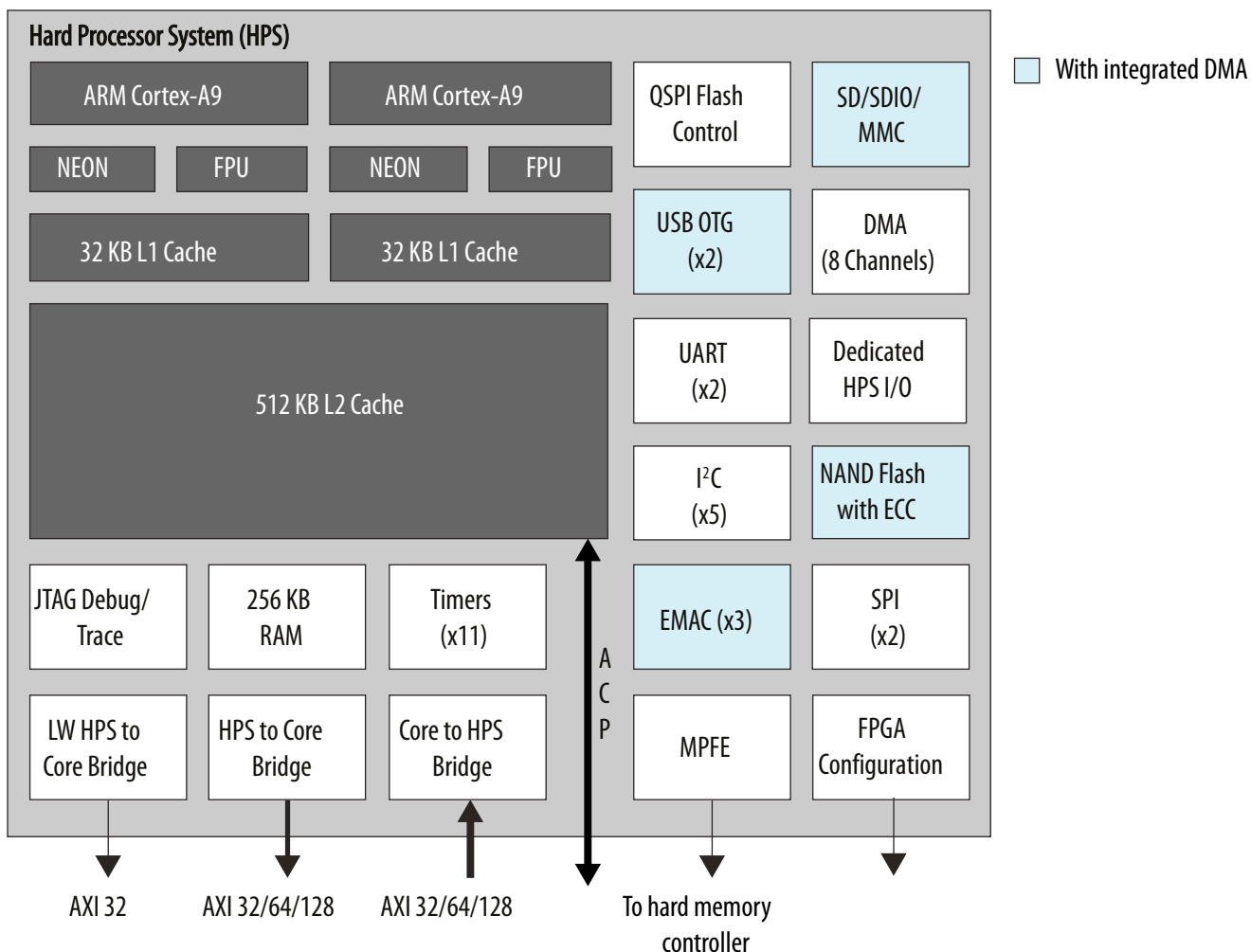
The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed



Figure 9. HPS Block Diagram

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) ⁽¹³⁾ | Decompression | Design Security ⁽¹⁴⁾ | Partial Reconfiguration ⁽¹⁵⁾ | Remote System Update |
|--|----------------------|----------------------|--------------------------------------|---------------|---------------------------------|---|----------------------|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes ⁽¹⁶⁾ | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁷⁾ Supported at a maximum clock rate of 100 MHz.



| Date | Version | Changes |
|----------------|------------|--|
| | | <ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | <ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | <ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel. |
| October 2016 | 2016.10.31 | <ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | <ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | <ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section. |

continued...