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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 320K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA, FC (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10as032e3f29i2lg



Feature	Description	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none">Native support for signal processing precision levels from 18 x 19 to 54 x 54Native support for 27 x 27 multiplier mode64-bit accumulator and cascade for systolic finite impulse responses (FIRs)Internal coefficient memory banksPreadder/subtractor for improved efficiencyAdditional pipeline register to increase performance and reduce powerSupports floating point arithmetic:<ul style="list-style-type: none">Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.Dynamic accumulator reset control.Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.
	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express*	PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port
	Transceiver I/O	<ul style="list-style-type: none">10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)PCS hard IPs that support:<ul style="list-style-type: none">10-Gbps Ethernet (10GbE)PCIe PIPE interfaceInterlakenGbps Ethernet (GbE)Common Public Radio Interface (CPRI) with deterministic latency supportGigabit-capable passive optical network (GPON) with fast lock-time support13.5G JESD204b8B/10B, 64B/66B, 64B/67B encoders and decodersCustom mode support for proprietary protocols
Core clock networks	<ul style="list-style-type: none">Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none">667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface800 MHz LVDS interface clocking with 1,600 Mbps LVDS interfaceGlobal, regional, and peripheral clock networksClock networks that are not used can be gated to reduce dynamic power	
Phase-locked loops (PLLs)	<ul style="list-style-type: none">High-resolution fractional synthesis PLLs:<ul style="list-style-type: none">Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)Support integer mode and fractional modeFractional mode support with third-order delta-sigma modulationInteger PLLs:<ul style="list-style-type: none">Adjacent to general purpose I/OsSupport external memory and LVDS interfaces	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none">1.6 Gbps LVDS—every pair can be configured as receiver or transmitterOn-chip termination (OCT)1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing	
External Memory Interface	<ul style="list-style-type: none">Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none">DDR4—speeds up to 1,200 MHz/2,400 MbpsDDR3—speeds up to 1,067 MHz/2,133 MbpsSoft memory controller—provides support for RLDRAM 3⁽²⁾, QDR IV⁽²⁾, and QDR II+	
continued...		



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none">Continuous operating range:<ul style="list-style-type: none">Intel Arria 10 GX—1 Gbps to 17.4 GbpsIntel Arria 10 GT—1 Gbps to 25.8 GbpsBackplane support:<ul style="list-style-type: none">Intel Arria 10 GX—up to 12.5Intel Arria 10 GT—up to 12.5Extended range down to 125 Mbps with oversamplingATX transmit PLLs with user-configurable fractional synthesis capabilityElectronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical moduleAdaptive linear and decision feedback equalizationTransmitter pre-emphasis and de-emphasisDynamic partial reconfiguration of individual transceiver channels	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none">Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability256 KB on-chip RAM and 64 KB on-chip ROMSystem peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managersSecurity features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage
	External interfaces	<ul style="list-style-type: none">Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controllerCommunication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I²C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)
	Interconnects to core	<ul style="list-style-type: none">High-performance ARM AMBA* AXI bus bridges that support simultaneous read and writeHPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versaConfiguration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration portFPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller
Configuration	<ul style="list-style-type: none">Tamper protection—comprehensive design protection to protect your valuable IP investmentsEnhanced 256-bit advanced encryption standard (AES) design security with authenticationConfiguration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3	
continued...		

⁽²⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

Resource		Product Line			
		GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		570	660	900	1,150
ALM		217,080	251,680	339,620	427,200
Register		868,320	1,006,720	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precision DSP Block		1,523	1,687	1,518	1,518
18 x 19 Multiplier		3,046	3,374	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	16	16	16
17.4 Gbps Transceiver		48	48	96	96
GPIO ⁽³⁾		696	696	768	768
LVDS Pair ⁽⁴⁾		324	324	384	384
PCIe Hard IP Block		2	2	4	4
Hard Memory Controller		16	16	16	16

Package Plan

Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 160	48	192	6	48	192	12	48	240	12
GX 220	48	192	6	48	192	12	48	240	12
GX 270	—	—	—	48	192	12	48	312	12
GX 320	—	—	—	48	192	12	48	312	12
GX 480	—	—	—	—	—	—	48	312	12



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

Available Options

Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Maximum Resources

Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687
18 x 19 Multiplier		312	384	1,660	1,970	2,736	3,046	3,374
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO ⁽⁸⁾		288	288	384	384	492	696	696
LVDS Pair ⁽⁹⁾		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

Package Plan

Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
continued...												

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ Each LVDS I/O pair can be used as differential input or output.



I/O Vertical Migration for Intel Arria 10 Devices

Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160	↑	↑	↑								
	GX 220	↓	↓	↓								
	GX 270		↓	↓	↑	↑						
	GX 320		↓	↓	↑	↑						
	GX 480			↓	↑	↑						
	GX 570				↑	↑	↑	↑				
	GX 660				↑	↑	↑	↑	↑	↑	↑	↑
	GX 900				↑			↑	↑	↑	↑	↑
	GX 1150				↑			↑	↑	↑	↑	↑
	GT 900										↑	↑
	GT 1150										↑	↑
Intel Arria 10 SX	SX 160	↑	↑	↑								
	SX 220	↓	↓	↓								
	SX 270		↓	↓	↑	↑						
	SX 320		↓	↓	↑	↑						
	SX 480			↓	↑	↑						
	SX 570				↑	↑	↑	↑				
	SX 660				↑	↑	↑	↑				

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
Intel Arria 10 GX	GX 160	156	312	156	156	156
	GX 220	192	384	192	192	192
	GX 270	830	1,660	830	830	830
	GX 320	984	1,968	984	984	984
	GX 480	1,368	2,736	1,368	1,368	1,368
	GX 570	1,523	3,046	1,523	1,523	1,523
	GX 660	1,687	3,374	1,687	1,687	1,687
	GX 900	1,518	3,036	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 GT	GT 900	1,518	3,036	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 SX	SX 160	156	312	156	156	156
	SX 220	192	384	192	192	192
	SX 270	830	1,660	830	830	830

continued...



Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
	SX 320	984	1,968	984	984	984
	SX 480	1,368	2,736	1,368	1,368	1,368
	SX 570	1,523	3,046	1,523	1,523	1,523
	SX 660	1,687	3,374	1,687	1,687	1,687

Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single-Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating-Point Operations per Second (GFLOPs)
Intel Arria 10 GX	GX 160	156	156	156	156	140
	GX 220	192	192	192	192	173
	GX 270	830	830	830	830	747
	GX 320	984	984	984	984	886
	GX 480	1,369	1,368	1,368	1,368	1,231
	GX 570	1,523	1,523	1,523	1,523	1,371
	GX 660	1,687	1,687	1,687	1,687	1,518
	GX 900	1,518	1,518	1,518	1,518	1,366
	GX 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 GT	GT 900	1,518	1,518	1,518	1,518	1,366
	GT 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 SX	SX 160	156	156	156	156	140
	SX 220	192	192	192	192	173
	SX 270	830	830	830	830	747
	SX 320	984	984	984	984	886
	SX 480	1,369	1,368	1,368	1,368	1,231
	SX 570	1,523	1,523	1,523	1,523	1,371
	SX 660	1,687	1,687	1,687	1,687	1,518

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Intel Arria 10 Devices

Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Intel Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	587	11,740	2,703	1,690	13,430
	GX 270	750	15,000	3,922	2,452	17,452
	GX 320	891	17,820	4,363	2,727	20,547
	GX 480	1,431	28,620	6,662	4,164	32,784
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,131	42,620	9,260	5,788	48,408
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	587	11,740	2,703	1,690	13,430
	SX 270	750	15,000	3,922	2,452	17,452
	SX 320	891	17,820	4,363	2,727	20,547
	SX 480	1,431	28,620	6,662	4,164	32,784
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,131	42,620	9,260	5,788	48,408

- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Related Information

[External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.



Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices

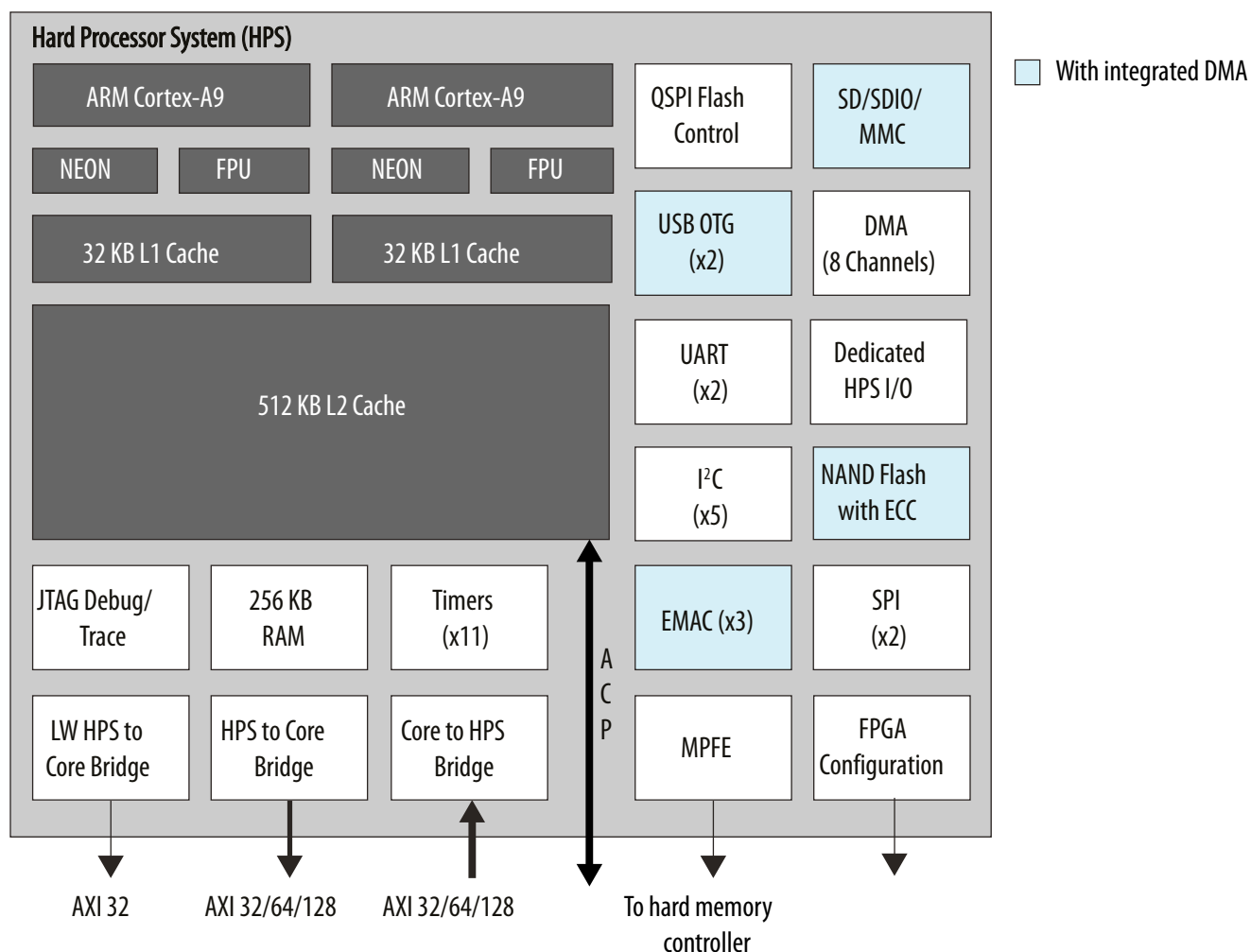
Feature	Capability
Chip-to-Chip Data Rates	1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices) 1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 12.5 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

Figure 9. HPS Block Diagram

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none">• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I ² C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History for Intel Arria 10 Device Overview

Document Version	Changes
2018.04.09	Updated the lowest V_{CC} from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	<ul style="list-style-type: none">• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.• Updated transceiver backplane capability to 12.5 Gbps.• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.
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Date	Version	Changes
		<ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks.
March 2017	2017.03.15	<ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel.
October 2016	2016.10.31	<ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.
May 2016	2016.05.02	<ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.
February 2016	2016.02.11	<ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section.
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