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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

Details

| | |
|-------------------------|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I ² C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 320K Logic Elements |
| Operating Temperature | 0°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as032h2f34e1hg |



Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

| Market | Applications |
|-----------------------|---|
| Wireless | <ul style="list-style-type: none"> • Channel and switch cards in remote radio heads • Mobile backhaul |
| Wireline | <ul style="list-style-type: none"> • 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation |
| Broadcast | <ul style="list-style-type: none"> • Studio switches • Servers and transport • Videoconferencing • Professional audio and video |
| Computing and Storage | <ul style="list-style-type: none"> • Flash cache • Cloud computing servers • Server acceleration |
| Medical | <ul style="list-style-type: none"> • Diagnostic scanners • Diagnostic imaging |
| Military | <ul style="list-style-type: none"> • Missile guidance and control • Radar • Electronic warfare • Secure communications |

Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



| Feature | Description | |
|-----------------------------------|--|---|
| Embedded Hard IP blocks | Variable-precision DSP | <ul style="list-style-type: none">Native support for signal processing precision levels from 18 x 19 to 54 x 54Native support for 27 x 27 multiplier mode64-bit accumulator and cascade for systolic finite impulse responses (FIRs)Internal coefficient memory banksPreadder/subtractor for improved efficiencyAdditional pipeline register to increase performance and reduce powerSupports floating point arithmetic:<ul style="list-style-type: none">Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.Dynamic accumulator reset control.Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks. |
| | Memory controller | DDR4, DDR3, and DDR3L |
| | PCI Express* | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port |
| | Transceiver I/O | <ul style="list-style-type: none">10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)PCS hard IPs that support:<ul style="list-style-type: none">10-Gbps Ethernet (10GbE)PCIe PIPE interfaceInterlakenGbps Ethernet (GbE)Common Public Radio Interface (CPRI) with deterministic latency supportGigabit-capable passive optical network (GPON) with fast lock-time support13.5G JESD204b8B/10B, 64B/66B, 64B/67B encoders and decodersCustom mode support for proprietary protocols |
| Core clock networks | <ul style="list-style-type: none">Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none">667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface800 MHz LVDS interface clocking with 1,600 Mbps LVDS interfaceGlobal, regional, and peripheral clock networksClock networks that are not used can be gated to reduce dynamic power | |
| Phase-locked loops (PLLs) | <ul style="list-style-type: none">High-resolution fractional synthesis PLLs:<ul style="list-style-type: none">Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)Support integer mode and fractional modeFractional mode support with third-order delta-sigma modulationInteger PLLs:<ul style="list-style-type: none">Adjacent to general purpose I/OsSupport external memory and LVDS interfaces | |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none">1.6 Gbps LVDS—every pair can be configured as receiver or transmitterOn-chip termination (OCT)1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing | |
| External Memory Interface | <ul style="list-style-type: none">Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none">DDR4—speeds up to 1,200 MHz/2,400 MbpsDDR3—speeds up to 1,067 MHz/2,133 MbpsSoft memory controller—provides support for RLDRAM 3⁽²⁾, QDR IV⁽²⁾, and QDR II+ | |
| continued... | | |



| Feature | Description |
|--------------------|---|
| | <ul style="list-style-type: none">Dynamic reconfiguration of the transceivers and PLLsFine-grained partial reconfiguration of the core fabricActive Serial x4 Interface |
| Power management | <ul style="list-style-type: none">SmartVIDLow static power device optionsProgrammable Power TechnologyIntel Quartus Prime integrated power analysis |
| Software and tools | <ul style="list-style-type: none">Intel Quartus Prime design suiteTransceiver toolkitPlatform Designer system integration toolDSP Builder for Intel FPGAsOpenCL™ supportIntel SoC FPGA Embedded Design Suite (EDS) |

Related Information

[Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

Intel Arria 10 Device Variants and Packages

Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|-------------------|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring: <ul style="list-style-type: none">17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Maximum Resources

Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO ⁽³⁾ | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair ⁽⁴⁾ | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁴⁾ Each LVDS I/O pair can be used as differential input or output.



Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|------------------------------|----------------------|--------------|-----------|-----------|-----------|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO ⁽³⁾ | | 696 | 696 | 768 | 768 |
| LVDS Pair ⁽⁴⁾ | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

Package Plan

Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|--------------|---|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|-------------|------|--|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





Maximum Resources

Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

| Resource | | Product Line | |
|------------------------------|----------------------|-------------------|-------------------|
| | | GT 900 | GT 1150 |
| Logic Elements (LE) (K) | | 900 | 1,150 |
| ALM | | 339,620 | 427,200 |
| Register | | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 48,460 | 54,260 |
| | MLAB | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 32 | 32 |
| | I/O | 16 | 16 |
| Transceiver | 17.4 Gbps | 72 ⁽⁵⁾ | 72 ⁽⁵⁾ |
| | 25.8 Gbps | 6 | 6 |
| GPIO ⁽⁶⁾ | | 624 | 624 |
| LVDS Pair ⁽⁷⁾ | | 312 | 312 |
| PCIe Hard IP Block | | 4 | 4 |
| Hard Memory Controller | | 16 | 16 |

Related Information

Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

Package Plan

Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45 (45 mm x 45 mm, 1932-pin FBGA) | | |
|--------------|--|----------|------|
| | 3 V I/O | LVDS I/O | XCVR |
| GT 900 | — | 624 | 72 |
| GT 1150 | — | 624 | 72 |

⁽⁵⁾ If all 6 GT channels are in use, 12 of the GX channels are not usable.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁷⁾ Each LVDS I/O pair can be used as differential input or output.



| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 480 | — | — | — | — | — | — | 48 | 312 | 12 | 48 | 444 | 24 |
| SX 570 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |
| SX 660 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |

Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 270 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 320 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 480 | 48 | 348 | 36 | — | — | — | — | — | — |
| SX 570 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| SX 660 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
| | | | 18 x 19 Multiplier | 27 x 27 Multiplier | | |
| | SX 320 | 984 | 1,968 | 984 | 984 | 984 |
| | SX 480 | 1,368 | 2,736 | 1,368 | 1,368 | 1,368 |
| | SX 570 | 1,523 | 3,046 | 1,523 | 1,523 | 1,523 |
| | SX 660 | 1,687 | 3,374 | 1,687 | 1,687 | 1,687 |

Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160 | 156 | 156 | 156 | 156 | 140 |
| | GX 220 | 192 | 192 | 192 | 192 | 173 |
| | GX 270 | 830 | 830 | 830 | 830 | 747 |
| | GX 320 | 984 | 984 | 984 | 984 | 886 |
| | GX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | GX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | GX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |
| | GX 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GX 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 GT | GT 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GT 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 SX | SX 160 | 156 | 156 | 156 | 156 | 140 |
| | SX 220 | 192 | 192 | 192 | 192 | 173 |
| | SX 270 | 830 | 830 | 830 | 830 | 747 |
| | SX 320 | 984 | 984 | 984 | 984 | 886 |
| | SX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | SX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | SX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB | 32 | x16, x18, or x20 |
| | 64 ⁽¹⁰⁾ | x8, x9, x10 |
| M20K | 512 | x40, x32 |
| | 1K | x20, x16 |
| | 2K | x10, x8 |
| | 4K | x5, x4 |
| | 8K | x2 |
| | 16K | x1 |

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

[PCS Features](#) on page 30

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed

Figure 6. Intel Arria 10 Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|----------------------|-------------------------------|----------------|--------------|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143 ⁽¹²⁾ to 2.97 | Native PHY | Standard PCS |

Related Information

[Intel Arria 10 Transceiver PHY User Guide](#)

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

⁽¹²⁾ The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.



Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none">• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I ² C interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |



Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
 - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
 - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
 - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
 - 32 KB of L1 instruction cache, 32 KB of L1 data cache
 - Single- and double-precision floating-point unit and NEON media engine
 - CoreSight debug and trace technology
 - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I²C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
 - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
 - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

Enhanced Configuration and Configuration via Protocol

Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) ⁽¹³⁾ | Decompression | Design Security ⁽¹⁴⁾ | Partial Reconfiguration ⁽¹⁵⁾ | Remote System Update |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG | 1 bit | 33 | 33 | — | — | Yes ⁽¹⁶⁾ | — |
| Active Serial (AS) through the EPCQ-L configuration device | 1 bit, 4 bits | 100 | 400 | Yes | Yes | Yes ⁽¹⁶⁾ | Yes |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit | 100 | 100 | Yes | Yes | Yes ⁽¹⁶⁾ | Parallel Flash Loader (PFL) IP core |

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⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁶⁾ Partial configuration can be performed only when it is configured as internal host.



| Date | Version | Changes |
|----------------|------------|--|
| | | <ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | <ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | <ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel. |
| October 2016 | 2016.10.31 | <ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | <ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | <ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section. |
| continued... | | |



| Date | Version | Changes |
|----------------|------------|--|
| December 2015 | 2015.12.14 | <ul style="list-style-type: none"> Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb. Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | <ul style="list-style-type: none"> Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660. Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in Number of Multipliers in Intel Arria 10 Devices table. Updated the available options for Arria 10 GX, GT, and SX. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | <ul style="list-style-type: none"> Added support for 13.5G JESD204b in the Summary of Features table. Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic. Added a note to the table, Maximum Resource Counts for Arria 10 GT devices. Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | <ul style="list-style-type: none"> Added floating point arithmetic features in the Summary of Features table. Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb. Updated the table that lists the memory standards supported by Intel Arria 10 devices. Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2. Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller. Added soft memory controller support for QDR IV. Updated the maximum resource count table to include the number of hard memory controllers available in each device variant. Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps. Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz. Added a feature for fractional synthesis PLLs: PLL cascading. Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | <ul style="list-style-type: none"> Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX. Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660. Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |
| continued... | | |