# Intel - 10AS032H2F34I2LG Datasheet

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

| **Details** | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 320K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as032h2f34i2lg |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# Key Advantages of Intel Arria 10 Devices

## Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|---|---|
| Enhanced core architecture | • Built on TSMC's 20 nm process technology<br>• 60% higher performance than the previous generation of mid-range FPGAs<br>• 15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | • Short-reach rates up to 25.8 Gigabits per second (Gbps)<br>• Backplane capability up to 12.5 Gbps<br>• Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | • 8-input adaptive logic module (ALM)<br>• Up to 65.6 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks<br>• Fractional synthesis phase-locked loops (PLLs)<br>• Hard PCI Express Gen3 IP blocks<br>• Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | • Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | • Comprehensive set of advanced power saving features<br>• Power-optimized MultiTrack routing and core architecture<br>• Up to 40% lower power compared to previous generation of mid-range FPGAs<br>• Up to 60% lower power compared to previous generation of high-end FPGAs |

# Summary of Intel Arria 10 Features

## Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|---|---|
| Technology | • TSMC's 20-nm SoC process technology<br>• Allows operation at a lower $V_{CC}$ level of 0.82 V instead of the 0.9 V standard $V_{CC}$ core voltage |
| Packaging | • 1.0 mm ball-pitch Fineline BGA packaging<br>• 0.8 mm ball-pitch Ultra Fineline BGA packaging<br>• Multiple devices with identical package footprints for seamless migration between different FPGA densities<br>• Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices<br>• RoHS, leaded(1), and lead-free (Pb-free) options |
| High-performance FPGA fabric | • Enhanced 8-input ALM with four registers<br>• Improved multi-track routing architecture to reduce congestion and improve compilation time<br>• Hierarchical core clocking architecture<br>• Fine-grained partial reconfiguration |
| Internal memory blocks | • M20K—20-Kb memory blocks with hard error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit memory |

*continued...*

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(1) Contact Intel for availability.

| Feature | Description | |
|---|---|---|
| Embedded Hard IP blocks | Variable-precision DSP | • Native support for signal processing precision levels from 18 x 19 to 54 x 54<br>• Native support for 27 x 27 multiplier mode<br>• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)<br>• Internal coefficient memory banks<br>• Preadder/subtractor for improved efficiency<br>• Additional pipeline register to increase performance and reduce power<br>• Supports floating point arithmetic:<br>— Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.<br>— Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.<br>— Dynamic accumulator reset control.<br>— Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks. |
| | Memory controller | DDR4, DDR3, and DDR3L |
| | PCI Express* | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port |
| | Transceiver I/O | • 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)<br>• PCS hard IPs that support:<br>— 10-Gbps Ethernet (10GbE)<br>— PCIe PIPE interface<br>— Interlaken<br>— Gbps Ethernet (GbE)<br>— Common Public Radio Interface (CPRI) with deterministic latency support<br>— Gigabit-capable passive optical network (GPON) with fast lock-time support<br>• 13.5G JESD204b<br>• 8B/10B, 64B/66B, 64B/67B encoders and decoders<br>• Custom mode support for proprietary protocols |
| Core clock networks | • Up to 800 MHz fabric clocking, depending on the application:<br>— 667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface<br>— 800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface<br>• Global, regional, and peripheral clock networks<br>• Clock networks that are not used can be gated to reduce dynamic power | |
| Phase-locked loops (PLLs) | • High-resolution fractional synthesis PLLs:<br>— Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)<br>— Support integer mode and fractional mode<br>— Fractional mode support with third-order delta-sigma modulation<br>• Integer PLLs:<br>— Adjacent to general purpose I/Os<br>— Support external memory and LVDS interfaces | |
| FPGA General-purpose I/Os (GPIOs) | • 1.6 Gbps LVDS—every pair can be configured as receiver or transmitter<br>• On-chip termination (OCT)<br>• 1.2 V to 3.0 V single-ended LVTTL/LVCMOS interfacing | |
| External Memory Interface | • Hard memory controller— DDR4, DDR3, and DDR3L support<br>— DDR4—speeds up to 1,200 MHz/2,400 Mbps<br>— DDR3—speeds up to 1,067 MHz/2,133 Mbps<br>• Soft memory controller—provides support for RLDRAM 3(2), QDR IV(2), and QDR II+ | |

***continued...***

| Feature | Description |
|---|---|
| | • Dynamic reconfiguration of the transceivers and PLLs<br>• Fine-grained partial reconfiguration of the core fabric<br>• Active Serial x4 Interface |
| Power management | • SmartVID<br>• Low static power device options<br>• Programmable Power Technology<br>• Intel Quartus Prime integrated power analysis |
| Software and tools | • Intel Quartus Prime design suite<br>• Transceiver toolkit<br>• Platform Designer system integration tool<br>• DSP Builder for Intel FPGAs<br>• OpenCL™ support<br>• Intel SoC FPGA Embedded Design Suite (EDS) |

### Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

### Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|---|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring:<br>• 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.<br>• 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Maximum Resources

### Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|---|---|---|---|---|---|---|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO (3) | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair (4) | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

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(3) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(4) Each LVDS I/O pair can be used as differential input or output.

### Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|---|---|---|---|---|---|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO (3) | | 696 | 696 | 768 | 768 |
| LVDS Pair (4) | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

## Package Plan

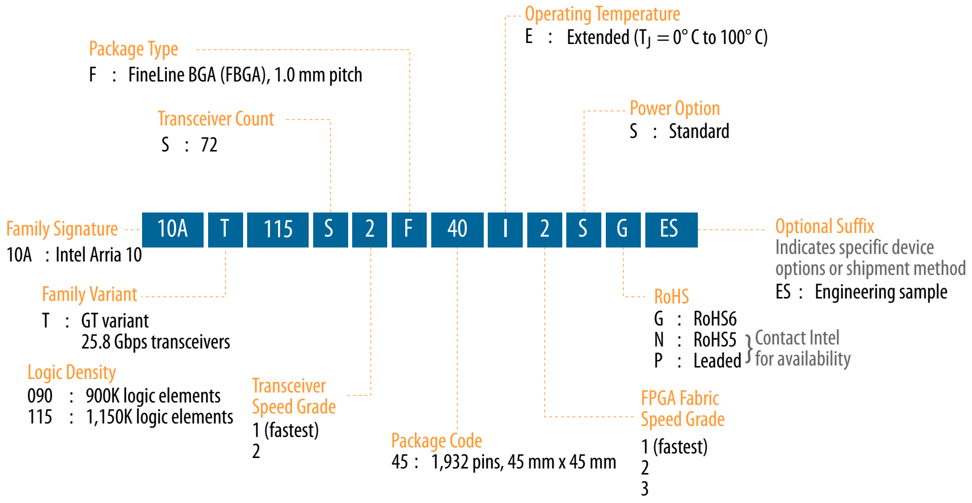
### Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

## Available Options

### Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices



## Embedded Memory Configurations for Single-port Mode

### Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|---|---|---|
| MLAB | 32 | x16, x18, or x20 |
| | 64 (10) | x8, x9, x10 |
| M20K | 512 | x40, x32 |
| | 1K | x20, x16 |
| | 2K | x10, x8 |
| | 4K | x5, x4 |
| | 8K | x2 |
| | 16K | x1 |

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

## Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

## Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

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(10) Supported through software emulation and consumes additional MLAB blocks.

- Series ($R_S$) and parallel ($R_T$) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

External Memory Interface Spec Estimator
Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Related Information**

Intel Arria 10 Device Datasheet
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

**Related Information**

PCS Features on page 30

## Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

### Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

**Related Information**

PCS Features on page 30

### 10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

**Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices**

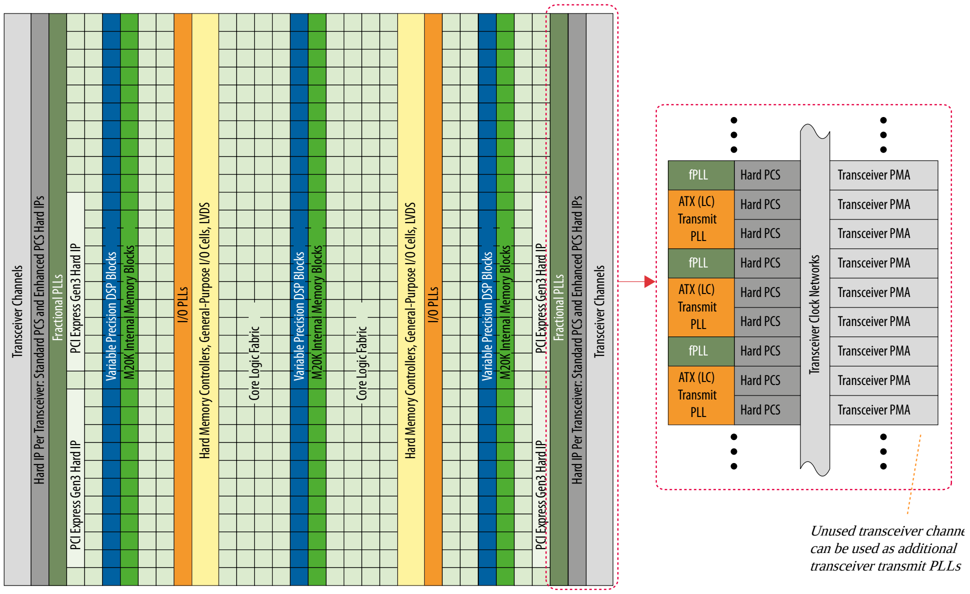
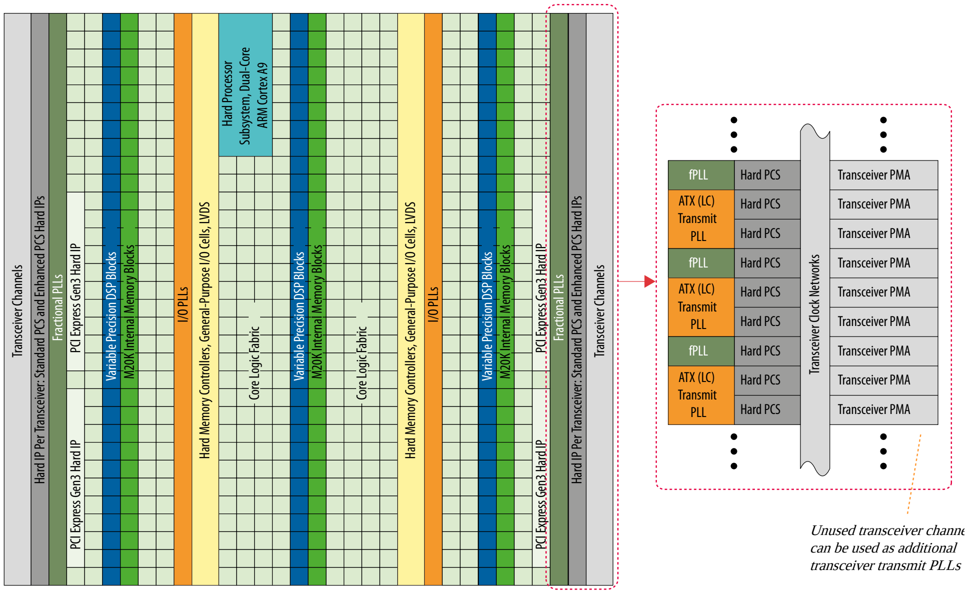


**Figure 8. Device Chip Overview for Intel Arria 10 SX Devices**



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143(12) to 2.97 | Native PHY | Standard PCS |

### Related Information

Intel Arria 10 Transceiver PHY User Guide
Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

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(12) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

### Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:<br>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.<br>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.<br>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or $I^2C$ interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |

## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
    - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
    - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
    - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
    - 32 KB of L1 instruction cache, 32 KB of L1 data cache
    - Single- and double-precision floating-point unit and NEON media engine
    - CoreSight debug and trace technology
    - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I$^2$C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.

## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

## Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

## Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

### Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps)(13) | Decompression | Design Security(14) | Partial Reconfiguration(15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| JTAG | 1 bit | 33 | 33 | — | — | Yes(16) | — |
| Active Serial (AS) through the EPCQ-L configuration device | 1 bit,<br>4 bits | 100 | 400 | Yes | Yes | Yes(16) | Yes |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit | 100 | 100 | Yes | Yes | Yes(16) | Parallel Flash Loader (PFL) IP core |

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(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

(14) Encryption and compression cannot be used simultaneously.

(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(16) Partial configuration can be performed only when it is configured as internal host.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps)(13) | Decompression | Design Security(14) | Partial Reconfiguration(15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes(17) | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes(17) | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes(16) | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

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(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

(14) Encryption and compression cannot be used simultaneously.

(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(17) Supported at a maximum clock rate of 100 MHz.

The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core $V_{CC}$ while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes |
|---|---|
| 2018.04.09 | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|---|---|---|
| January 2018 | 2018.01.17 | • Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.<br>• Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in *Memory Standards Supported by the Soft Memory Controller* table.<br>• Updated transceiver backplane capability to 12.5 Gbps.<br>• Removed transceiver speed grade 5 in *Sample Ordering Core and Available Options for Intel Arria 10 GX Devices* figure. |

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| Date | Version | Changes |
|---|---|---|
| | | • Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from *Sample Ordering Core and Available Options for Intel Arria 10 GT Devices* figure.<br>• Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.<br>• Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from *PMA Features of the Transceivers in Intel Arria 10 Devices* table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | • Corrected protocol names with "1588" to "IEEE 1588v2".<br>• Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.<br>• Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | • Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.<br>• Rebranded as Intel. |
| October 2016 | 2016.10.31 | • Removed package F36 from Intel Arria 10 GX devices.<br>• Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | • Updated the FPGA Configuration and HPS Booting topic.<br>• Remove $V_{CC}$ PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.<br>• Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.<br>• Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | • Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.<br>• Revised the state for Core clock networks in the Summary of Features topic.<br>• Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.<br>• Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.<br>• Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.<br>• Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.<br>• Changed transceiver parameters in the "Low Power Serial Transceivers" section.<br>• Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.<br>• Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.<br>• Changed the datarates for GT devices in the "PMA Features" section.<br>• Changed the datarates for GT devices in the "PCS Features" section. |

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| Date | Version | Changes |
|---|---|---|
| December 2015 | 2015.12.14 | • Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.<br>• Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | • Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.<br>• Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in **Number of Multipliers in Intel Arria 10 Devices** table.<br>• Updated the available options for Arria 10 GX, GT, and SX.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | • Added support for 13.5G JESD204b in the Summary of Features table.<br>• Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.<br>• Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.<br>• Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | • Added floating point arithmetic features in the Summary of Features table.<br>• Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.<br>• Updated the table that lists the memory standards supported by Intel Arria 10 devices.<br>• Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2.<br>• Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller.<br>• Added soft memory controller support for QDR IV.<br>• Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.<br>• Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.<br>• Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.<br>• Added a feature for fractional synthesis PLLs: PLL cascading.<br>• Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | • Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.<br>• Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.<br>• Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |

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