# E·XFL

# Intel - 10AS048E2F29E1HG Datasheet



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Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions. SoCs combine a central

#### Details

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore <sup>™</sup> with CoreSight <sup>™</sup>
Flash Size	-
RAM Size	256КВ
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 480K Logic Elements
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	780-BBGA, FCBGA
Supplier Device Package	780-FBGA, FC (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10as048e2f29e1hg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



# Intel<sup>®</sup> Arria<sup>®</sup> 10 Device Overview

The Intel<sup>®</sup> Arria<sup>®</sup> 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Market	Applications
Wireless	<ul><li>Channel and switch cards in remote radio heads</li><li>Mobile backhaul</li></ul>
Wireline	<ul> <li>40G/100G muxponders and transponders</li> <li>100G line cards</li> <li>Bridging</li> <li>Aggregation</li> </ul>
Broadcast	<ul> <li>Studio switches</li> <li>Servers and transport</li> <li>Videoconferencing</li> <li>Professional audio and video</li> </ul>
Computing and Storage	<ul><li>Flash cache</li><li>Cloud computing servers</li><li>Server acceleration</li></ul>
Medical	<ul><li>Diagnostic scanners</li><li>Diagnostic imaging</li></ul>
Military	<ul> <li>Missile guidance and control</li> <li>Radar</li> <li>Electronic warfare</li> <li>Secure communications</li> </ul>

#### Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

#### **Related Information**

Intel Arria 10 Device Handbook: Known Issues Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.

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# **Key Advantages of Intel Arria 10 Devices**

# Table 2. Key Advantages of the Intel Arria 10 Device Family

Advantage	Supporting Feature
Enhanced core architecture	<ul> <li>Built on TSMC's 20 nm process technology</li> <li>60% higher performance than the previous generation of mid-range FPGAs</li> <li>15% higher performance than the fastest previous-generation FPGA</li> </ul>
High-bandwidth integrated transceivers	<ul> <li>Short-reach rates up to 25.8 Gigabits per second (Gbps)</li> <li>Backplane capability up to 12.5 Gbps</li> <li>Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)</li> </ul>
Improved logic integration and hard IP blocks	<ul> <li>8-input adaptive logic module (ALM)</li> <li>Up to 65.6 megabits (Mb) of embedded memory</li> <li>Variable-precision digital signal processing (DSP) blocks</li> <li>Fractional synthesis phase-locked loops (PLLs)</li> <li>Hard PCI Express Gen3 IP blocks</li> <li>Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)</li> </ul>
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	<ul> <li>Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)</li> <li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li> </ul>
Advanced power savings	<ul> <li>Comprehensive set of advanced power saving features</li> <li>Power-optimized MultiTrack routing and core architecture</li> <li>Up to 40% lower power compared to previous generation of mid-range FPGAs</li> <li>Up to 60% lower power compared to previous generation of high-end FPGAs</li> </ul>

# **Summary of Intel Arria 10 Features**

## Table 3. Summary of Features for Intel Arria 10 Devices

Feature	Description
Technology	<ul> <li>TSMC's 20-nm SoC process technology</li> <li>Allows operation at a lower V<sub>CC</sub> level of 0.82 V instead of the 0.9 V standard V<sub>CC</sub> core voltage</li> </ul>
Packaging	<ul> <li>1.0 mm ball-pitch Fineline BGA packaging</li> <li>0.8 mm ball-pitch Ultra Fineline BGA packaging</li> <li>Multiple devices with identical package footprints for seamless migration between different FPGA densities</li> <li>Devices with compatible package footprints allow migration to next generation high-end Stratix<sup>®</sup> 10 devices</li> <li>RoHS, leaded<sup>(1)</sup>, and lead-free (Pb-free) options</li> </ul>
High-performance FPGA fabric	<ul> <li>Enhanced 8-input ALM with four registers</li> <li>Improved multi-track routing architecture to reduce congestion and improve compilation time</li> <li>Hierarchical core clocking architecture</li> <li>Fine-grained partial reconfiguration</li> </ul>
Internal memory blocks	<ul> <li>M20K—20-Kb memory blocks with hard error correction code (ECC)</li> <li>Memory logic array block (MLAB)—640-bit memory</li> </ul>
	continued

<sup>&</sup>lt;sup>(1)</sup> Contact Intel for availability.



# **Available Options**

## Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## **Related Information**

Transceiver Performance for Intel Arria 10 GX/SX Devices Provides more information about the transceiver speed grade.



# Table 6.Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

Re	source		Product	t Line	
		GX 570	GX 660	GX 900	GX 1150
Logic Elements	(LE) (K)	570	660	900	1,150
ALM		217,080	251,680	339,620	427,200
Register		868,320	1,006,720	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precis	ion DSP Block	1,523 1,687 1,518		1,518	1,518
18 x 19 Multipl	ier	3,046	3,374	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	660         900           251,680         339,620           1,006,720         1,358,480           42,620         48,460           5,788         9,386           1,687         1,518           3,374         3,036           16         32           16         16           48         96           696         768           324         384           2         4	16	
17.4 Gbps Trar	isceiver	48	48	96	96
GPIO <sup>(3)</sup>		696	696	768	768
LVDS Pair <sup>(4)</sup>		324	324	384	384
PCIe Hard IP B	lock	2	2	4	4
Hard Memory (	Controller	16	16	16	16

# Package Plan

# Table 7.Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			(27 67	F27 mm × 27 n 72-pin FBG/	nm, A)	F29 (29 mm × 29 mm, 780-pin FBGA)			
	3 V I/O	LVDS I/O	XCVR	3 V I/O LVDS I/O XCVR			3 V I/O	LVDS I/O	XCVR	
GX 160	48	192	6	48	192	12	48	240	12	
GX 220	48	192	6	48	192	12	48	240	12	
GX 270	-	_	_	48	192	12	48	312	12	
GX 320	-	-	_	48	192	12	48	312	12	
GX 480	_	_	_	_	_	_	48	312	12	



# **Maximum Resources**

### Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

Reso	urce	Produc	ct Line	
		GT 900	GT 1150	
Logic Elements (LE) (K)		900	1,150	
ALM		339,620	427,200	
Register		1,358,480	1,708,800	
Memory (Kb)	M20K	48,460	54,260	
	MLAB	9,386	12,984	
Variable-precision DSP Block		1,518	1,518	
18 x 19 Multiplier		3,036	3,036	
PLL	Fractional Synthesis	32	32	
	I/O	16	16	
Transceiver	17.4 Gbps	72 <sup>(5)</sup>	72 <sup>(5)</sup>	
	25.8 Gbps	6	6	
GPIO <sup>(6)</sup>		624	624	
LVDS Pair <sup>(7)</sup>		312	312	
PCIe Hard IP Block		4	4	
Hard Memory Controller		16	16	

## **Related Information**

#### Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

# Package Plan

## Table 11.Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	SF45 (45 mm × 45 mm, 1932-pin FBGA)						
	3 V I/O	LVDS I/O	XCVR				
GT 900	—	624	72				
GT 1150	—	624	72				

<sup>&</sup>lt;sup>(5)</sup> If all 6 GT channels are in use, 12 of the GX channels are not usable.

<sup>&</sup>lt;sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>&</sup>lt;sup>(7)</sup> Each LVDS I/O pair can be used as differential input or output.



## **Related Information**

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

# **Intel Arria 10 SX**

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

## **Related Information**

Intel FPGA Product Selector

Provides the latest information on Intel products.

## **Available Options**

#### Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices



#### **Related Information**

Transceiver Performance for Intel Arria 10 GX/SX Devices Provides more information about the transceiver speed grade.



## **Maximum Resources**

## Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

Reso	ource		Product Line								
		SX 160	SX 220	SX 270	Product Line           SX 270         SX 320         SX 480         SX 570         SX           270         320         480         570         SX           01,620         119,900         183,590         217,080         25           06,480         479,600         734,360         868,320         1,0           15,000         17,820         28,620         36,000         4           2,452         2,727         4,164         5,096         5           830         985         1,368         1,523         1           1,660         1,970         2,736         3,046         3           8         8         12         16         1           24         24         36         48         4           384         384         492         696         1			SX 660			
Logic Elements	s (LE) (K)	160	220	270	320	480	570	660			
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680			
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720			
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620			
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788			
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687			
18 x 19 Multip	18 x 19 Multiplier		384	1,660	1,970	2,736	3,046	3,374			
PLL	Fractional Synthesis	6	6	8	8	12	16	16			
	I/O	6	6	8	8	12	16	16			
17.4 Gbps Trai	nsceiver	12	12	24	24	36	48	48			
GPIO <sup>(8)</sup>		288	288	384	384	492	696	696			
LVDS Pair <sup>(9)</sup>		120	120	168	168	174	324	324			
PCIe Hard IP E	Block	1	1	2	2	2	2	2			
Hard Memory	Controller	6	6	8	8	12	16	16			
ARM Cortex-A9 Processor	9 MPCore	Yes	Yes	Yes	Yes	Yes	Yes	Yes			

# Package Plan

# Table 13.Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)		F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)			
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	-	-	-
SX 220	48	144	6	48	192	12	48	240	12	_	-	-
SX 270	-	-	_	48	192	12	48	312	12	48	336	24
SX 320	-	-	_	48	192	12	48	312	12	48	336	24
											contii	nued

<sup>&</sup>lt;sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.



Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)		19         F27           × 19 mm, 1 UBGA)         (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)			
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 480	-	-	-	-	-	-	48	312	12	48	444	24
SX 570	-	-	-	-	-	—	-	-	-	48	444	24
SX 660	-	_	-	_	-	_	-	-	-	48	444	24

## Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			(40 15	KF40 mm × 40 n 17-pin FBG	nm, A)	(40 15	NF40 mm × 40 n 17-pin FBG	nm, A)
	3 V I/O	LVDS I/O	XCVR	3 V I/O LVDS I/O XCVR			3 V I/O	LVDS I/O	XCVR
SX 270	48	336	24	_	-		_	_	—
SX 320	48	336	24	_	_	—	_	_	—
SX 480	48	348	36	_	_	_	_	_	_
SX 570	48	348	36	96	600	36	48	540	48
SX 660	48	348	36	96	600	36	48	540	48

## **Related Information**

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



# I/O Vertical Migration for Intel Arria 10 Devices

## Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use
  memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to
  banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
  - Package Product Variant Line U19 F27 KF40 NF40 RF40 NF45 SF45 UF45 F29 F34 F35 GX 160 GX 220 GX 270 GX 320 Intel® Arria® 10 GX GX 480 GX 570 GX 660 GX 900 GX 1150 GT 900 Intel Arria 10 GT GT 1150 SX 160 SX 220 SX 270 Intel Arria 10 SX SX 320 SX 480 SX 570 SX 660
- Some migration paths are not shown in the Intel Quartus Prime software Pin Migration View.

*Note:* To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

# **Adaptive Logic Module**

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



## Figure 5. ALM for Intel Arria 10 Devices



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

# **Variable-Precision DSP Block**

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Variant	Product Line	Variable- precision DSP Block	Independent In Multiplicatio	put and Output ns Operator	18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
	SX 320	984	1,968	984	984	984
	SX 480	1,368	2,736	1,368	1,368	1,368
	SX 570	1,523	3,046	1,523	1,523	1,523
	SX 660	1,687	3,374	1,687	1,687	1,687

# Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable- precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single- Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating- Point Operations per Second (GFLOPs)
Intel Arria 10	GX 160	156	156	156	156	140
GX	GX 220	192	192	192	192	173
	GX 270	830	830	830	830	747
	GX 320	984	984	984	984	886
	GX 480	1,369	1,368	1,368	1,368	1,231
	GX 570	1,523	1,523	1,523	1,523	1,371
	GX 660	1,687	1,687	1,687	1,687	1,518
	GX 900	1,518	1,518	1,518	1,518	1,366
	GX 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 GT	GT 900	1,518	1,518	1,518	1,518	1,366
	GT 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10	SX 160	156	156	156	156	140
SX	SX 220	192	192	192	192	173
	SX 270	830	830	830	830	747
	SX 320	984	984	984	984	886
	SX 480	1,369	1,368	1,368	1,368	1,231
	SX 570	1,523	1,523	1,523	1,523	1,371
	SX 660	1,687	1,687	1,687	1,687	1,518

# **Embedded Memory Blocks**

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

# **External Memory Interface**

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened highperformance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios<sup>®</sup> II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

## **Related Information**

#### External Memory Interface Spec Estimator

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

# **Memory Standards Supported by Intel Arria 10 Devices**

The I/Os are designed to provide high performance support for existing and emerging external memory standards.



### Table 20. Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		-	1,200
DDR3 SDRAM	Half rate	Yes	533
		-	667
	Quarter rate	Yes	1,067
		-	1,067
DDR3L SDRAM	Half rate	Yes	533
		-	667
	Quarter rate	Yes	933
		-	933
LPDDR3 SDRAM	Half rate	-	533
	Quarter rate	-	800

## Table 21. Memory Standards Supported by the Soft Memory Controller

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 (11)	Quarter rate	1,200
QDR IV SRAM <sup>(11)</sup>	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

## Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

<sup>&</sup>lt;sup>(11)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



## **Related Information**

#### Intel Arria 10 Device Datasheet

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

# PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

#### **Related Information**

PCS Features on page 30

# **Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet**

# **Interlaken Support**

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

#### **Related Information**

PCS Features on page 30

## **10 Gbps Ethernet Support**

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.





# Figure 6. Intel Arria 10 Transceiver Block Architecture

# **Transceiver Channels**

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other preprocessing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



## Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices



Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



# **PMA Features**

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.



## **System Peripherals and Debug Access Port**

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## **HPS-FPGA AXI Bridges**

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI<sup>m</sup>) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

### **HPS SDRAM Controller Subsystem**

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon<sup>®</sup> Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) (13)	Decompression	Design Security <sup>(1</sup> 4)	Partial Reconfiguration (15)	Remote System Update
Fast passive	8 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	PFL IP core
through CPLD or	16 bits			Yes	Yes		
microcontroller	32 bits			Yes	Yes		
Configuration via	16 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	_
пръ	32 bits			Yes	Yes		
Configuration via Protocol [CvP (PCIe*)]	x1, x2, x4, x8 lanes	_	8000	Yes	Yes	Yes <sup>(16)</sup>	_

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

# **SEU Error Detection and Correction**

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

# **Power Management**

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

<sup>&</sup>lt;sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>&</sup>lt;sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>&</sup>lt;sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>&</sup>lt;sup>(17)</sup> Supported at a maximum clock rate of 100 MHz.



The optional power reduction techniques in Intel Arria 10 devices include:

- SmartVID—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V<sub>CC</sub> while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- Low Static Power Options—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

# **Incremental Compilation**

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

# **Document Revision History for Intel Arria 10 Device Overview**

Document Version	Changes
2018.04.09	Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	<ul> <li>Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li> </ul>
		<ul> <li>Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft</i> <i>Memory Controller</i> table.</li> </ul>
		Updated transceiver backplane capability to 12.5 Gbps.
		• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.
		continued

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Date	Version	Changes
August 2014	2014.08.18	<ul> <li>Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.</li> </ul>
		<ul> <li>Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.</li> </ul>
		• Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.
		<ul> <li>Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.</li> </ul>
		<ul> <li>Added variable precision DSP blocks support for floating-point arithmetic.</li> </ul>
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	<ul> <li>Updated the HPS memory standards support from LPDDR2 to LPDDR3.</li> <li>Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .</li> </ul>
December 2013	2013.12.02	Initial release.