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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 480K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as048h1f34i1hg |

# Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market | Applications |
|---|---|
| Wireless | • Channel and switch cards in remote radio heads<br>• Mobile backhaul |
| Wireline | • 40G/100G muxponders and transponders<br>• 100G line cards<br>• Bridging<br>• Aggregation |
| Broadcast | • Studio switches<br>• Servers and transport<br>• Videoconferencing<br>• Professional audio and video |
| Computing and Storage | • Flash cache<br>• Cloud computing servers<br>• Server acceleration |
| Medical | • Diagnostic scanners<br>• Diagnostic imaging |
| Military | • Missile guidance and control<br>• Radar<br>• Electronic warfare<br>• Secure communications |

## Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.

# Key Advantages of Intel Arria 10 Devices

## Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|---|---|
| Enhanced core architecture | • Built on TSMC's 20 nm process technology<br>• 60% higher performance than the previous generation of mid-range FPGAs<br>• 15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | • Short-reach rates up to 25.8 Gigabits per second (Gbps)<br>• Backplane capability up to 12.5 Gbps<br>• Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | • 8-input adaptive logic module (ALM)<br>• Up to 65.6 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks<br>• Fractional synthesis phase-locked loops (PLLs)<br>• Hard PCI Express Gen3 IP blocks<br>• Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | • Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | • Comprehensive set of advanced power saving features<br>• Power-optimized MultiTrack routing and core architecture<br>• Up to 40% lower power compared to previous generation of mid-range FPGAs<br>• Up to 60% lower power compared to previous generation of high-end FPGAs |

# Summary of Intel Arria 10 Features

## Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|---|---|
| Technology | • TSMC's 20-nm SoC process technology<br>• Allows operation at a lower $V_{CC}$ level of 0.82 V instead of the 0.9 V standard $V_{CC}$ core voltage |
| Packaging | • 1.0 mm ball-pitch Fineline BGA packaging<br>• 0.8 mm ball-pitch Ultra Fineline BGA packaging<br>• Multiple devices with identical package footprints for seamless migration between different FPGA densities<br>• Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices<br>• RoHS, leaded(1), and lead-free (Pb-free) options |
| High-performance FPGA fabric | • Enhanced 8-input ALM with four registers<br>• Improved multi-track routing architecture to reduce congestion and improve compilation time<br>• Hierarchical core clocking architecture<br>• Fine-grained partial reconfiguration |
| Internal memory blocks | • M20K—20-Kb memory blocks with hard error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit memory |

***continued...***

(1) Contact Intel for availability.

| Feature | Description | |
|---|---|---|
| Low-power serial transceivers | • Continuous operating range:<br>— Intel Arria 10 GX—1 Gbps to 17.4 Gbps<br>— Intel Arria 10 GT—1 Gbps to 25.8 Gbps<br>• Backplane support:<br>— Intel Arria 10 GX—up to 12.5<br>— Intel Arria 10 GT—up to 12.5<br>• Extended range down to 125 Mbps with oversampling<br>• ATX transmit PLLs with user-configurable fractional synthesis capability<br>• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module<br>• Adaptive linear and decision feedback equalization<br>• Transmitter pre-emphasis and de-emphasis<br>• Dynamic partial reconfiguration of individual transceiver channels | |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system | • Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability<br>• 256 KB on-chip RAM and 64 KB on-chip ROM<br>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers<br>• Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)<br>• ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage |
| | External interfaces | • Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller<br>• Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-GO (OTG) controllers, $I^2C$ controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os) |
| | Interconnects to core | • High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write<br>• HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa<br>• Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port<br>• FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller |
| Configuration | • Tamper protection—comprehensive design protection to protect your valuable IP investments<br>• Enhanced 256-bit advanced encryption standard (AES) design security with authentication<br>• Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3 | |

***continued...***

(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

| Feature | Description |
|---|---|
| | • Dynamic reconfiguration of the transceivers and PLLs<br>• Fine-grained partial reconfiguration of the core fabric<br>• Active Serial x4 Interface |
| Power management | • SmartVID<br>• Low static power device options<br>• Programmable Power Technology<br>• Intel Quartus Prime integrated power analysis |
| Software and tools | • Intel Quartus Prime design suite<br>• Transceiver toolkit<br>• Platform Designer system integration tool<br>• DSP Builder for Intel FPGAs<br>• OpenCL™ support<br>• Intel SoC FPGA Embedded Design Suite (EDS) |

### Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

### Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|---|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring:<br>• 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.<br>• 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Maximum Resources

### Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|---|---|---|---|---|---|---|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO (3) | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair (4) | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

(3) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(4) Each LVDS I/O pair can be used as differential input or output.

### Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|---|---|---|---|---|---|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO (3) | | 696 | 696 | 768 | 768 |
| LVDS Pair (4) | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

## Package Plan

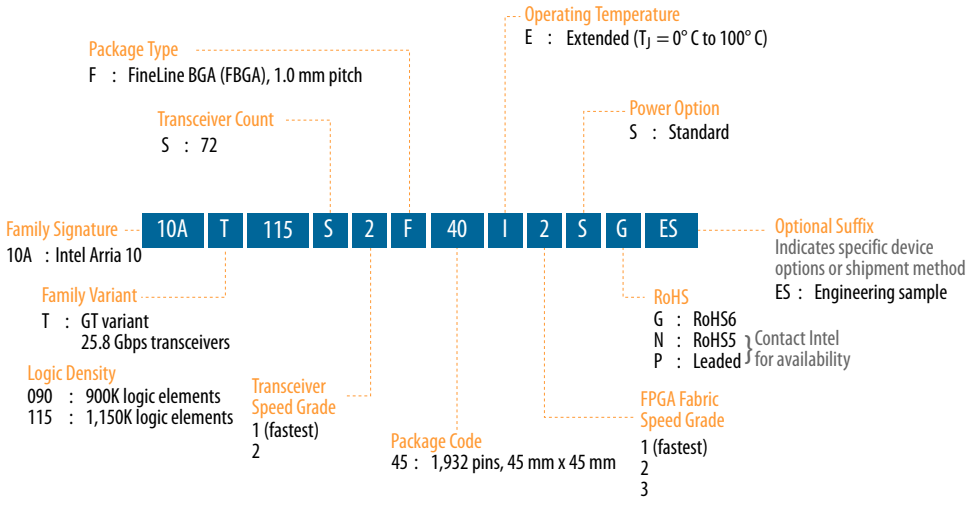
### Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

## Available Options

### Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices



## Maximum Resources

### Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

| Resource | | Product Line | |
|---|---|---|---|
| | | GT 900 | GT 1150 |
| Logic Elements (LE) (K) | | 900 | 1,150 |
| ALM | | 339,620 | 427,200 |
| Register | | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 48,460 | 54,260 |
| | MLAB | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 32 | 32 |
| | I/O | 16 | 16 |
| Transceiver | 17.4 Gbps | 72 (5) | 72 (5) |
| | 25.8 Gbps | 6 | 6 |
| GPIO(6) | | 624 | 624 |
| LVDS Pair(7) | | 312 | 312 |
| PCIe Hard IP Block | | 4 | 4 |
| Hard Memory Controller | | 16 | 16 |

#### Related Information

Intel Arria 10 GT Channel Usage
Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

### Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45 (45 mm × 45 mm, 1932-pin FBGA) | | |
|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR |
| GT 900 | — | 624 | 72 |
| GT 1150 | — | 624 | 72 |

(5) If all 6 GT channels are in use, 12 of the GX channels are not usable.

(6) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(7) Each LVDS I/O pair can be used as differential input or output.

### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook
Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

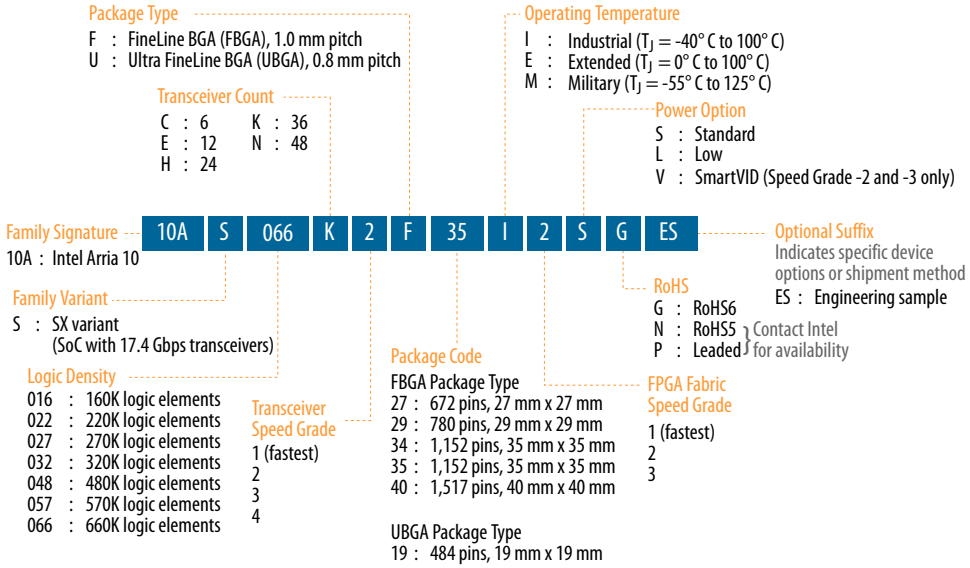
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



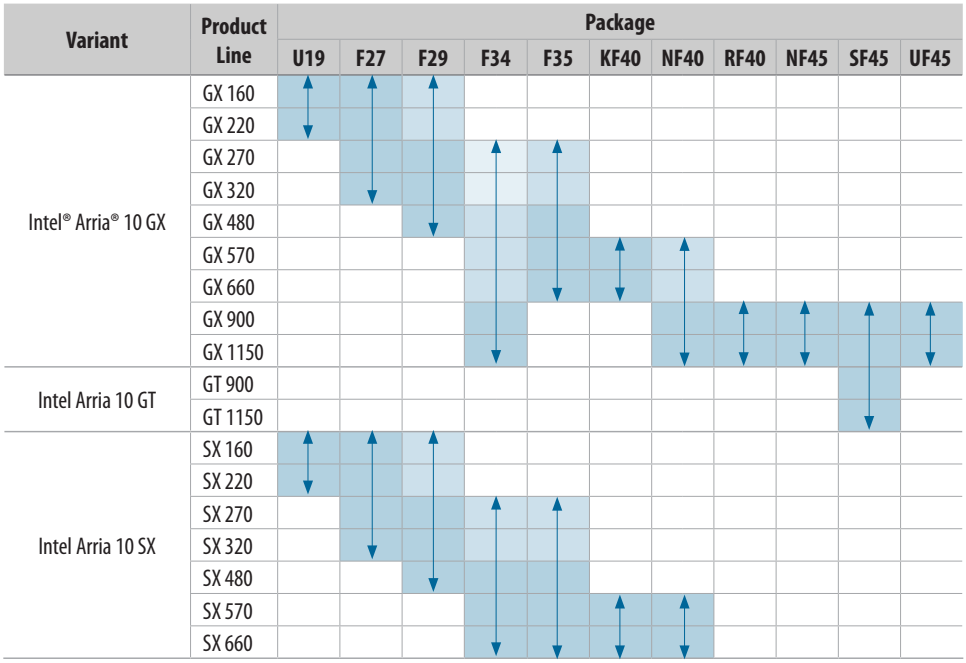

### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices
Provides more information about the transceiver speed grade.

# I/O Vertical Migration for Intel Arria 10 Devices

## Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.




*Note:* To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

# Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

**Related Information**

Intel Arria 10 Device Datasheet
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

**Related Information**

PCS Features on page 30

## Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

### Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

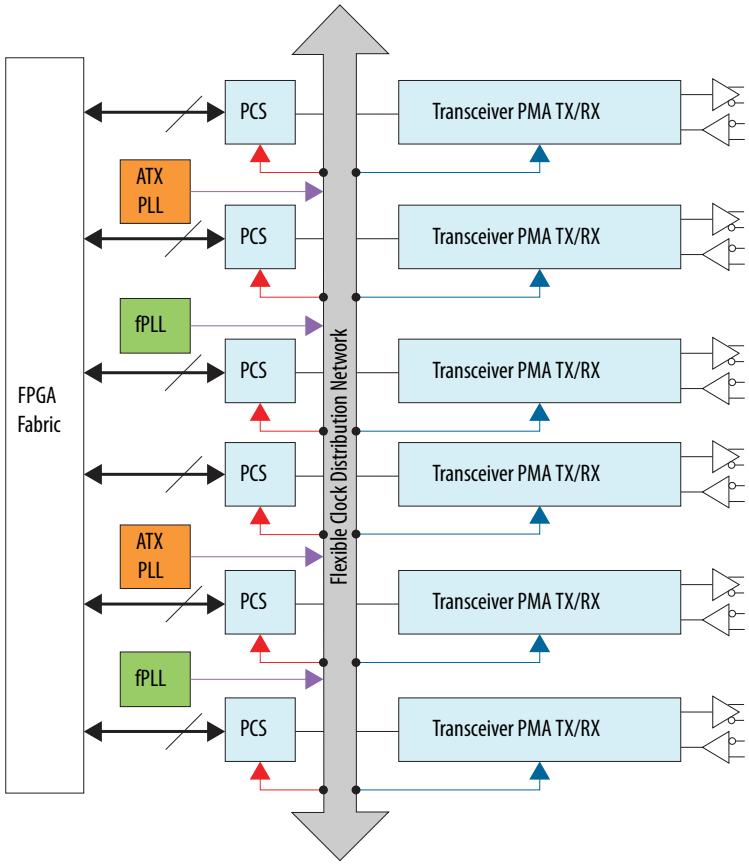
**Related Information**

PCS Features on page 30

### 10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

**Figure 6. Intel Arria 10 Transceiver Block Architecture**




## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.

| PCS | Description |
|---|---|
| Standard PCS | • Operates at a data rate up to 12 Gbps<br>• Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS<br>• Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | • Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA<br>• Handles data transfer to and from the FPGA fabric<br>• Handles data transfer internally to and from the PMA<br>• Provides frequency compensation<br>• Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | • Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates<br>• Provides support for PIPE 3.0 features<br>• Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

### Related Information

- PCIe Gen1, Gen2, and Gen3 Hard IP on page 26
- Interlaken Support on page 26
- 10 Gbps Ethernet Support on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |

***continued...***

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143[(12)] to 2.97 | Native PHY | Standard PCS |

### Related Information

Intel Arria 10 Transceiver PHY User Guide
Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

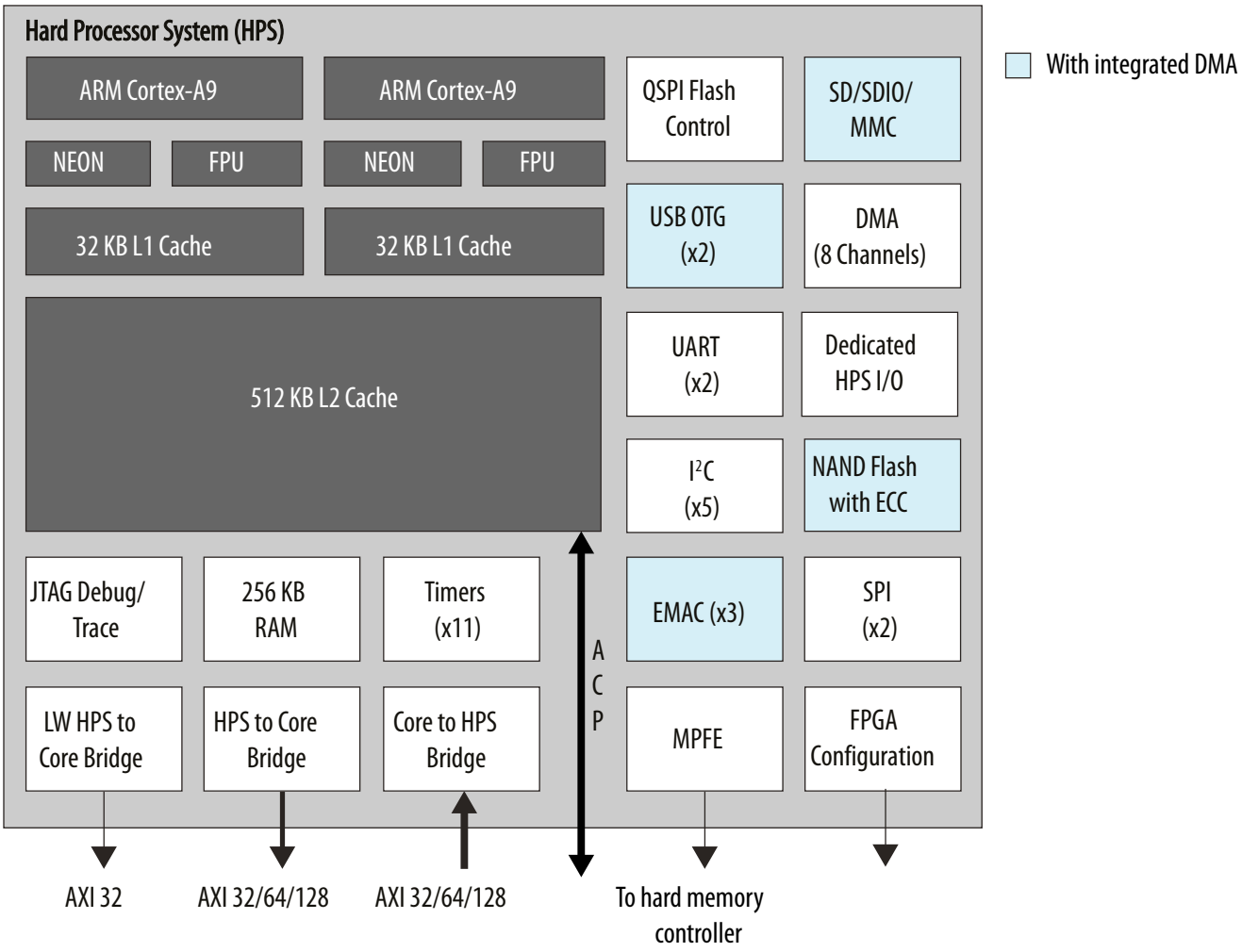
Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

(12) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.




## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - — ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - — Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - — Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - — 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - — Single- and double-precision floating-point unit and NEON media engine
  - — CoreSight debug and trace technology
  - — Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 $I^2C$ controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.

## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

# Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

## Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

## Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core $V_{CC}$ while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes |
|---|---|
| 2018.04.09 | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|---|---|---|
| January 2018 | 2018.01.17 | • Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.<br>• Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in *Memory Standards Supported by the Soft Memory Controller* table.<br>• Updated transceiver backplane capability to 12.5 Gbps.<br>• Removed transceiver speed grade 5 in *Sample Ordering Core and Available Options for Intel Arria 10 GX Devices* figure. |

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| Date | Version | Changes |
|---|---|---|
| December 2015 | 2015.12.14 | • Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.<br>• Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | • Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.<br>• Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in **Number of Multipliers in Intel Arria 10 Devices** table.<br>• Updated the available options for Arria 10 GX, GT, and SX.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | • Added support for 13.5G JESD204b in the Summary of Features table.<br>• Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.<br>• Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.<br>• Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | • Added floating point arithmetic features in the Summary of Features table.<br>• Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.<br>• Updated the table that lists the memory standards supported by Intel Arria 10 devices.<br>• Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2.<br>• Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller.<br>• Added soft memory controller support for QDR IV.<br>• Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.<br>• Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.<br>• Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.<br>• Added a feature for fractional synthesis PLLs: PLL cascading.<br>• Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | • Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.<br>• Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.<br>• Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |

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