# Intel - 10AS048H2F34I2SG Datasheet

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 480K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as048h2f34i2sg |

# Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market | Applications |
|---|---|
| Wireless | • Channel and switch cards in remote radio heads<br>• Mobile backhaul |
| Wireline | • 40G/100G muxponders and transponders<br>• 100G line cards<br>• Bridging<br>• Aggregation |
| Broadcast | • Studio switches<br>• Servers and transport<br>• Videoconferencing<br>• Professional audio and video |
| Computing and Storage | • Flash cache<br>• Cloud computing servers<br>• Server acceleration |
| Medical | • Diagnostic scanners<br>• Diagnostic imaging |
| Military | • Missile guidance and control<br>• Radar<br>• Electronic warfare<br>• Secure communications |

## Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.

# Key Advantages of Intel Arria 10 Devices

## Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|---|---|
| Enhanced core architecture | • Built on TSMC's 20 nm process technology<br>• 60% higher performance than the previous generation of mid-range FPGAs<br>• 15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | • Short-reach rates up to 25.8 Gigabits per second (Gbps)<br>• Backplane capability up to 12.5 Gbps<br>• Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | • 8-input adaptive logic module (ALM)<br>• Up to 65.6 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks<br>• Fractional synthesis phase-locked loops (PLLs)<br>• Hard PCI Express Gen3 IP blocks<br>• Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | • Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | • Comprehensive set of advanced power saving features<br>• Power-optimized MultiTrack routing and core architecture<br>• Up to 40% lower power compared to previous generation of mid-range FPGAs<br>• Up to 60% lower power compared to previous generation of high-end FPGAs |

# Summary of Intel Arria 10 Features

## Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|---|---|
| Technology | • TSMC's 20-nm SoC process technology<br>• Allows operation at a lower $V_{CC}$ level of 0.82 V instead of the 0.9 V standard $V_{CC}$ core voltage |
| Packaging | • 1.0 mm ball-pitch Fineline BGA packaging<br>• 0.8 mm ball-pitch Ultra Fineline BGA packaging<br>• Multiple devices with identical package footprints for seamless migration between different FPGA densities<br>• Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices<br>• RoHS, leaded(1), and lead-free (Pb-free) options |
| High-performance FPGA fabric | • Enhanced 8-input ALM with four registers<br>• Improved multi-track routing architecture to reduce congestion and improve compilation time<br>• Hierarchical core clocking architecture<br>• Fine-grained partial reconfiguration |
| Internal memory blocks | • M20K—20-Kb memory blocks with hard error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit memory |

***continued...***

(1) Contact Intel for availability.

| Feature | Description | |
|---|---|---|
| Embedded Hard IP blocks | Variable-precision DSP | • Native support for signal processing precision levels from 18 x 19 to 54 x 54<br>• Native support for 27 x 27 multiplier mode<br>• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)<br>• Internal coefficient memory banks<br>• Preadder/subtractor for improved efficiency<br>• Additional pipeline register to increase performance and reduce power<br>• Supports floating point arithmetic:<br>— Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.<br>— Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.<br>— Dynamic accumulator reset control.<br>— Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks. |
| | Memory controller | DDR4, DDR3, and DDR3L |
| | PCI Express* | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port |
| | Transceiver I/O | • 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)<br>• PCS hard IPs that support:<br>— 10-Gbps Ethernet (10GbE)<br>— PCIe PIPE interface<br>— Interlaken<br>— Gbps Ethernet (GbE)<br>— Common Public Radio Interface (CPRI) with deterministic latency support<br>— Gigabit-capable passive optical network (GPON) with fast lock-time support<br>• 13.5G JESD204b<br>• 8B/10B, 64B/66B, 64B/67B encoders and decoders<br>• Custom mode support for proprietary protocols |
| Core clock networks | • Up to 800 MHz fabric clocking, depending on the application:<br>— 667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface<br>— 800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface<br>• Global, regional, and peripheral clock networks<br>• Clock networks that are not used can be gated to reduce dynamic power | |
| Phase-locked loops (PLLs) | • High-resolution fractional synthesis PLLs:<br>— Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)<br>— Support integer mode and fractional mode<br>— Fractional mode support with third-order delta-sigma modulation<br>• Integer PLLs:<br>— Adjacent to general purpose I/Os<br>— Support external memory and LVDS interfaces | |
| FPGA General-purpose I/Os (GPIOs) | • 1.6 Gbps LVDS—every pair can be configured as receiver or transmitter<br>• On-chip termination (OCT)<br>• 1.2 V to 3.0 V single-ended LVTTL/LVCMOS interfacing | |
| External Memory Interface | • Hard memory controller— DDR4, DDR3, and DDR3L support<br>— DDR4—speeds up to 1,200 MHz/2,400 Mbps<br>— DDR3—speeds up to 1,067 MHz/2,133 Mbps<br>• Soft memory controller—provides support for RLDRAM 3(2), QDR IV(2), and QDR II+ | |

***continued...***

### Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

### Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

#### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

#### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook
Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

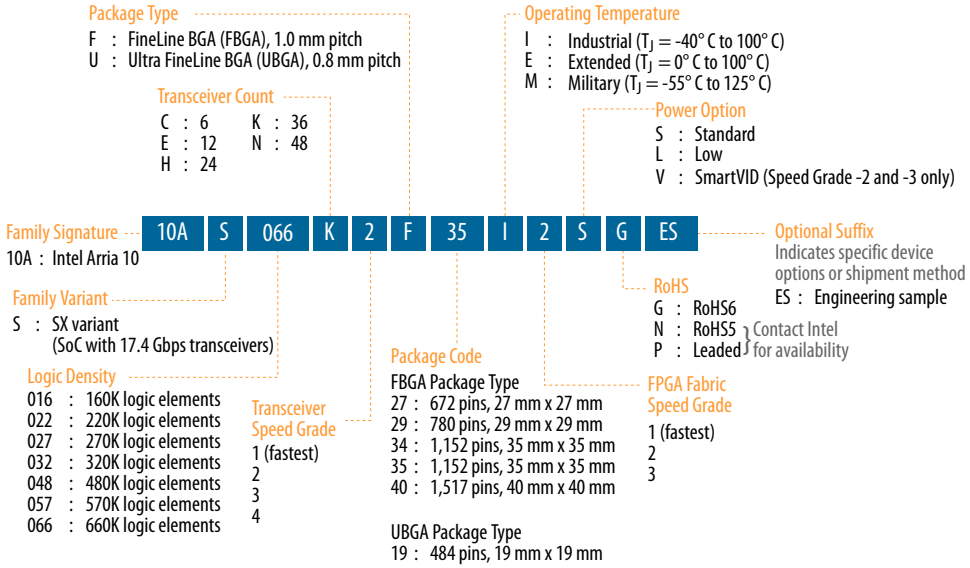
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**




### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices
Provides more information about the transceiver speed grade.

## Maximum Resources

### Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

| Resource | | Product Line | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | SX 160 | SX 220 | SX 270 | SX 320 | SX 480 | SX 570 | SX 660 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 | 570 | 660 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 | 217,080 | 251,680 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 | 36,000 | 42,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 | 5,096 | 5,788 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 | 1,523 | 1,687 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 | 3,046 | 3,374 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| | I/O | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 | 48 | 48 |
| GPIO (8) | | 288 | 288 | 384 | 384 | 492 | 696 | 696 |
| LVDS Pair (9) | | 120 | 120 | 168 | 168 | 174 | 324 | 324 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| ARM Cortex-A9 MPCore Processor | | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

## Package Plan

### Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 160 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 220 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| SX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |

*continued...*

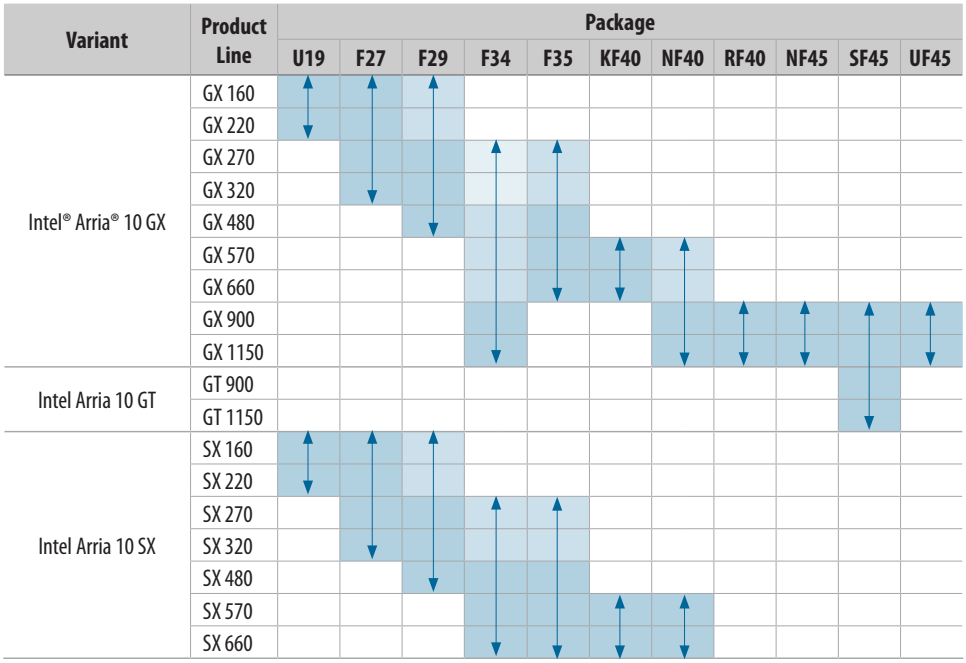
(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(9) Each LVDS I/O pair can be used as differential input or output.

# I/O Vertical Migration for Intel Arria 10 Devices

## Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.




*Note:* To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

# Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

### Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

| Variant | Product Line | M20K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Intel Arria 10 GX | GX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | GX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | GX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | GX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | GX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | GX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | GX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |
| | GX 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GX 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 GT | GT 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GT 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 SX | SX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | SX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | SX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | SX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | SX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | SX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | SX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |

## Table 20. Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|---|---|---|---|
| DDR4 SDRAM | Quarter rate | Yes | 1,067 |
| | | — | 1,200 |
| DDR3 SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 1,067 |
| | | — | 1,067 |
| DDR3L SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 933 |
| | | — | 933 |
| LPDDR3 SDRAM | Half rate | — | 533 |
| | Quarter rate | — | 800 |

## Table 21. Memory Standards Supported by the Soft Memory Controller

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| RLDRAM 3 (11) | Quarter rate | 1,200 |
| QDR IV SRAM(11) | Quarter rate | 1,067 |
| QDR II SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ Xtreme SRAM | Full rate | 333 |
| | Half rate | 633 |

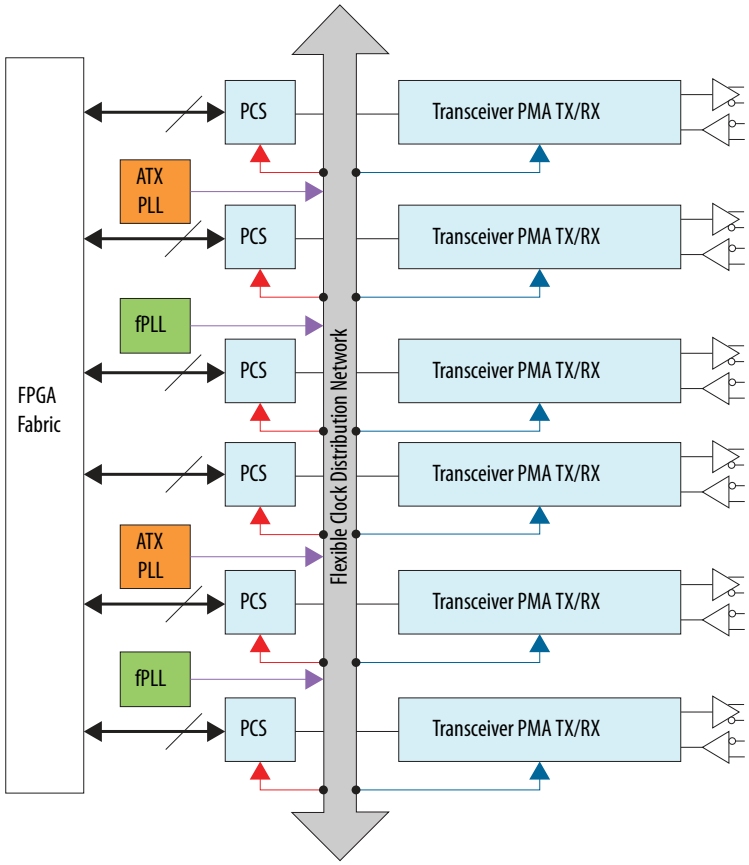
## Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,067 |
| DDR3L SDRAM | Half rate | 933 |

(11) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

**Figure 6. Intel Arria 10 Transceiver Block Architecture**




## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.

**Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices**

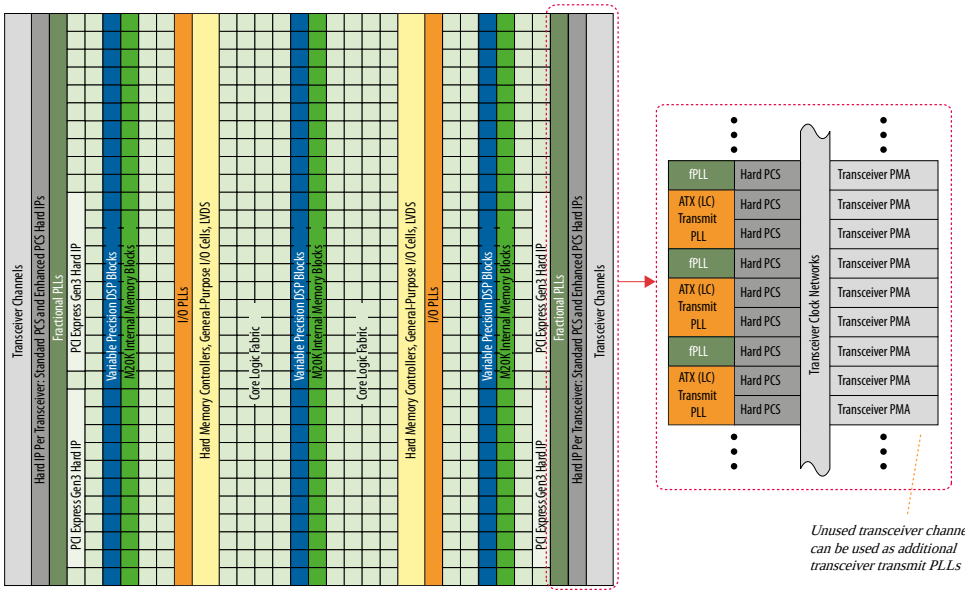
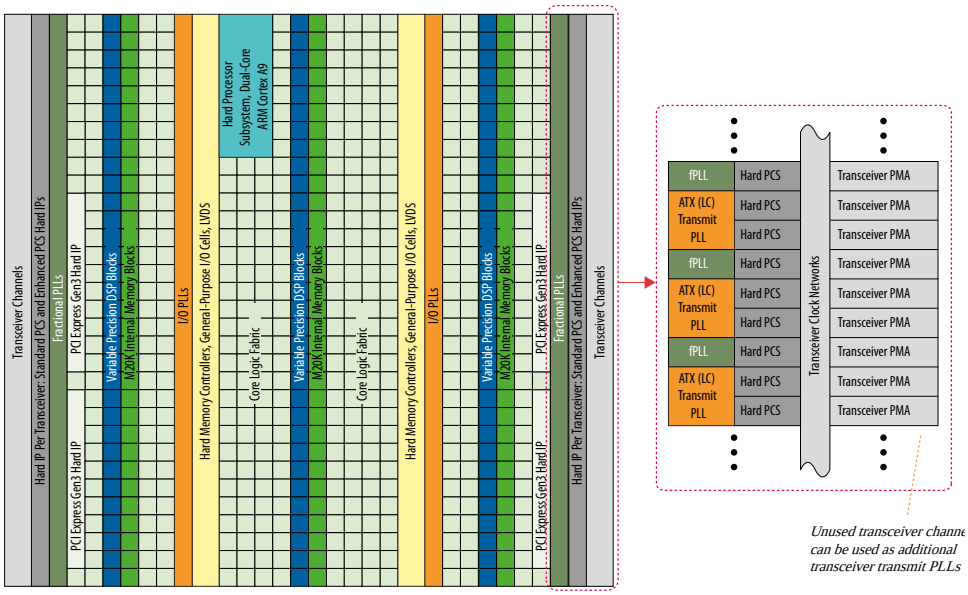



**Figure 8. Device Chip Overview for Intel Arria 10 SX Devices**




## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

| Feature | Capability |
|---|---|
| Chip-to-Chip Data Rates | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices) |
| Backplane Support | Drive backplanes at data rates up to 12.5 Gbps |
| Optical Module Support | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4 |
| Cable Driving Support | SFP+ Direct Attach, PCI Express over cable, eSATA |
| Transmit Pre-Emphasis | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss |
| Continuous Time Linear Equalizer (CTLE) | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss |
| Decision Feedback Equalizer (DFE) | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments |
| Variable Gain Amplifier | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes |
| Altera Digital Adaptive Parametric Tuning (ADAPT) | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance |
| Advanced Transmit (ATX) PLL | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols |
| Fractional PLLs | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost |
| Digitally Assisted Analog CDR | Superior jitter tolerance with fast lock time |
| Dynamic Partial Reconfiguration | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility |
| Multiple PCS-PMA and PCS-PLD interface widths | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

| PCS | Description |
|---|---|
| Standard PCS | • Operates at a data rate up to 12 Gbps<br>• Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS<br>• Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | • Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA<br>• Handles data transfer to and from the FPGA fabric<br>• Handles data transfer internally to and from the PMA<br>• Provides frequency compensation<br>• Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | • Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates<br>• Provides support for PIPE 3.0 features<br>• Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

### Related Information

- PCIe Gen1, Gen2, and Gen3 Hard IP on page 26
- Interlaken Support on page 26
- 10 Gbps Ethernet Support on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |

***continued...***

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143[(12)] to 2.97 | Native PHY | Standard PCS |

### Related Information

Intel Arria 10 Transceiver PHY User Guide
Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

(12) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

## Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:<br>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.<br>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.<br>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or $I^2C$ interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.

## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

# Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

## Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

## Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

### Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) (13) | Decompression | Design Security (14) | Partial Reconfiguration (15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| JTAG | 1 bit | 33 | 33 | — | — | Yes(16) | — |
| Active Serial (AS) through the EPCQ-L configuration device | 1 bit, 4 bits | 100 | 400 | Yes | Yes | Yes(16) | Yes |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit | 100 | 100 | Yes | Yes | Yes(16) | Parallel Flash Loader (PFL) IP core |

*continued...*

(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

(14) Encryption and compression cannot be used simultaneously.

(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(16) Partial configuration can be performed only when it is configured as internal host.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) (13) | Decompression | Design Security (14) | Partial Reconfiguration (15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes(17) | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes(17) | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes(16) | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.
(14) Encryption and compression cannot be used simultaneously.
(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(17) Supported at a maximum clock rate of 100 MHz.

| Date | Version | Changes |
|---|---|---|
| August 2014 | 2014.08.18 | • Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.<br>• Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.<br>• Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.<br>• Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.<br>• Added variable precision DSP blocks support for floating-point arithmetic. |
| June 2014 | 2014.06.19 | Updated number of dedicated I/Os in the HPS block to 17. |
| February 2014 | 2014.02.21 | Updated transceiver speed grade options for GT devices in Figure 2. |
| February 2014 | 2014.02.06 | Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps. |
| December 2013 | 2013.12.10 | • Updated the HPS memory standards support from LPDDR2 to LPDDR3.<br>• Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks . |
| December 2013 | 2013.12.02 | Initial release. |