# Intel - 10AS048H4F34I3LG Datasheet

**Welcome to E-XFL.COM**

## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| **Details** | |
|---|---|
| Product Status | Active |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 480K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as048h4f34i3lg |

# Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

### Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

| Market | Applications |
|---|---|
| Wireless | • Channel and switch cards in remote radio heads<br>• Mobile backhaul |
| Wireline | • 40G/100G muxponders and transponders<br>• 100G line cards<br>• Bridging<br>• Aggregation |
| Broadcast | • Studio switches<br>• Servers and transport<br>• Videoconferencing<br>• Professional audio and video |
| Computing and Storage | • Flash cache<br>• Cloud computing servers<br>• Server acceleration |
| Medical | • Diagnostic scanners<br>• Diagnostic imaging |
| Military | • Missile guidance and control<br>• Radar<br>• Electronic warfare<br>• Secure communications |

### Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.

---

| Feature | Description | |
|---|---|---|
| Low-power serial transceivers | • Continuous operating range:<br>— Intel Arria 10 GX—1 Gbps to 17.4 Gbps<br>— Intel Arria 10 GT—1 Gbps to 25.8 Gbps<br>• Backplane support:<br>— Intel Arria 10 GX—up to 12.5<br>— Intel Arria 10 GT—up to 12.5<br>• Extended range down to 125 Mbps with oversampling<br>• ATX transmit PLLs with user-configurable fractional synthesis capability<br>• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module<br>• Adaptive linear and decision feedback equalization<br>• Transmitter pre-emphasis and de-emphasis<br>• Dynamic partial reconfiguration of individual transceiver channels | |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system | • Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability<br>• 256 KB on-chip RAM and 64 KB on-chip ROM<br>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers<br>• Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)<br>• ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage |
| | External interfaces | • Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller<br>• Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-GO (OTG) controllers, I$^2$C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os) |
| | Interconnects to core | • High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write<br>• HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa<br>• Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port<br>• FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller |
| Configuration | • Tamper protection—comprehensive design protection to protect your valuable IP investments<br>• Enhanced 256-bit advanced encryption standard (AES) design security with authentication<br>• Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3 | |

***continued...***

---

(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

| Feature | Description |
|---|---|
| | • Dynamic reconfiguration of the transceivers and PLLs<br>• Fine-grained partial reconfiguration of the core fabric<br>• Active Serial x4 Interface |
| Power management | • SmartVID<br>• Low static power device options<br>• Programmable Power Technology<br>• Intel Quartus Prime integrated power analysis |
| Software and tools | • Intel Quartus Prime design suite<br>• Transceiver toolkit<br>• Platform Designer system integration tool<br>• DSP Builder for Intel FPGAs<br>• OpenCL™ support<br>• Intel SoC FPGA Embedded Design Suite (EDS) |

### Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

### Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|---|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring:<br>• 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.<br>• 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

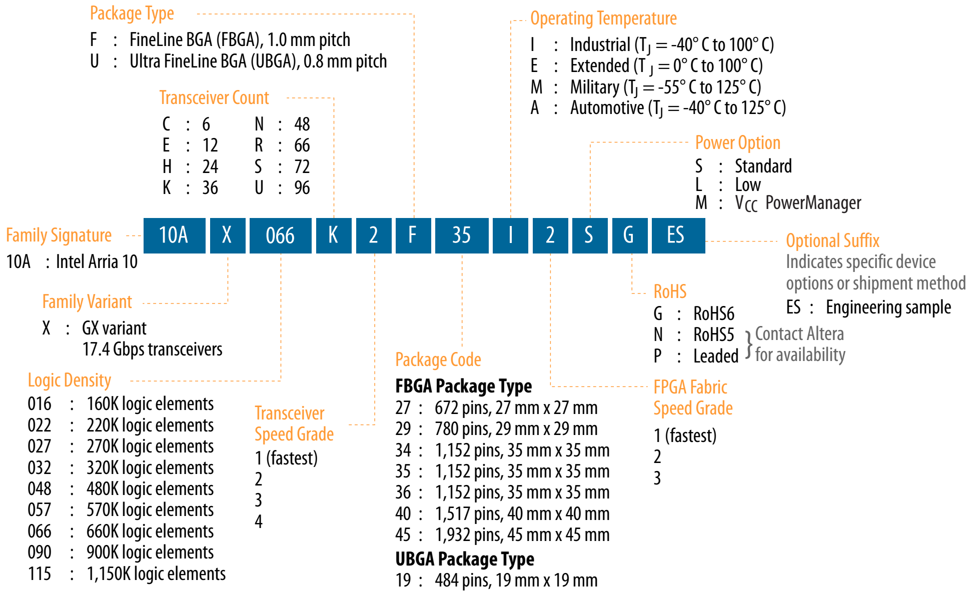
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Available Options

### Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.

### Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|---|---|---|---|---|---|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO (3) | | 696 | 696 | 768 | 768 |
| LVDS Pair (4) | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

## Package Plan

### Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

## Maximum Resources

### Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

| Resource | | Product Line | |
|---|---|---|---|
| | | GT 900 | GT 1150 |
| Logic Elements (LE) (K) | | 900 | 1,150 |
| ALM | | 339,620 | 427,200 |
| Register | | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 48,460 | 54,260 |
| | MLAB | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 32 | 32 |
| | I/O | 16 | 16 |
| Transceiver | 17.4 Gbps | 72 (5) | 72 (5) |
| | 25.8 Gbps | 6 | 6 |
| GPIO(6) | | 624 | 624 |
| LVDS Pair(7) | | 312 | 312 |
| PCIe Hard IP Block | | 4 | 4 |
| Hard Memory Controller | | 16 | 16 |

#### Related Information

Intel Arria 10 GT Channel Usage
Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

### Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45 (45 mm × 45 mm, 1932-pin FBGA) | | |
|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR |
| GT 900 | — | 624 | 72 |
| GT 1150 | — | 624 | 72 |

---

(5) If all 6 GT channels are in use, 12 of the GX channels are not usable.

(6) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(7) Each LVDS I/O pair can be used as differential input or output.

| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---|---|---|---|---|---|---|
| | | | 18 x 19 Multiplier | 27 x 27 Multiplier | | |
| | SX 320 | 984 | 1,968 | 984 | 984 | 984 |
| | SX 480 | 1,368 | 2,736 | 1,368 | 1,368 | 1,368 |
| | SX 570 | 1,523 | 3,046 | 1,523 | 1,523 | 1,523 |
| | SX 660 | 1,687 | 3,374 | 1,687 | 1,687 | 1,687 |

### Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|---|---|---|---|---|---|---|
| Intel Arria 10 GX | GX 160 | 156 | 156 | 156 | 156 | 140 |
| | GX 220 | 192 | 192 | 192 | 192 | 173 |
| | GX 270 | 830 | 830 | 830 | 830 | 747 |
| | GX 320 | 984 | 984 | 984 | 984 | 886 |
| | GX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | GX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | GX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |
| | GX 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GX 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 GT | GT 900 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| | GT 1150 | 1,518 | 1,518 | 1,518 | 1,518 | 1,366 |
| Intel Arria 10 SX | SX 160 | 156 | 156 | 156 | 156 | 140 |
| | SX 220 | 192 | 192 | 192 | 192 | 173 |
| | SX 270 | 830 | 830 | 830 | 830 | 747 |
| | SX 320 | 984 | 984 | 984 | 984 | 886 |
| | SX 480 | 1,369 | 1,368 | 1,368 | 1,368 | 1,231 |
| | SX 570 | 1,523 | 1,523 | 1,523 | 1,523 | 1,371 |
| | SX 660 | 1,687 | 1,687 | 1,687 | 1,687 | 1,518 |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

### Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

| Variant | Product Line | M20K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Intel Arria 10 GX | GX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | GX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | GX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | GX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | GX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | GX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | GX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |
| | GX 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GX 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 GT | GT 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GT 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 SX | SX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | SX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | SX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | SX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | SX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | SX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | SX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |

**Related Information**

Intel Arria 10 Device Datasheet
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

**Related Information**

PCS Features on page 30

## Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

### Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

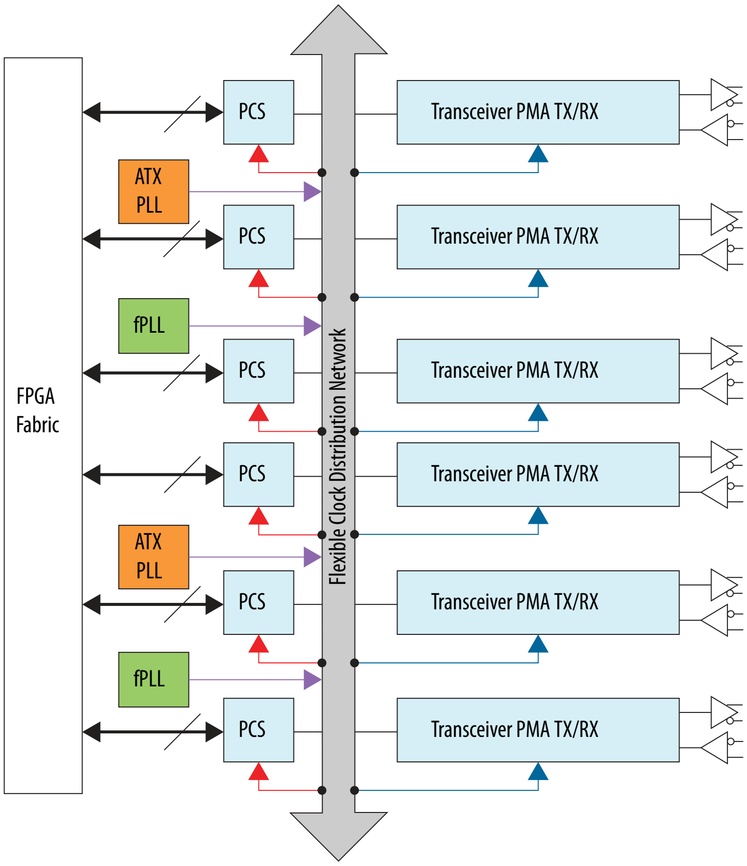
**Related Information**

PCS Features on page 30

### 10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

**Figure 6. Intel Arria 10 Transceiver Block Architecture**



## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.

Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

### Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices

| Feature | Capability |
|---|---|
| Chip-to-Chip Data Rates | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices) |
| Backplane Support | Drive backplanes at data rates up to 12.5 Gbps |
| Optical Module Support | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4 |
| Cable Driving Support | SFP+ Direct Attach, PCI Express over cable, eSATA |
| Transmit Pre-Emphasis | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss |
| Continuous Time Linear Equalizer (CTLE) | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss |
| Decision Feedback Equalizer (DFE) | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments |
| Variable Gain Amplifier | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes |
| Altera Digital Adaptive Parametric Tuning (ADAPT) | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance |
| Advanced Transmit (ATX) PLL | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols |
| Fractional PLLs | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost |
| Digitally Assisted Analog CDR | Superior jitter tolerance with fast lock time |
| Dynamic Partial Reconfiguration | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility |
| Multiple PCS-PMA and PCS-PLD interface widths | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

| PCS | Description |
|---|---|
| Standard PCS | • Operates at a data rate up to 12 Gbps<br>• Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS<br>• Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | • Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA<br>• Handles data transfer to and from the FPGA fabric<br>• Handles data transfer internally to and from the PMA<br>• Provides frequency compensation<br>• Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | • Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates<br>• Provides support for PIPE 3.0 features<br>• Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

### Related Information

- PCIe Gen1, Gen2, and Gen3 Hard IP on page 26
- Interlaken Support on page 26
- 10 Gbps Ethernet Support on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |

***continued...***

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143(12) to 2.97 | Native PHY | Standard PCS |

### Related Information

Intel Arria 10 Transceiver PHY User Guide

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

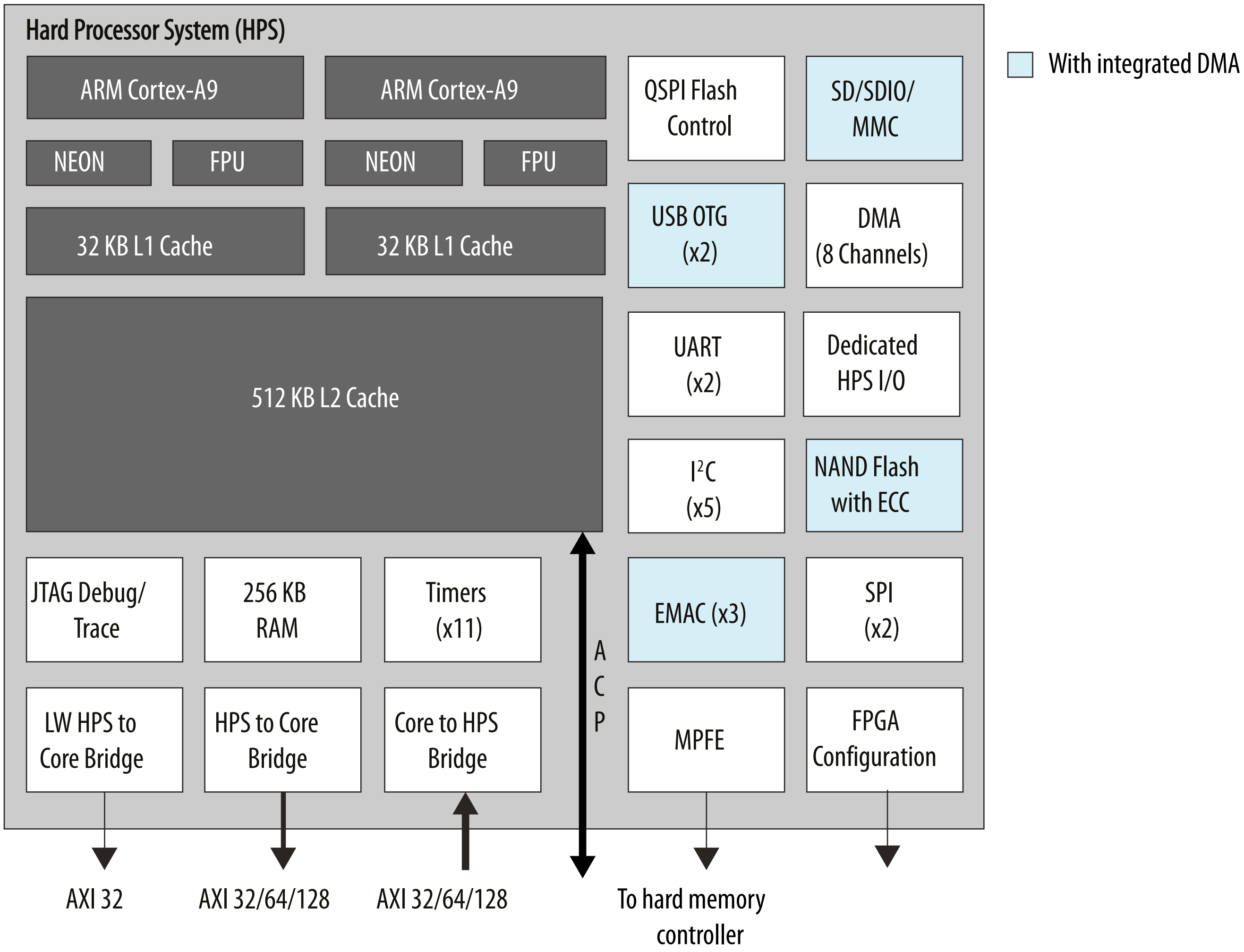
- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

---

(12) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

## Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:<br>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.<br>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.<br>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or $I^2C$ interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |

## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
    - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
    - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
    - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
    - 32 KB of L1 instruction cache, 32 KB of L1 data cache
    - Single- and double-precision floating-point unit and NEON media engine
    - CoreSight debug and trace technology
    - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I$^2$C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS–FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS–FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS–FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps)(13) | Decompression | Design Security(14) | Partial Reconfiguration(15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes(17) | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes(17) | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes(16) | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

---

(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

(14) Encryption and compression cannot be used simultaneously.

(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(17) Supported at a maximum clock rate of 100 MHz.

The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core $V_{CC}$ while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes |
|---|---|
| 2018.04.09 | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|---|---|---|
| January 2018 | 2018.01.17 | • Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.<br>• Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in *Memory Standards Supported by the Soft Memory Controller* table.<br>• Updated transceiver backplane capability to 12.5 Gbps.<br>• Removed transceiver speed grade 5 in *Sample Ordering Core and Available Options for Intel Arria 10 GX Devices* figure. |

**continued...**

| Date | Version | Changes |
|---|---|---|
| | | - Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from *Sample Ordering Core and Available Options for Intel Arria 10 GT Devices* figure.<br>- Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.<br>- Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from *PMA Features of the Transceivers in Intel Arria 10 Devices* table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | - Corrected protocol names with "1588" to "IEEE 1588v2".<br>- Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.<br>- Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | - Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.<br>- Rebranded as Intel. |
| October 2016 | 2016.10.31 | - Removed package F36 from Intel Arria 10 GX devices.<br>- Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | - Updated the FPGA Configuration and HPS Booting topic.<br>- Remove $V_{CC}$ PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.<br>- Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.<br>- Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | - Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.<br>- Revised the state for Core clock networks in the Summary of Features topic.<br>- Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.<br>- Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.<br>- Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.<br>- Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.<br>- Changed transceiver parameters in the "Low Power Serial Transceivers" section.<br>- Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.<br>- Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.<br>- Changed the datarates for GT devices in the "PMA Features" section.<br>- Changed the datarates for GT devices in the "PCS Features" section. |

***continued...***