Welcome to E-XFL.COM

Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

Embedded - System On Chip (SoC) refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

What are Embedded - System On Chip (SoC)?

System On Chip (SoC) integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

Details	
Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 570K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10as057k2f40i2lg

Key Advantages of Intel Arria 10 Devices

Table 2. Key Advantages of the Intel Arria 10 Device Family

Advantage	Supporting Feature
Enhanced core architecture	• Built on TSMC's 20 nm process technology • 60% higher performance than the previous generation of mid-range FPGAs • 15% higher performance than the fastest previous-generation FPGA
High-bandwidth integrated transceivers	• Short-reach rates up to 25.8 Gigabits per second (Gbps) • Backplane capability up to 12.5 Gbps • Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)
Improved logic integration and hard IP blocks	• 8-input adaptive logic module (ALM) • Up to 65.6 megabits (Mb) of embedded memory • Variable-precision digital signal processing (DSP) blocks • Fractional synthesis phase-locked loops (PLLs) • Hard PCI Express Gen3 IP blocks • Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	• Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC) • Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Advanced power savings	• Comprehensive set of advanced power saving features • Power-optimized MultiTrack routing and core architecture • Up to 40% lower power compared to previous generation of mid-range FPGAs • Up to 60% lower power compared to previous generation of high-end FPGAs

Summary of Intel Arria 10 Features

Table 3. Summary of Features for Intel Arria 10 Devices

Feature	Description
Technology	• TSMC's 20-nm SoC process technology • Allows operation at a lower V_{CC} level of 0.82 V instead of the 0.9 V standard V_{CC} core voltage
Packaging	• 1.0 mm ball-pitch Fineline BGA packaging • 0.8 mm ball-pitch Ultra Fineline BGA packaging • Multiple devices with identical package footprints for seamless migration between different FPGA densities • Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices • RoHS, leaded(1), and lead-free (Pb-free) options
High-performance FPGA fabric	• Enhanced 8-input ALM with four registers • Improved multi-track routing architecture to reduce congestion and improve compilation time • Hierarchical core clocking architecture • Fine-grained partial reconfiguration
Internal memory blocks	• M20K—20-Kb memory blocks with hard error correction code (ECC) • Memory logic array block (MLAB)—640-bit memory

continued...

(1) Contact Intel for availability.

Maximum Resources

Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

Resource	Product Line				
	GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)	160	220	270	320	480
ALM	61,510	80,330	101,620	119,900	183,590
Register	246,040				

The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History for Intel Arria 10 Device Overview

Document Version	Changes
2018.04.09	Updated the lowest V_{CC} from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps. • Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in *Memory Standards Supported by the Soft Memory Controller* table. • Updated transceiver backplane capability to 12.5 Gbps. • Removed transceiver speed grade 5 in *Sample Ordering Core and Available Options for Intel Arria 10 GX Devices* figure.

continued...

Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices

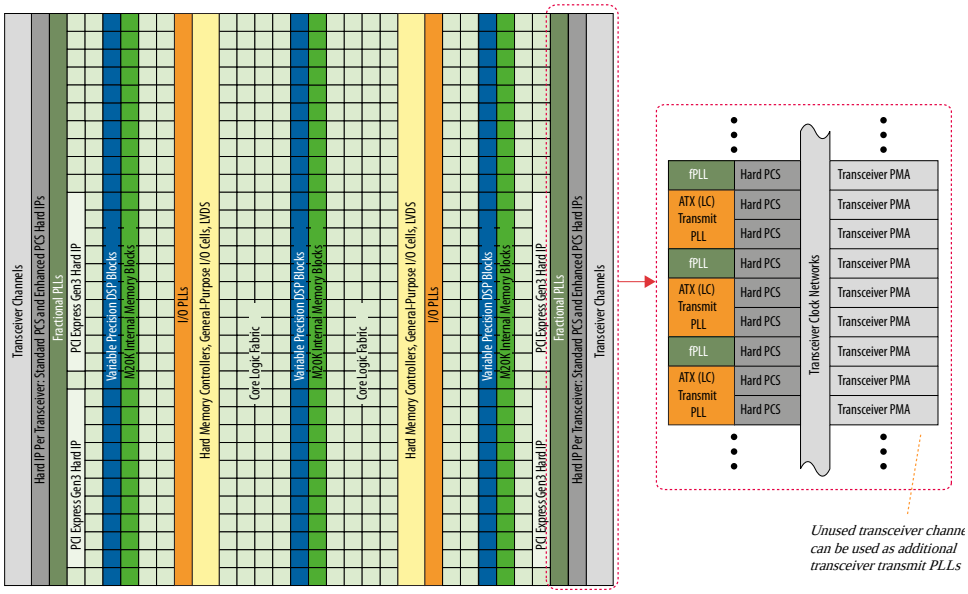
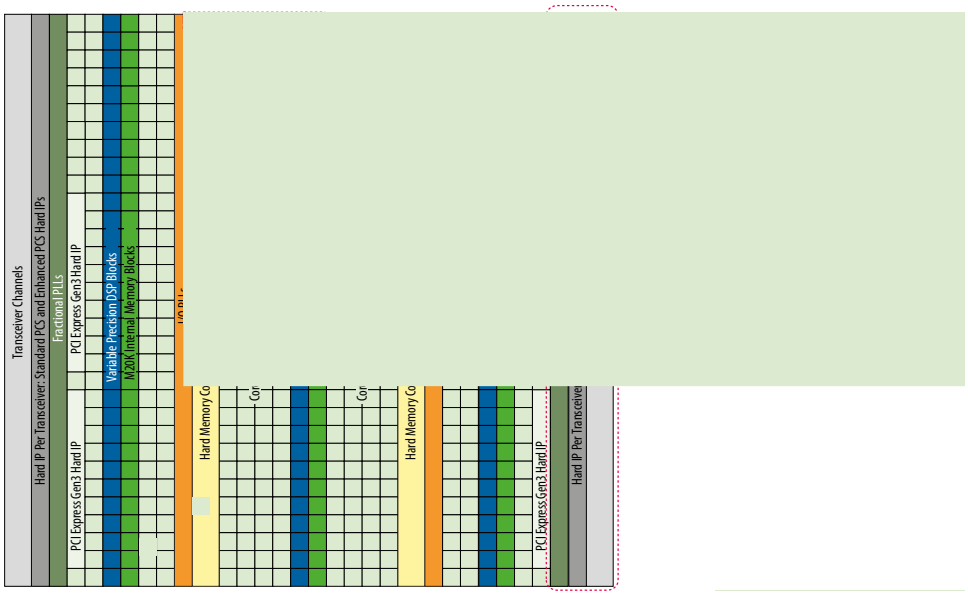
Figure 8. Device Chip Overview for Intel Arria 10 SX Devices