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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

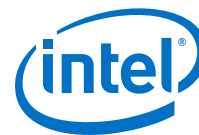
**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

|                         |   |
|-------------------------|---|
| Product Status          | Active  |
| Architecture            | MCU, FPGA   |
| Core Processor          | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™  |
| Flash Size              | -   |
| RAM Size                | 256KB   |
| Peripherals             | DMA, POR, WDT   |
| Connectivity            | EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG  |
| Speed                   | 1.5GHz  |
| Primary Attributes      | FPGA - 570K Logic Elements  |
| Operating Temperature   | 0°C ~ 100°C (TJ)  |
| Package / Case          | 1517-BBGA, FCBGA  |
| Supplier Device Package | 1517-FCBGA (40x40)  |
| Purchase URL            | <a href="https://www.e-xfl.com/product-detail/intel/10as057n2f40e1hg">https://www.e-xfl.com/product-detail/intel/10as057n2f40e1hg</a> |



## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market                | Applications  |
|-----------------------|---|
| Wireless              | <ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>   |
| Wireline              | <ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>            |
| Broadcast             | <ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul> |
| Computing and Storage | <ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>   |
| Medical               | <ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>   |
| Military              | <ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>          |

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Key Advantages of Intel Arria 10 Devices

**Table 2. Key Advantages of the Intel Arria 10 Device Family**

| Advantage  | Supporting Feature  |
|--|---|
| Enhanced core architecture   | <ul style="list-style-type: none"><li>Built on TSMC's 20 nm process technology</li><li>60% higher performance than the previous generation of mid-range FPGAs</li><li>15% higher performance than the fastest previous-generation FPGA</li></ul>  |
| High-bandwidth integrated transceivers   | <ul style="list-style-type: none"><li>Short-reach rates up to 25.8 Gigabits per second (Gbps)</li><li>Backplane capability up to 12.5 Gbps</li><li>Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)</li></ul>   |
| Improved logic integration and hard IP blocks  | <ul style="list-style-type: none"><li>8-input adaptive logic module (ALM)</li><li>Up to 65.6 megabits (Mb) of embedded memory</li><li>Variable-precision digital signal processing (DSP) blocks</li><li>Fractional synthesis phase-locked loops (PLLs)</li><li>Hard PCI Express Gen3 IP blocks</li><li>Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)</li></ul> |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | <ul style="list-style-type: none"><li>Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)</li><li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li></ul>  |
| Advanced power savings   | <ul style="list-style-type: none"><li>Comprehensive set of advanced power saving features</li><li>Power-optimized MultiTrack routing and core architecture</li><li>Up to 40% lower power compared to previous generation of mid-range FPGAs</li><li>Up to 60% lower power compared to previous generation of high-end FPGAs</li></ul>   |

## Summary of Intel Arria 10 Features

**Table 3. Summary of Features for Intel Arria 10 Devices**

| Feature                      | Description   |
|------------------------------|---|
| Technology                   | <ul style="list-style-type: none"><li>TSMC's 20-nm SoC process technology</li><li>Allows operation at a lower <math>V_{CC}</math> level of 0.82 V instead of the 0.9 V standard <math>V_{CC}</math> core voltage</li></ul>  |
| Packaging                    | <ul style="list-style-type: none"><li>1.0 mm ball-pitch FINELINE BGA packaging</li><li>0.8 mm ball-pitch Ultra FINELINE BGA packaging</li><li>Multiple devices with identical package footprints for seamless migration between different FPGA densities</li><li>Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices</li><li>RoHS, leaded<sup>(1)</sup>, and lead-free (Pb-free) options</li></ul> |
| High-performance FPGA fabric | <ul style="list-style-type: none"><li>Enhanced 8-input ALM with four registers</li><li>Improved multi-track routing architecture to reduce congestion and improve compilation time</li><li>Hierarchical core clocking architecture</li><li>Fine-grained partial reconfiguration</li></ul>   |
| Internal memory blocks       | <ul style="list-style-type: none"><li>M20K—20-Kb memory blocks with hard error correction code (ECC)</li><li>Memory logic array block (MLAB)—640-bit memory</li></ul>   |
| continued...                 |   |

(1) Contact Intel for availability.

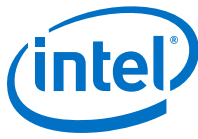


| Feature                           | Description  |   |
|-----------------------------------|--|---|
| Embedded Hard IP blocks           | Variable-precision DSP   | <ul style="list-style-type: none"><li>Native support for signal processing precision levels from 18 x 19 to 54 x 54</li><li>Native support for 27 x 27 multiplier mode</li><li>64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li><li>Internal coefficient memory banks</li><li>Padder/subtractor for improved efficiency</li><li>Additional pipeline register to increase performance and reduce power</li><li>Supports floating point arithmetic:<ul style="list-style-type: none"><li>Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.</li><li>Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.</li><li>Dynamic accumulator reset control.</li><li>Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.</li></ul></li></ul> |
|                                   | Memory controller  | DDR4, DDR3, and DDR3L   |
|                                   | PCI Express*   | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port   |
|                                   | Transceiver I/O  | <ul style="list-style-type: none"><li>10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>PCS hard IPs that support:<ul style="list-style-type: none"><li>10-Gbps Ethernet (10GbE)</li><li>PCIe PIPE interface</li><li>Interlaken</li><li>Gbps Ethernet (GbE)</li><li>Common Public Radio Interface (CPRI) with deterministic latency support</li><li>Gigabit-capable passive optical network (GPON) with fast lock-time support</li></ul></li><li>13.5G JESD204b</li><li>8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>Custom mode support for proprietary protocols</li></ul>  |
| Core clock networks               | <ul style="list-style-type: none"><li>Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none"><li>667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface</li><li>800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface</li></ul></li><li>Global, regional, and peripheral clock networks</li><li>Clock networks that are not used can be gated to reduce dynamic power</li></ul>   |   |
| Phase-locked loops (PLLs)         | <ul style="list-style-type: none"><li>High-resolution fractional synthesis PLLs:<ul style="list-style-type: none"><li>Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li><li>Support integer mode and fractional mode</li><li>Fractional mode support with third-order delta-sigma modulation</li></ul></li><li>Integer PLLs:<ul style="list-style-type: none"><li>Adjacent to general purpose I/Os</li><li>Support external memory and LVDS interfaces</li></ul></li></ul> |   |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none"><li>1.6 Gbps LVDS—every pair can be configured as receiver or transmitter</li><li>On-chip termination (OCT)</li><li>1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing</li></ul>  |   |
| External Memory Interface         | <ul style="list-style-type: none"><li>Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none"><li>DDR4—speeds up to 1,200 MHz/2,400 Mbps</li><li>DDR3—speeds up to 1,067 MHz/2,133 Mbps</li></ul></li><li>Soft memory controller—provides support for RLDRAM 3<sup>(2)</sup>, QDR IV<sup>(2)</sup>, and QDR II+</li></ul>  |   |
| continued...                      |  |   |



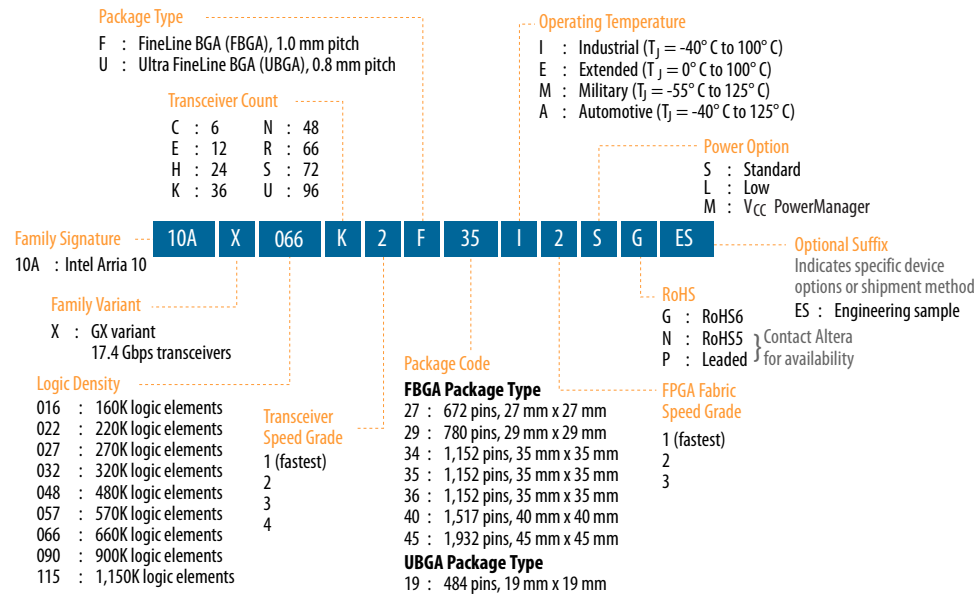
| Feature                                 | Description   |  |
|---|---|--|
| Low-power serial transceivers           | <ul style="list-style-type: none"><li>• Continuous operating range:<ul style="list-style-type: none"><li>— Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>— Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>• Backplane support:<ul style="list-style-type: none"><li>— Intel Arria 10 GX—up to 12.5</li><li>— Intel Arria 10 GT—up to 12.5</li></ul></li><li>• Extended range down to 125 Mbps with oversampling</li><li>• ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>• Adaptive linear and decision feedback equalization</li><li>• Transmitter pre-emphasis and de-emphasis</li><li>• Dynamic partial reconfiguration of individual transceiver channels</li></ul> |  |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system  | <ul style="list-style-type: none"><li>• Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>• 256 KB on-chip RAM and 64 KB on-chip ROM</li><li>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>• Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>• ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>   |
|   | External interfaces   | <ul style="list-style-type: none"><li>• Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>• Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>   |
|   | Interconnects to core   | <ul style="list-style-type: none"><li>• High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>• HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>• Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>• FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul> |
| Configuration                           | <ul style="list-style-type: none"><li>• Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>• Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>• Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>   |  |
| continued...                            |   |  |

<sup>(2)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

| Resource                     |                      | Product Line |         |         |         |         |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
|                              |                      | GX 160       | GX 220  | GX 270  | GX 320  | GX 480  |
| Logic Elements (LE) (K)      |                      | 160          | 220     | 270     | 320     | 480     |
| ALM                          |                      | 61,510       | 80,330  | 101,620 | 119,900 | 183,590 |
| Register                     |                      | 246,040      | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb)                  | M20K                 | 8,800        | 11,740  | 15,000  | 17,820  | 28,620  |
|                              | MLAB                 | 1,050        | 1,690   | 2,452   | 2,727   | 4,164   |
| Variable-precision DSP Block |                      | 156          | 192     | 830     | 985     | 1,368   |
| 18 x 19 Multiplier           |                      | 312          | 384     | 1,660   | 1,970   | 2,736   |
| PLL                          | Fractional Synthesis | 6            | 6       | 8       | 8       | 12      |
|                              | I/O                  | 6            | 6       | 8       | 8       | 12      |
| 17.4 Gbps Transceiver        |                      | 12           | 12      | 24      | 24      | 36      |
| GPIO <sup>(3)</sup>          |                      | 288          | 288     | 384     | 384     | 492     |
| LVDS Pair <sup>(4)</sup>     |                      | 120          | 120     | 168     | 168     | 222     |
| PCIe Hard IP Block           |                      | 1            | 1       | 2       | 2       | 2       |
| Hard Memory Controller       |                      | 6            | 6       | 8       | 8       | 12      |

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.



## Maximum Resources

**Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices**

| Resource                     |                      | Product Line      |                   |
|------------------------------|----------------------|-------------------|-------------------|
|                              |                      | GT 900            | GT 1150           |
| Logic Elements (LE) (K)      |                      | 900               | 1,150             |
| ALM                          |                      | 339,620           | 427,200           |
| Register                     |                      | 1,358,480         | 1,708,800         |
| Memory (Kb)                  | M20K                 | 48,460            | 54,260            |
|                              | MLAB                 | 9,386             | 12,984            |
| Variable-precision DSP Block |                      | 1,518             | 1,518             |
| 18 x 19 Multiplier           |                      | 3,036             | 3,036             |
| PLL                          | Fractional Synthesis | 32                | 32                |
|                              | I/O                  | 16                | 16                |
| Transceiver                  | 17.4 Gbps            | 72 <sup>(5)</sup> | 72 <sup>(5)</sup> |
|                              | 25.8 Gbps            | 6                 | 6                 |
| GPIO <sup>(6)</sup>          |                      | 624               | 624               |
| LVDS Pair <sup>(7)</sup>     |                      | 312               | 312               |
| PCIe Hard IP Block           |                      | 4                 | 4                 |
| Hard Memory Controller       |                      | 16                | 16                |

### Related Information

#### Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

**Table 11. Package Plan for Intel Arria 10 GT Devices**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

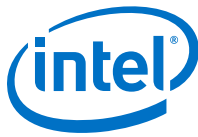
| Product Line | SF45<br>(45 mm x 45 mm, 1932-pin FBGA) |          |      |
|--------------|--|----------|------|
|              | 3 V I/O                                | LVDS I/O | XCVR |
| GT 900       | —                                      | 624      | 72   |
| GT 1150      | —                                      | 624      | 72   |

<sup>(5)</sup> If all 6 GT channels are in use, 12 of the GX channels are not usable.

<sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(7)</sup> Each LVDS I/O pair can be used as differential input or output.





### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

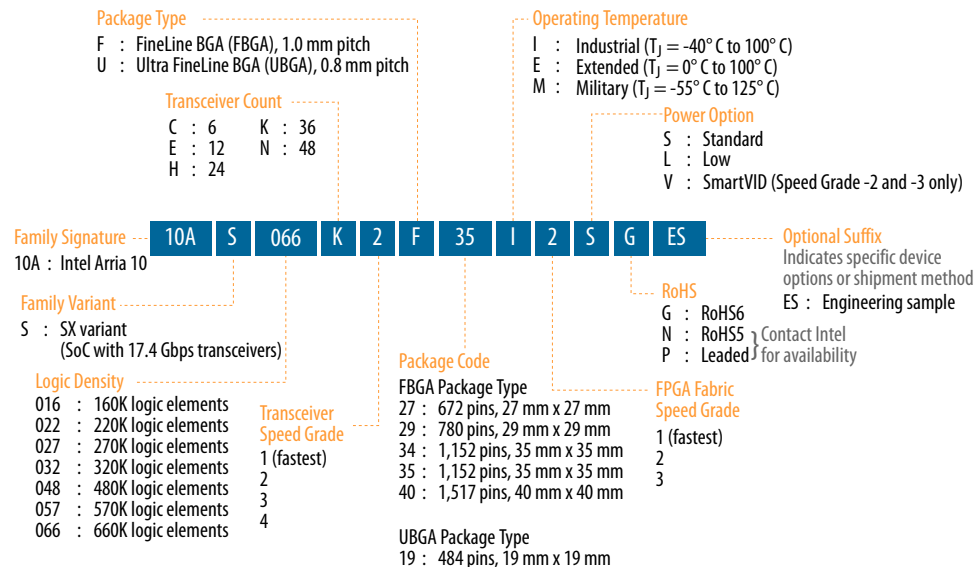
### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Available Options

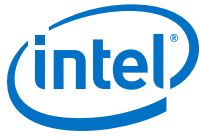
**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 480       | —                                       | —           | —    | —                                       | —           | —    | 48                                      | 312         | 12   | 48                                       | 444         | 24   |
| SX 570       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |
| SX 660       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

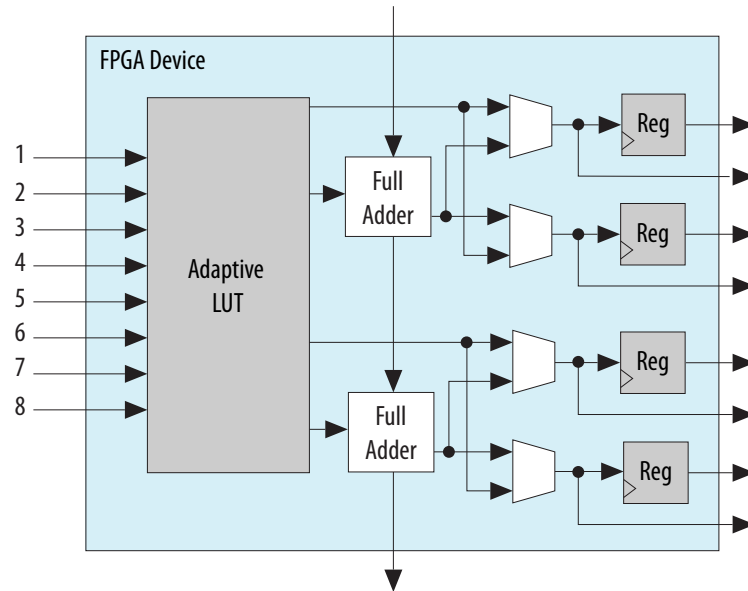
| Product Line | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |          |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      |
|--------------|--|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                  | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR |
| SX 270       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 320       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 480       | 48                                       | 348      | 36   | —   | —        | —    | —   | —        | —    |
| SX 570       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |
| SX 660       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

**Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices**

| Usage Example   | Multiplier Size (Bit)           | DSP Block Resources |
|---|---------------------------------|---------------------|
| Medium precision fixed point                            | Two 18 x 19                     | 1                   |
| High precision fixed or Single precision floating point | One 27 x 27                     | 1                   |
| Fixed point FFTs  | One 19 x 36 with external adder | 1                   |
| Very high precision fixed point                         | One 36 x 36 with external adder | 2                   |
| Double precision floating point                         | One 54 x 54 with external adder | 4                   |

**Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|-------------------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|                   |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
| Intel Arria 10 GX | GX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | GX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | GX 270       | 830                          | 1,660   | 830                | 830                               | 830   |
|                   | GX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|                   | GX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|                   | GX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|                   | GX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |
|                   | GX 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GX 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GT 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 SX | SX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | SX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | SX 270       | 830                          | 1,660   | 830                | 830                               | 830   |

*continued...*



## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

**Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices**

| Variant           | Product Line | M20K  |              | MLAB   |              | Total RAM Bit (Kb) |
|-------------------|--------------|-------|--------------|--------|--------------|--------------------|
|                   |              | Block | RAM Bit (Kb) | Block  | RAM Bit (Kb) |                    |
| Intel Arria 10 GX | GX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | GX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | GX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | GX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | GX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | GX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | GX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |
|                   | GX 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GX 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 GT | GT 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GT 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 SX | SX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | SX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | SX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | SX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | SX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | SX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | SX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits)       | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB         | 32                 | x16, x18, or x20   |
|              | 64 <sup>(10)</sup> | x8, x9, x10        |
| M20K         | 512                | x40, x32           |
|              | 1K                 | x20, x16           |
|              | 2K                 | x10, x8            |
|              | 4K                 | x5, x4             |
|              | 8K                 | x2                 |
|              | 16K                | x1                 |

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

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<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

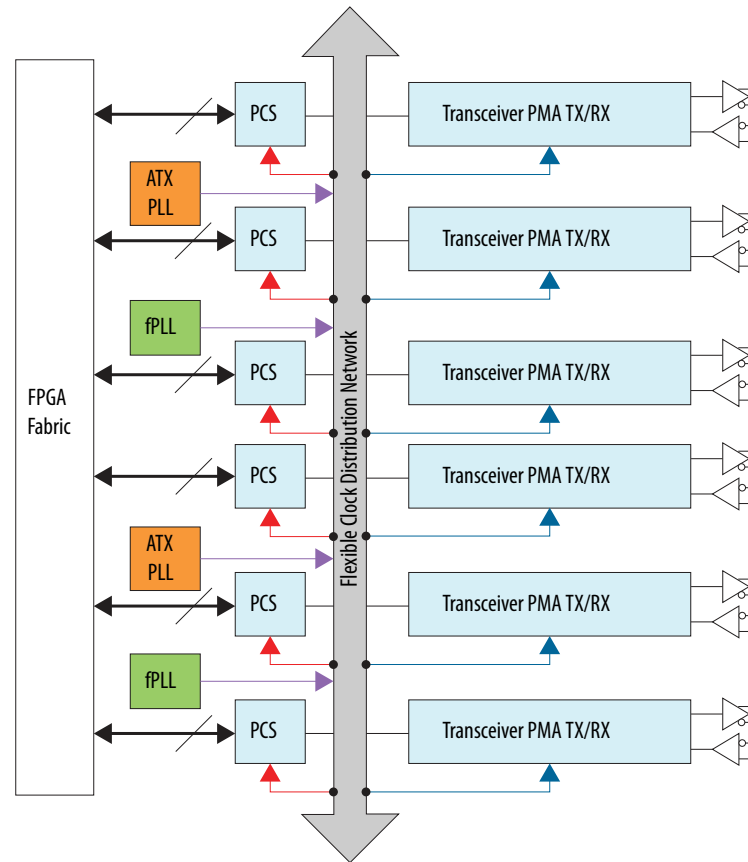
#### [External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

Figure 6. Intel Arria 10 Transceiver Block Architecture



## Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.





Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

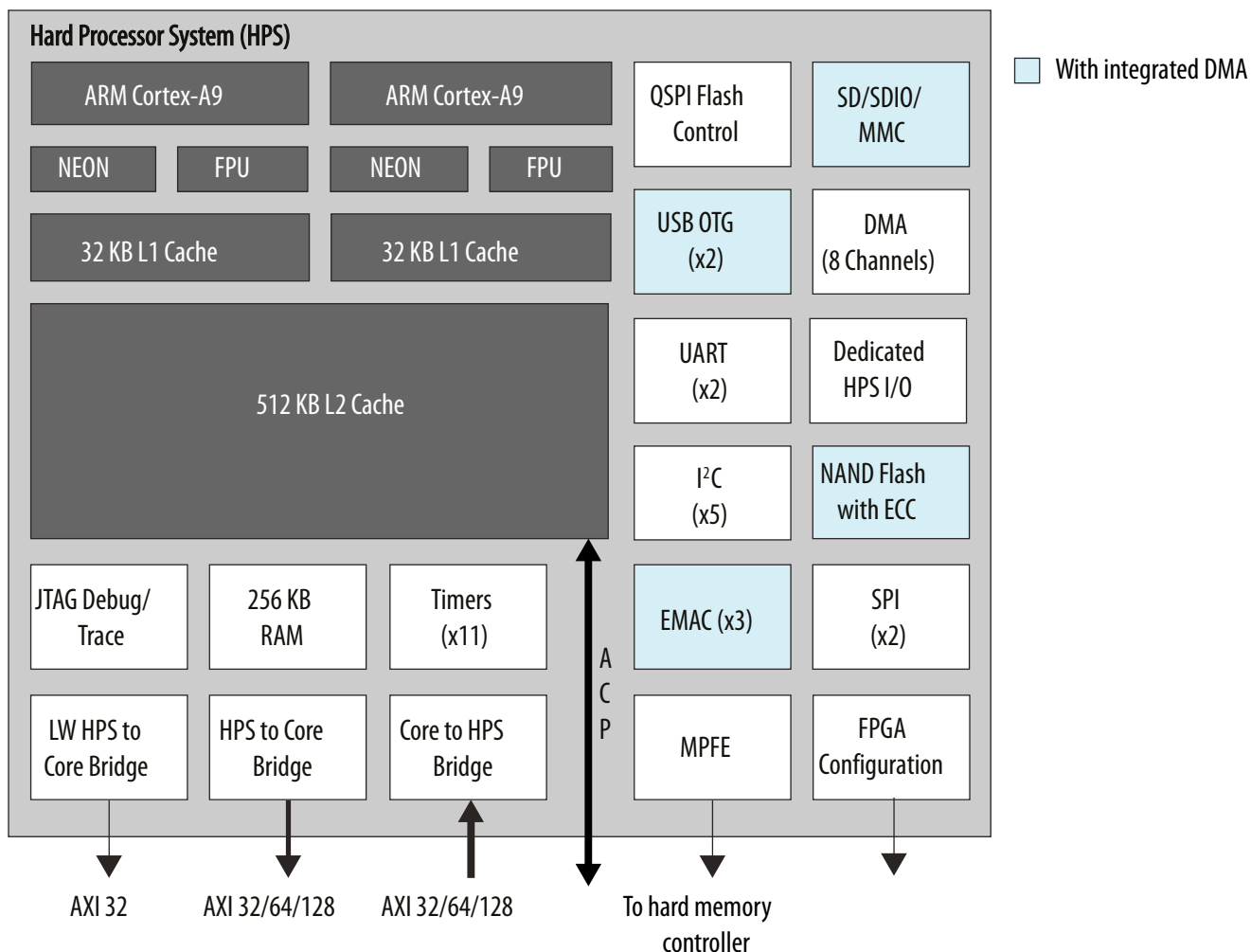
| Feature   | Capability   |
|---|--|
| Chip-to-Chip Data Rates                                 | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)   |
| Backplane Support                                       | Drive backplanes at data rates up to 12.5 Gbps   |
| Optical Module Support                                  | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4   |
| Cable Driving Support                                   | SFP+ Direct Attach, PCI Express over cable, eSATA  |
| Transmit Pre-Emphasis                                   | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss  |
| Continuous Time Linear Equalizer (CTLE)                 | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss  |
| Decision Feedback Equalizer (DFE)                       | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments  |
| Variable Gain Amplifier                                 | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes  |
| Altera Digital Adaptive Parametric Tuning (ADAPT)       | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance  |
| Advanced Transmit (ATX) PLL                             | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols   |
| Fractional PLLs   | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost   |
| Digitally Assisted Analog CDR                           | Superior jitter tolerance with fast lock time  |
| Dynamic Partial Reconfiguration                         | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility   |
| Multiple PCS-PMA and PCS-PLD interface widths           | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency  |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

**Table 25. Configuration Schemes and Features of Intel Arria 10 Devices**

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme   | Data Width    | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update                |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG   | 1 bit         | 33                   | 33                                   | —             | —                               | Yes <sup>(16)</sup>                     | —                                   |
| Active Serial (AS) through the EPCQ-L configuration device   | 1 bit, 4 bits | 100                  | 400                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Yes                                 |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit         | 100                  | 100                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Parallel Flash Loader (PFL) IP core |

*continued...*

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(16)</sup> Partial configuration can be performed only when it is configured as internal host.



| Date           | Version    | Changes  |
|----------------|------------|--|
|                |            | <ul style="list-style-type: none"> <li>Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure.</li> <li>Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.</li> <li>Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.</li> </ul>   |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.   |
| July 2017      | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".  |
| July 2017      | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family.  |
| May 2017       | 2017.05.08 | <ul style="list-style-type: none"> <li>Corrected protocol names with "1588" to "IEEE 1588v2".</li> <li>Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.</li> <li>Removed all "Preliminary" marks.</li> </ul>   |
| March 2017     | 2017.03.15 | <ul style="list-style-type: none"> <li>Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.</li> <li>Rebranded as Intel.</li> </ul>  |
| October 2016   | 2016.10.31 | <ul style="list-style-type: none"> <li>Removed package F36 from Intel Arria 10 GX devices.</li> <li>Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.</li> </ul>   |
| May 2016       | 2016.05.02 | <ul style="list-style-type: none"> <li>Updated the FPGA Configuration and HPS Booting topic.</li> <li>Remove V<sub>CC</sub> PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.</li> <li>Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.</li> <li>Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.</li> </ul>   |
| February 2016  | 2016.02.11 | <ul style="list-style-type: none"> <li>Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.</li> <li>Revised the state for Core clock networks in the Summary of Features topic.</li> <li>Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.</li> <li>Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.</li> <li>Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.</li> <li>Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.</li> <li>Changed transceiver parameters in the "Low Power Serial Transceivers" section.</li> <li>Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.</li> <li>Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.</li> <li>Changed the datarates for GT devices in the "PMA Features" section.</li> <li>Changed the datarates for GT devices in the "PCS Features" section.</li> </ul> |
| continued...   |            |  |