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### **Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems**

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

### **What are Embedded - System On Chip (SoC)?**

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

#### **Details**

Product Status	Active
Architecture	MCU, FPGA
Core Processor	Dual ARM® Cortex®-A9 MPCore™ with CoreSight™
Flash Size	-
RAM Size	256KB
Peripherals	DMA, POR, WDT
Connectivity	EBI/EMI, Ethernet, I <sup>2</sup> C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed	1.5GHz
Primary Attributes	FPGA - 660K Logic Elements
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA, FC (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/10as066h1f34i1hg">https://www.e-xfl.com/product-detail/intel/10as066h1f34i1hg</a>



## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

Market	Applications
Wireless	<ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>
Wireline	<ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>
Broadcast	<ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul>
Computing and Storage	<ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>
Medical	<ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>
Military	<ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Key Advantages of Intel Arria 10 Devices

**Table 2. Key Advantages of the Intel Arria 10 Device Family**

Advantage	Supporting Feature
Enhanced core architecture	<ul style="list-style-type: none"><li>Built on TSMC's 20 nm process technology</li><li>60% higher performance than the previous generation of mid-range FPGAs</li><li>15% higher performance than the fastest previous-generation FPGA</li></ul>
High-bandwidth integrated transceivers	<ul style="list-style-type: none"><li>Short-reach rates up to 25.8 Gigabits per second (Gbps)</li><li>Backplane capability up to 12.5 Gbps</li><li>Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)</li></ul>
Improved logic integration and hard IP blocks	<ul style="list-style-type: none"><li>8-input adaptive logic module (ALM)</li><li>Up to 65.6 megabits (Mb) of embedded memory</li><li>Variable-precision digital signal processing (DSP) blocks</li><li>Fractional synthesis phase-locked loops (PLLs)</li><li>Hard PCI Express Gen3 IP blocks</li><li>Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)</li></ul>
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	<ul style="list-style-type: none"><li>Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)</li><li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li></ul>
Advanced power savings	<ul style="list-style-type: none"><li>Comprehensive set of advanced power saving features</li><li>Power-optimized MultiTrack routing and core architecture</li><li>Up to 40% lower power compared to previous generation of mid-range FPGAs</li><li>Up to 60% lower power compared to previous generation of high-end FPGAs</li></ul>

## Summary of Intel Arria 10 Features

**Table 3. Summary of Features for Intel Arria 10 Devices**

Feature	Description
Technology	<ul style="list-style-type: none"><li>TSMC's 20-nm SoC process technology</li><li>Allows operation at a lower <math>V_{CC}</math> level of 0.82 V instead of the 0.9 V standard <math>V_{CC}</math> core voltage</li></ul>
Packaging	<ul style="list-style-type: none"><li>1.0 mm ball-pitch FINELINE BGA packaging</li><li>0.8 mm ball-pitch Ultra FINELINE BGA packaging</li><li>Multiple devices with identical package footprints for seamless migration between different FPGA densities</li><li>Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices</li><li>RoHS, leaded<sup>(1)</sup>, and lead-free (Pb-free) options</li></ul>
High-performance FPGA fabric	<ul style="list-style-type: none"><li>Enhanced 8-input ALM with four registers</li><li>Improved multi-track routing architecture to reduce congestion and improve compilation time</li><li>Hierarchical core clocking architecture</li><li>Fine-grained partial reconfiguration</li></ul>
Internal memory blocks	<ul style="list-style-type: none"><li>M20K—20-Kb memory blocks with hard error correction code (ECC)</li><li>Memory logic array block (MLAB)—640-bit memory</li></ul>
continued...	

(1) Contact Intel for availability.



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none"><li>Continuous operating range:<ul style="list-style-type: none"><li>Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>Backplane support:<ul style="list-style-type: none"><li>Intel Arria 10 GX—up to 12.5</li><li>Intel Arria 10 GT—up to 12.5</li></ul></li><li>Extended range down to 125 Mbps with oversampling</li><li>ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>Adaptive linear and decision feedback equalization</li><li>Transmitter pre-emphasis and de-emphasis</li><li>Dynamic partial reconfiguration of individual transceiver channels</li></ul>	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none"><li>Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>256 KB on-chip RAM and 64 KB on-chip ROM</li><li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>
	External interfaces	<ul style="list-style-type: none"><li>Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>
	Interconnects to core	<ul style="list-style-type: none"><li>High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul>
Configuration	<ul style="list-style-type: none"><li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>	
continued...		

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(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Feature	Description
	<ul style="list-style-type: none"> <li>Dynamic reconfiguration of the transceivers and PLLs</li> <li>Fine-grained partial reconfiguration of the core fabric</li> <li>Active Serial x4 Interface</li> </ul>
Power management	<ul style="list-style-type: none"> <li>SmartVID</li> <li>Low static power device options</li> <li>Programmable Power Technology</li> <li>Intel Quartus Prime integrated power analysis</li> </ul>
Software and tools	<ul style="list-style-type: none"> <li>Intel Quartus Prime design suite</li> <li>Transceiver toolkit</li> <li>Platform Designer system integration tool</li> <li>DSP Builder for Intel FPGAs</li> <li>OpenCL™ support</li> <li>Intel SoC FPGA Embedded Design Suite (EDS)</li> </ul>

### Related Information

#### [Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: <ul style="list-style-type: none"> <li>17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.</li> <li>25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.</li> </ul>
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

### Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

#### [Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F34 (35 mm × 35 mm, 1152-pin FBGA)			F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 270	48	336	24	48	336	24	—	—	—	—	—	—
GX 320	48	336	24	48	336	24	—	—	—	—	—	—
GX 480	48	444	24	48	348	36	—	—	—	—	—	—
GX 570	48	444	24	48	348	36	96	600	36	48	540	48
GX 660	48	444	24	48	348	36	96	600	36	48	540	48
GX 900	—	504	24	—	—	—	—	—	—	—	600	48
GX 1150	—	504	24	—	—	—	—	—	—	—	600	48

**Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	RF40 (40 mm × 40 mm, 1517-pin FBGA)			NF45 (45 mm × 45 mm) 1932-pin FBGA)			SF45 (45 mm × 45 mm) 1932-pin FBGA)			UF45 (45 mm × 45 mm) 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 900	—	342	66	—	768	48	—	624	72	—	480	96
GX 1150	—	342	66	—	768	48	—	624	72	—	480	96

### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 <sup>(10)</sup>	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

## I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis



- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

#### [External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,200
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933
LPDDR3 SDRAM	Half rate	—	533
	Quarter rate	—	800

**Table 21. Memory Standards Supported by the Soft Memory Controller**

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 <sup>(11)</sup>	Quarter rate	1,200
QDR IV SRAM <sup>(11)</sup>	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

**Table 22. Memory Standards Supported by the HPS Hard Memory Controller**

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

<sup>(11)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



### **Related Information**

#### [Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## **PCIe Gen1, Gen2, and Gen3 Hard IP**

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

### **Related Information**

[PCS Features](#) on page 30

## **Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet**

### **Interlaken Support**

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

### **Related Information**

[PCS Features](#) on page 30

### **10 Gbps Ethernet Support**

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.



Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices



Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.



Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices) 1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 12.5 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.



**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul>
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).





## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) <sup>(13)</sup>	Decompression	Design Security <sup>(14)</sup>	Partial Reconfiguration <sup>(15)</sup>	Remote System Update
Fast passive parallel (FPP) through CPLD or external microcontroller	8 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	PFL IP core
	16 bits			Yes	Yes		
	32 bits			Yes	Yes		
Configuration via HPS	16 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	—
	32 bits			Yes	Yes		
Configuration via Protocol [CvP (PCIe*)]	x1, x2, x4, x8 lanes	—	8000	Yes	Yes	Yes <sup>(16)</sup>	—

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(17)</sup> Supported at a maximum clock rate of 100 MHz.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core  $V_{CC}$  while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

Document Version	Changes
2018.04.09	Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	<ul style="list-style-type: none"><li>• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li><li>• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.</li><li>• Updated transceiver backplane capability to 12.5 Gbps.</li><li>• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.</li></ul>
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Date	Version	Changes
		<ul style="list-style-type: none"> <li>Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure.</li> <li>Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.</li> <li>Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.</li> </ul>
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>Corrected protocol names with "1588" to "IEEE 1588v2".</li> <li>Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.</li> <li>Removed all "Preliminary" marks.</li> </ul>
March 2017	2017.03.15	<ul style="list-style-type: none"> <li>Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.</li> <li>Rebranded as Intel.</li> </ul>
October 2016	2016.10.31	<ul style="list-style-type: none"> <li>Removed package F36 from Intel Arria 10 GX devices.</li> <li>Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.</li> </ul>
May 2016	2016.05.02	<ul style="list-style-type: none"> <li>Updated the FPGA Configuration and HPS Booting topic.</li> <li>Remove V<sub>CC</sub> PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.</li> <li>Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.</li> <li>Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.</li> </ul>
February 2016	2016.02.11	<ul style="list-style-type: none"> <li>Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.</li> <li>Revised the state for Core clock networks in the Summary of Features topic.</li> <li>Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.</li> <li>Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.</li> <li>Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.</li> <li>Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.</li> <li>Changed transceiver parameters in the "Low Power Serial Transceivers" section.</li> <li>Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.</li> <li>Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.</li> <li>Changed the datarates for GT devices in the "PMA Features" section.</li> <li>Changed the datarates for GT devices in the "PCS Features" section.</li> </ul>
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