# Intel - 10AS066K3F35I2SGES Datasheet

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## Embedded - System On Chip (SoC): The Heart of Modern Embedded Systems

**Embedded - System On Chip (SoC)** refers to an integrated circuit that consolidates all the essential components of a computer system into a single chip. This includes a microprocessor, memory, and other peripherals, all packed into one compact and efficient package. SoCs are designed to provide a complete computing solution, optimizing both space and power consumption, making them ideal for a wide range of embedded applications.

## What are Embedded - System On Chip (SoC)?

**System On Chip (SoC)** integrates multiple functions of a computer or electronic system onto a single chip. Unlike traditional multi-chip solutions, SoCs combine a central

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Architecture | MCU, FPGA |
| Core Processor | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size | - |
| RAM Size | 256KB |
| Peripherals | DMA, POR, WDT |
| Connectivity | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed | 1.5GHz |
| Primary Attributes | FPGA - 660K Logic Elements |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FBGA, FC (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10as066k3f35i2sges |

# Key Advantages of Intel Arria 10 Devices

## Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|---|---|
| Enhanced core architecture | • Built on TSMC's 20 nm process technology<br>• 60% higher performance than the previous generation of mid-range FPGAs<br>• 15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | • Short-reach rates up to 25.8 Gigabits per second (Gbps)<br>• Backplane capability up to 12.5 Gbps<br>• Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | • 8-input adaptive logic module (ALM)<br>• Up to 65.6 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks<br>• Fractional synthesis phase-locked loops (PLLs)<br>• Hard PCI Express Gen3 IP blocks<br>• Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | • Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | • Comprehensive set of advanced power saving features<br>• Power-optimized MultiTrack routing and core architecture<br>• Up to 40% lower power compared to previous generation of mid-range FPGAs<br>• Up to 60% lower power compared to previous generation of high-end FPGAs |

# Summary of Intel Arria 10 Features

## Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|---|---|
| Technology | • TSMC's 20-nm SoC process technology<br>• Allows operation at a lower $V_{CC}$ level of 0.82 V instead of the 0.9 V standard $V_{CC}$ core voltage |
| Packaging | • 1.0 mm ball-pitch Fineline BGA packaging<br>• 0.8 mm ball-pitch Ultra Fineline BGA packaging<br>• Multiple devices with identical package footprints for seamless migration between different FPGA densities<br>• Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices<br>• RoHS, leaded(1), and lead-free (Pb-free) options |
| High-performance FPGA fabric | • Enhanced 8-input ALM with four registers<br>• Improved multi-track routing architecture to reduce congestion and improve compilation time<br>• Hierarchical core clocking architecture<br>• Fine-grained partial reconfiguration |
| Internal memory blocks | • M20K—20-Kb memory blocks with hard error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit memory |

***continued...***

(1) Contact Intel for availability.

| Feature | Description | |
|---|---|---|
| Low-power serial transceivers | • Continuous operating range:<br>— Intel Arria 10 GX—1 Gbps to 17.4 Gbps<br>— Intel Arria 10 GT—1 Gbps to 25.8 Gbps<br>• Backplane support:<br>— Intel Arria 10 GX—up to 12.5<br>— Intel Arria 10 GT—up to 12.5<br>• Extended range down to 125 Mbps with oversampling<br>• ATX transmit PLLs with user-configurable fractional synthesis capability<br>• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module<br>• Adaptive linear and decision feedback equalization<br>• Transmitter pre-emphasis and de-emphasis<br>• Dynamic partial reconfiguration of individual transceiver channels | |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system | • Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability<br>• 256 KB on-chip RAM and 64 KB on-chip ROM<br>• System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers<br>• Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)<br>• ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage |
| | External interfaces | • Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller<br>• Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-GO (OTG) controllers, $I^2C$ controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os) |
| | Interconnects to core | • High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write<br>• HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa<br>• Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port<br>• FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller |
| Configuration | • Tamper protection—comprehensive design protection to protect your valuable IP investments<br>• Enhanced 256-bit advanced encryption standard (AES) design security with authentication<br>• Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3 | |

***continued...***

(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

| Feature | Description |
|---|---|
| | • Dynamic reconfiguration of the transceivers and PLLs<br>• Fine-grained partial reconfiguration of the core fabric<br>• Active Serial x4 Interface |
| Power management | • SmartVID<br>• Low static power device options<br>• Programmable Power Technology<br>• Intel Quartus Prime integrated power analysis |
| Software and tools | • Intel Quartus Prime design suite<br>• Transceiver toolkit<br>• Platform Designer system integration tool<br>• DSP Builder for Intel FPGAs<br>• OpenCL™ support<br>• Intel SoC FPGA Embedded Design Suite (EDS) |

### Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

### Table 4. Device Variants for the Intel Arria 10 Device Family

| Variant | Description |
|---|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring:<br>• 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.<br>• 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Maximum Resources

### Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|---|---|---|---|---|---|---|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO (3) | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair (4) | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

(3) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(4) Each LVDS I/O pair can be used as differential input or output.

### Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

### Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

#### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

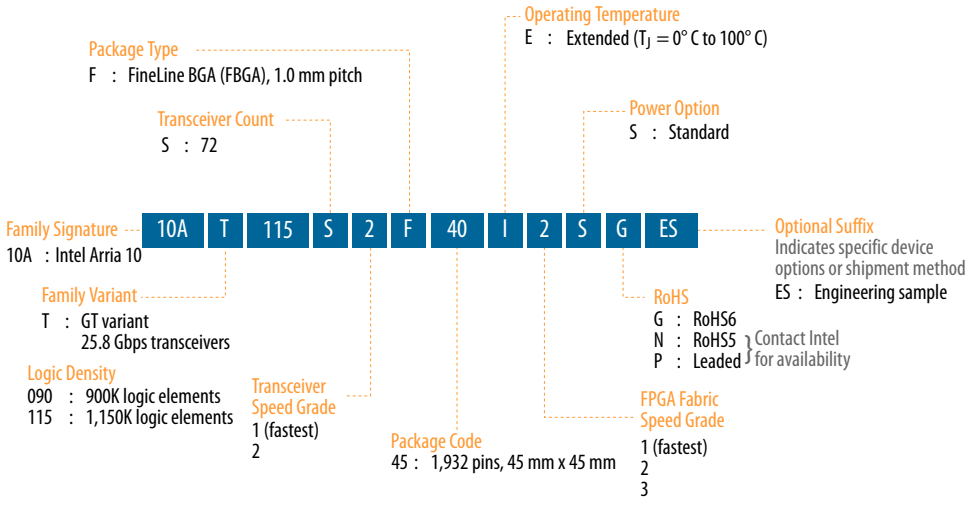
#### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Available Options

### Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices



### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook
Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

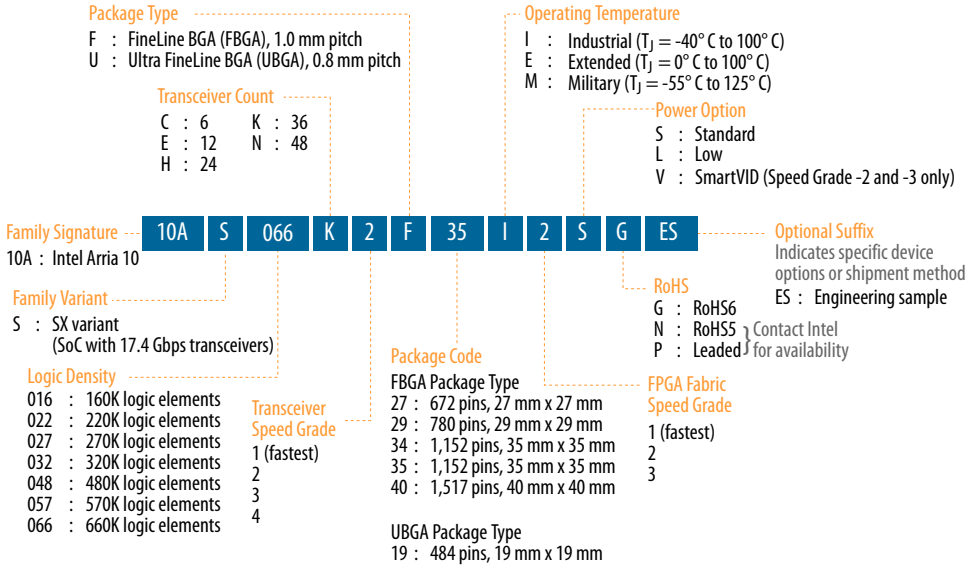
The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**




### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices
Provides more information about the transceiver speed grade.

## Maximum Resources

### Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

| Resource | | Product Line | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | SX 160 | SX 220 | SX 270 | SX 320 | SX 480 | SX 570 | SX 660 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 | 570 | 660 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 | 217,080 | 251,680 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 | 36,000 | 42,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 | 5,096 | 5,788 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 | 1,523 | 1,687 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 | 3,046 | 3,374 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| | I/O | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 | 48 | 48 |
| GPIO (8) | | 288 | 288 | 384 | 384 | 492 | 696 | 696 |
| LVDS Pair (9) | | 120 | 120 | 168 | 168 | 174 | 324 | 324 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 | 16 | 16 |
| ARM Cortex-A9 MPCore Processor | | Yes | Yes | Yes | Yes | Yes | Yes | Yes |

## Package Plan

### Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 160 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 220 | 48 | 144 | 6 | 48 | 192 | 12 | 48 | 240 | 12 | — | — | — |
| SX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |
| SX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 | 48 | 336 | 24 |

*continued...*

(8) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(9) Each LVDS I/O pair can be used as differential input or output.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 480 | — | — | — | — | — | — | 48 | 312 | 12 | 48 | 444 | 24 |
| SX 570 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |
| SX 660 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |

## Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 270 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 320 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 480 | 48 | 348 | 36 | — | — | — | — | — | — |
| SX 570 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| SX 660 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |

### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

### Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

| Variant | Product Line | M20K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Intel Arria 10 GX | GX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | GX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | GX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | GX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | GX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | GX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | GX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |
| | GX 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GX 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 GT | GT 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GT 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 SX | SX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | SX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | SX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | SX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | SX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | SX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | SX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |

The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

### I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ($V_{OD}$) and programmable pre-emphasis

## Table 20. Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|---|---|---|---|
| DDR4 SDRAM | Quarter rate | Yes | 1,067 |
| | | — | 1,200 |
| DDR3 SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 1,067 |
| | | — | 1,067 |
| DDR3L SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 933 |
| | | — | 933 |
| LPDDR3 SDRAM | Half rate | — | 533 |
| | Quarter rate | — | 800 |

## Table 21. Memory Standards Supported by the Soft Memory Controller

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| RLDRAM 3 (11) | Quarter rate | 1,200 |
| QDR IV SRAM(11) | Quarter rate | 1,067 |
| QDR II SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ Xtreme SRAM | Full rate | 333 |
| | Half rate | 633 |

## Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,067 |
| DDR3L SDRAM | Half rate | 933 |

(11) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

**Related Information**

Intel Arria 10 Device Datasheet
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

## PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

**Related Information**

PCS Features on page 30

## Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

### Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

**Related Information**

PCS Features on page 30

### 10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

**Related Information**

PCS Features on page 30

## Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed

**Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices**

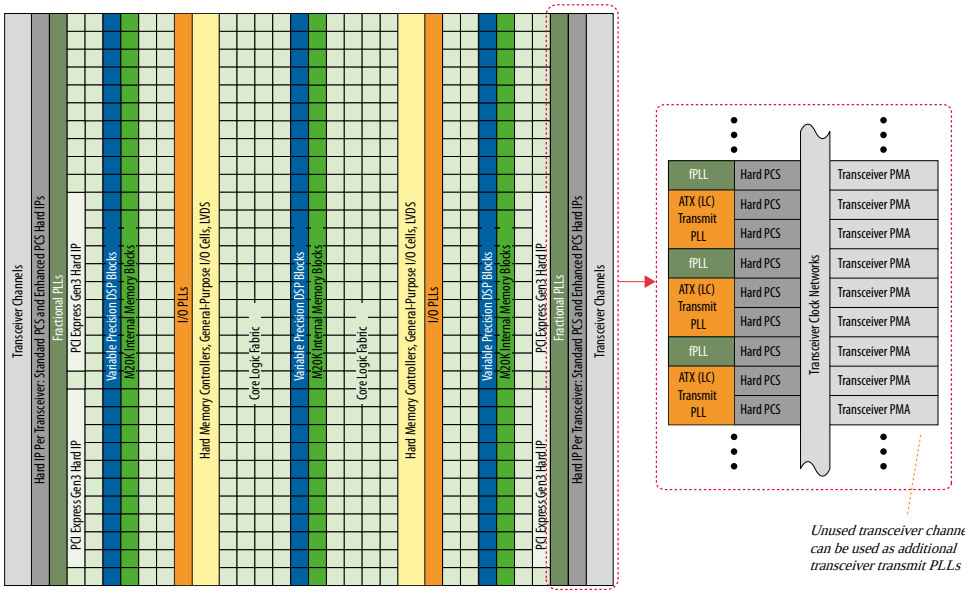
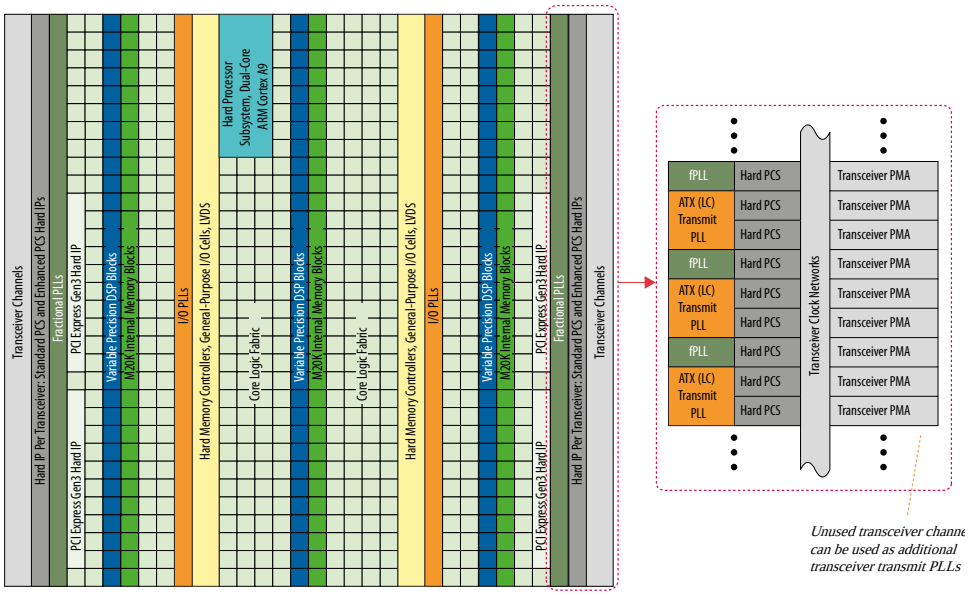



**Figure 8. Device Chip Overview for Intel Arria 10 SX Devices**




## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

| PCS | Description |
|---|---|
| Standard PCS | • Operates at a data rate up to 12 Gbps<br>• Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS<br>• Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | • Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA<br>• Handles data transfer to and from the FPGA fabric<br>• Handles data transfer internally to and from the PMA<br>• Provides frequency compensation<br>• Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | • Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates<br>• Provides support for PIPE 3.0 features<br>• Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

### Related Information

- PCIe Gen1, Gen2, and Gen3 Hard IP on page 26
- Interlaken Support on page 26
- 10 Gbps Ethernet Support on page 26

## PCS Protocol Support

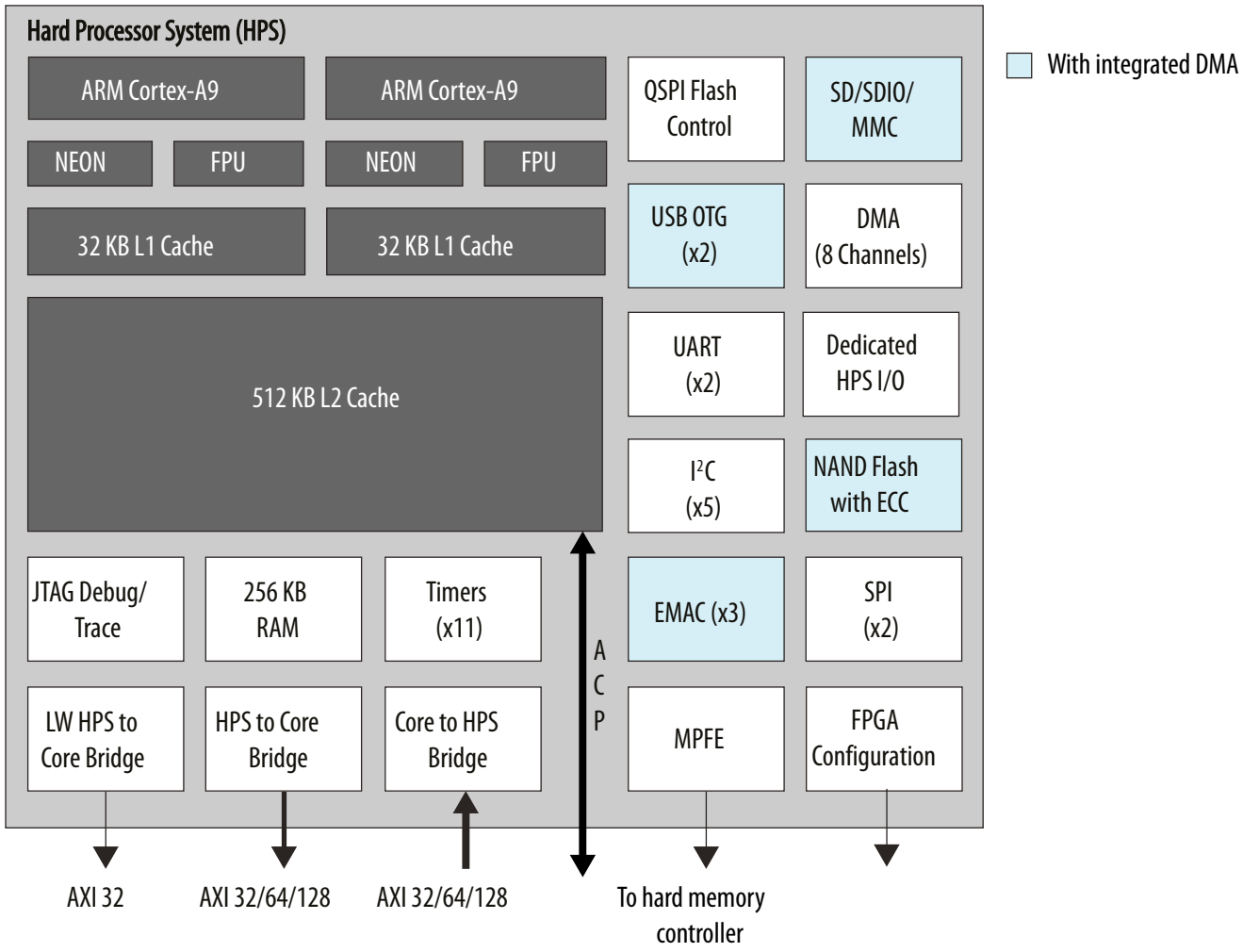
This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |

***continued...***

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.




## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

## Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an "overdrive" feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC:<br>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.<br>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.<br>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or $I^2C$ interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |

## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

# Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

## Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

## Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.

| Date | Version | Changes |
|---|---|---|
| December 2015 | 2015.12.14 | • Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.<br>• Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | • Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.<br>• Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in **Number of Multipliers in Intel Arria 10 Devices** table.<br>• Updated the available options for Arria 10 GX, GT, and SX.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | • Added support for 13.5G JESD204b in the Summary of Features table.<br>• Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.<br>• Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.<br>• Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | • Added floating point arithmetic features in the Summary of Features table.<br>• Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.<br>• Updated the table that lists the memory standards supported by Intel Arria 10 devices.<br>• Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2.<br>• Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller.<br>• Added soft memory controller support for QDR IV.<br>• Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.<br>• Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.<br>• Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.<br>• Added a feature for fractional synthesis PLLs: PLL cascading.<br>• Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | • Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.<br>• Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.<br>• Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |

***continued...***