



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 217080  |
| Number of Logic Elements/Cells | 570000  |
| Total RAM Bits                 | 42082304  |
| Number of I/O                  | 492   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.87V ~ 0.98V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 100°C (TJ)  |
| Package / Case                 | 1152-BBGA, FCBGA  |
| Supplier Device Package        | 1152-FCBGA (35x35)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/10ax057h2f34e2sg">https://www.e-xfl.com/product-detail/intel/10ax057h2f34e2sg</a> |



## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

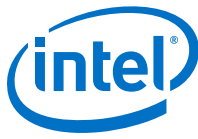
**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market                | Applications  |
|-----------------------|---|
| Wireless              | <ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>   |
| Wireline              | <ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>            |
| Broadcast             | <ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul> |
| Computing and Storage | <ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>   |
| Medical               | <ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>   |
| Military              | <ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>          |

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



**Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)**

| Resource                     |                      | Product Line |           |           |           |
|------------------------------|----------------------|--------------|-----------|-----------|-----------|
|                              |                      | GX 570       | GX 660    | GX 900    | GX 1150   |
| Logic Elements (LE) (K)      |                      | 570          | 660       | 900       | 1,150     |
| ALM                          |                      | 217,080      | 251,680   | 339,620   | 427,200   |
| Register                     |                      | 868,320      | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb)                  | M20K                 | 36,000       | 42,620    | 48,460    | 54,260    |
|                              | MLAB                 | 5,096        | 5,788     | 9,386     | 12,984    |
| Variable-precision DSP Block |                      | 1,523        | 1,687     | 1,518     | 1,518     |
| 18 x 19 Multiplier           |                      | 3,046        | 3,374     | 3,036     | 3,036     |
| PLL                          | Fractional Synthesis | 16           | 16        | 32        | 32        |
|                              | I/O                  | 16           | 16        | 16        | 16        |
| 17.4 Gbps Transceiver        |                      | 48           | 48        | 96        | 96        |
| GPIO <sup>(3)</sup>          |                      | 696          | 696       | 768       | 768       |
| LVDS Pair <sup>(4)</sup>     |                      | 324          | 324       | 384       | 384       |
| PCIe Hard IP Block           |                      | 2            | 2         | 4         | 4         |
| Hard Memory Controller       |                      | 16           | 16        | 16        | 16        |

## Package Plan

**Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |          |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |          |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |          |      |
|--------------|---|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                 | LVDS I/O | XCVR | 3 V I/O                                 | LVDS I/O | XCVR | 3 V I/O                                 | LVDS I/O | XCVR |
| GX 160       | 48                                      | 192      | 6    | 48                                      | 192      | 12   | 48                                      | 240      | 12   |
| GX 220       | 48                                      | 192      | 6    | 48                                      | 192      | 12   | 48                                      | 240      | 12   |
| GX 270       | —                                       | —        | —    | 48                                      | 192      | 12   | 48                                      | 312      | 12   |
| GX 320       | —                                       | —        | —    | 48                                      | 192      | 12   | 48                                      | 312      | 12   |
| GX 480       | —                                       | —        | —    | —                                       | —        | —    | 48                                      | 312      | 12   |

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |             |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |             |      |
|--------------|--|-------------|------|--|-------------|------|---|-------------|------|---|-------------|------|
|              | 3 V<br>I/O                               | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR | 3 V<br>I/O                                | LVDS<br>I/O | XCVR | 3 V<br>I/O                                | LVDS<br>I/O | XCVR |
| GX 270       | 48                                       | 336         | 24   | 48                                       | 336         | 24   | —   | —           | —    | —   | —           | —    |
| GX 320       | 48                                       | 336         | 24   | 48                                       | 336         | 24   | —   | —           | —    | —   | —           | —    |
| GX 480       | 48                                       | 444         | 24   | 48                                       | 348         | 36   | —   | —           | —    | —   | —           | —    |
| GX 570       | 48                                       | 444         | 24   | 48                                       | 348         | 36   | 96  | 600         | 36   | 48  | 540         | 48   |
| GX 660       | 48                                       | 444         | 24   | 48                                       | 348         | 36   | 96  | 600         | 36   | 48  | 540         | 48   |
| GX 900       | —  | 504         | 24   | —  | —           | —    | —   | —           | —    | —   | 600         | 48   |
| GX 1150      | —  | 504         | 24   | —  | —           | —    | —   | —           | —    | —   | 600         | 48   |

**Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |             |      | NF45<br>(45 mm × 45 mm)<br>1932-pin FBGA) |             |      | SF45<br>(45 mm × 45 mm)<br>1932-pin FBGA) |             |      | UF45<br>(45 mm × 45 mm)<br>1932-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|---|-------------|------|
|              | 3 V<br>I/O                                | LVDS<br>I/O | XCVR | 3 V<br>I/O                                | LVDS<br>I/O | XCVR | 3 V<br>I/O                                | LVDS<br>I/O | XCVR | 3 V<br>I/O                                | LVDS<br>I/O | XCVR |
| GX 900       | —   | 342         | 66   | —   | 768         | 48   | —   | 624         | 72   | —   | 480         | 96   |
| GX 1150      | —   | 342         | 66   | —   | 768         | 48   | —   | 624         | 72   | —   | 480         | 96   |

### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices**

| Resource                       |                      | Product Line |         |         |         |         |         |           |
|--------------------------------|----------------------|--------------|---------|---------|---------|---------|---------|-----------|
|                                |                      | SX 160       | SX 220  | SX 270  | SX 320  | SX 480  | SX 570  | SX 660    |
| Logic Elements (LE) (K)        |                      | 160          | 220     | 270     | 320     | 480     | 570     | 660       |
| ALM                            |                      | 61,510       | 80,330  | 101,620 | 119,900 | 183,590 | 217,080 | 251,680   |
| Register                       |                      | 246,040      | 321,320 | 406,480 | 479,600 | 734,360 | 868,320 | 1,006,720 |
| Memory (Kb)                    | M20K                 | 8,800        | 11,740  | 15,000  | 17,820  | 28,620  | 36,000  | 42,620    |
|                                | MLAB                 | 1,050        | 1,690   | 2,452   | 2,727   | 4,164   | 5,096   | 5,788     |
| Variable-precision DSP Block   |                      | 156          | 192     | 830     | 985     | 1,368   | 1,523   | 1,687     |
| 18 x 19 Multiplier             |                      | 312          | 384     | 1,660   | 1,970   | 2,736   | 3,046   | 3,374     |
| PLL                            | Fractional Synthesis | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
|                                | I/O                  | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
| 17.4 Gbps Transceiver          |                      | 12           | 12      | 24      | 24      | 36      | 48      | 48        |
| GPIO <sup>(8)</sup>            |                      | 288          | 288     | 384     | 384     | 492     | 696     | 696       |
| LVDS Pair <sup>(9)</sup>       |                      | 120          | 120     | 168     | 168     | 174     | 324     | 324       |
| PCIe Hard IP Block             |                      | 1            | 1       | 2       | 2       | 2       | 2       | 2         |
| Hard Memory Controller         |                      | 6            | 6       | 8       | 8       | 12      | 16      | 16        |
| ARM Cortex-A9 MPCore Processor |                      | Yes          | Yes     | Yes     | Yes     | Yes     | Yes     | Yes       |

## Package Plan

**Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|--|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                               | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 160       | 48                                       | 144         | 6    | 48                                      | 192         | 12   | 48                                      | 240         | 12   | —  | —           | —    |
| SX 220       | 48                                       | 144         | 6    | 48                                      | 192         | 12   | 48                                      | 240         | 12   | —  | —           | —    |
| SX 270       | —  | —           | —    | 48                                      | 192         | 12   | 48                                      | 312         | 12   | 48                                       | 336         | 24   |
| SX 320       | —  | —           | —    | 48                                      | 192         | 12   | 48                                      | 312         | 12   | 48                                       | 336         | 24   |
| continued... |  |             |      |   |             |      |   |             |      |  |             |      |

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.





| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 480       | —                                       | —           | —    | —                                       | —           | —    | 48                                      | 312         | 12   | 48                                       | 444         | 24   |
| SX 570       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |
| SX 660       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |          |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      |
|--------------|--|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                  | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR |
| SX 270       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 320       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 480       | 48                                       | 348      | 36   | —   | —        | —    | —   | —        | —    |
| SX 570       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |
| SX 660       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

**Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices**

| Usage Example   | Multiplier Size (Bit)           | DSP Block Resources |
|---|---------------------------------|---------------------|
| Medium precision fixed point                            | Two 18 x 19                     | 1                   |
| High precision fixed or Single precision floating point | One 27 x 27                     | 1                   |
| Fixed point FFTs  | One 19 x 36 with external adder | 1                   |
| Very high precision fixed point                         | One 36 x 36 with external adder | 2                   |
| Double precision floating point                         | One 54 x 54 with external adder | 4                   |

**Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|-------------------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|                   |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
| Intel Arria 10 GX | GX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | GX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | GX 270       | 830                          | 1,660   | 830                | 830                               | 830   |
|                   | GX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|                   | GX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|                   | GX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|                   | GX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |
|                   | GX 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GX 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GT 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 SX | SX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | SX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | SX 270       | 830                          | 1,660   | 830                | 830                               | 830   |

*continued...*



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|         |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
|         | SX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|         | SX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|         | SX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|         | SX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | GX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | GX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | GX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | GX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | GX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | GX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |
|                   | GX 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GX 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GT 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 SX | SX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | SX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | SX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | SX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | SX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | SX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | SX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits)       | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB         | 32                 | x16, x18, or x20   |
|              | 64 <sup>(10)</sup> | x8, x9, x10        |
| M20K         | 512                | x40, x32           |
|              | 1K                 | x20, x16           |
|              | 2K                 | x10, x8            |
|              | 4K                 | x5, x4             |
|              | 8K                 | x2                 |
|              | 16K                | x1                 |

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.

- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

#### [External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|-----------------|--------------|-----------------------|-------------------------|
| DDR4 SDRAM      | Quarter rate | Yes                   | 1,067                   |
|                 |              | —                     | 1,200                   |
| DDR3 SDRAM      | Half rate    | Yes                   | 533                     |
|                 |              | —                     | 667                     |
|                 | Quarter rate | Yes                   | 1,067                   |
|                 |              | —                     | 1,067                   |
| DDR3L SDRAM     | Half rate    | Yes                   | 533                     |
|                 |              | —                     | 667                     |
|                 | Quarter rate | Yes                   | 933                     |
|                 |              | —                     | 933                     |
| LPDDR3 SDRAM    | Half rate    | —                     | 533                     |
|                 | Quarter rate | —                     | 800                     |

**Table 21. Memory Standards Supported by the Soft Memory Controller**

| Memory Standard             | Rate Support | Maximum Frequency (MHz) |
|-----------------------------|--------------|-------------------------|
| RLDRAM 3 <sup>(11)</sup>    | Quarter rate | 1,200                   |
| QDR IV SRAM <sup>(11)</sup> | Quarter rate | 1,067                   |
| QDR II SRAM                 | Full rate    | 333                     |
|                             | Half rate    | 633                     |
| QDR II+ SRAM                | Full rate    | 333                     |
|                             | Half rate    | 633                     |
| QDR II+ Xtreme SRAM         | Full rate    | 333                     |
|                             | Half rate    | 633                     |

**Table 22. Memory Standards Supported by the HPS Hard Memory Controller**

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|-----------------|--------------|-------------------------|
| DDR4 SDRAM      | Half rate    | 1,200                   |
| DDR3 SDRAM      | Half rate    | 1,067                   |
| DDR3L SDRAM     | Half rate    | 933                     |

<sup>(11)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices

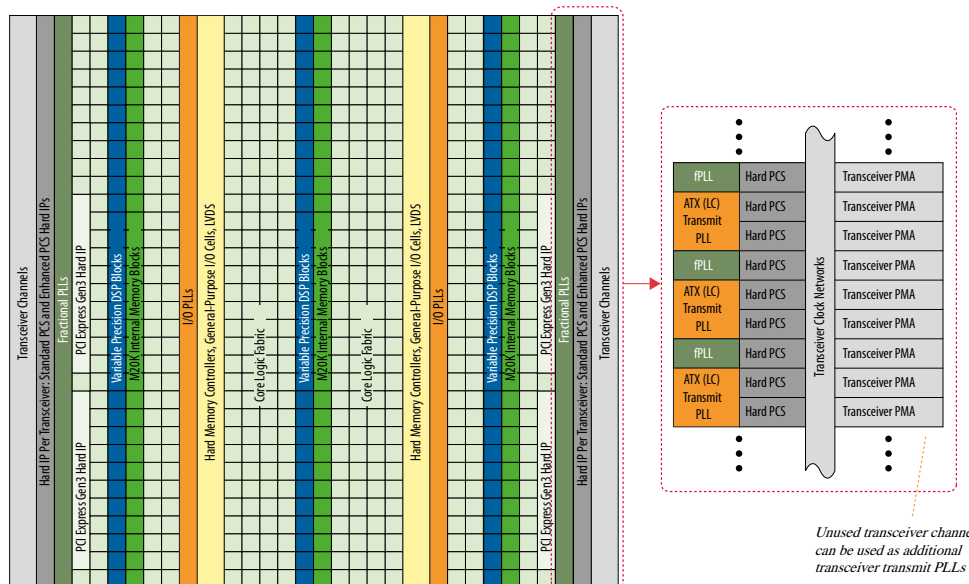


Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.



Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

| Feature   | Capability   |
|---|--|
| Chip-to-Chip Data Rates                                 | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)   |
| Backplane Support                                       | Drive backplanes at data rates up to 12.5 Gbps   |
| Optical Module Support                                  | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4   |
| Cable Driving Support                                   | SFP+ Direct Attach, PCI Express over cable, eSATA  |
| Transmit Pre-Emphasis                                   | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss  |
| Continuous Time Linear Equalizer (CTLE)                 | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss  |
| Decision Feedback Equalizer (DFE)                       | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments  |
| Variable Gain Amplifier                                 | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes  |
| Altera Digital Adaptive Parametric Tuning (ADAPT)       | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance  |
| Advanced Transmit (ATX) PLL                             | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols   |
| Fractional PLLs   | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost   |
| Digitally Assisted Analog CDR                           | Superior jitter tolerance with fast lock time  |
| Dynamic Partial Reconfiguration                         | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility   |
| Multiple PCS-PMA and PCS-PLD interface widths           | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency  |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.





| PCS           | Description  |
|---------------|--|
| Standard PCS  | <ul style="list-style-type: none"> <li>Operates at a data rate up to 12 Gbps</li> <li>Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS</li> <li>Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.</li> </ul>   |
| Enhanced PCS  | <ul style="list-style-type: none"> <li>Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA</li> <li>Handles data transfer to and from the FPGA fabric</li> <li>Handles data transfer internally to and from the PMA</li> <li>Provides frequency compensation</li> <li>Performs channel bonding for multi-channel low skew applications</li> </ul> |
| PCIe Gen3 PCS | <ul style="list-style-type: none"> <li>Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates</li> <li>Provides support for PIPE 3.0 features</li> <li>Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed</li> </ul>  |

### Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol                                     | Data Rate (Gbps) | Transceiver IP              | PCS Support                    |
|--|------------------|-----------------------------|--------------------------------|
| PCIe Gen3 x1, x2, x4, x8                     | 8.0              | Native PHY (PIPE)           | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8                     | 5.0              | Native PHY (PIPE)           | Standard PCS                   |
| PCIe Gen1 x1, x2, x4, x8                     | 2.5              | Native PHY (PIPE)           | Standard PCS                   |
| 1000BASE-X Gigabit Ethernet                  | 1.25             | Native PHY                  | Standard PCS                   |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25             | Native PHY                  | Standard PCS                   |
| 10GBASE-R                                    | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-R with IEEE 1588v2                   | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-R with KR FEC                        | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-KR and 1000BASE-X                    | 10.3125          | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS  |
| Interlaken (CEI-6G/11G)                      | 3.125 to 17.4    | Native PHY                  | Enhanced PCS                   |
| SFI-S/SFI-5.2                                | 11.2             | Native PHY                  | Enhanced PCS                   |
| 10G SDI                                      | 10.692           | Native PHY                  | Enhanced PCS                   |
| continued...                                 |                  |                             |                                |



**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/<br>Improvements                           | Description   |
|---|---|
| Increased performance and overdrive capability        | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.   |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.   |
| Flexible I/O sharing                                  | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul> |
| EMAC core   | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.  |
| On-chip memory  | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.  |
| ECC enhancements                                      | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.   |
| HPS to FPGA Interconnect Backbone                     | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.  |
| FPGA configuration and HPS booting                    | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.  |
| Security  | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).   |

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

**Table 25. Configuration Schemes and Features of Intel Arria 10 Devices**

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme   | Data Width    | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update                |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG   | 1 bit         | 33                   | 33                                   | —             | —                               | Yes <sup>(16)</sup>                     | —                                   |
| Active Serial (AS) through the EPCQ-L configuration device   | 1 bit, 4 bits | 100                  | 400                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Yes                                 |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit         | 100                  | 100                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Parallel Flash Loader (PFL) IP core |

*continued...*

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(16)</sup> Partial configuration can be performed only when it is configured as internal host.