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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Discontinued at Digi-Key
Number of LABs/CLBs	217080
Number of Logic Elements/Cells	570000
Total RAM Bits	42082304
Number of I/O	492
Number of Gates	-
Voltage - Supply	0.87V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/10ax057k1f35e1sg">https://www.e-xfl.com/product-detail/intel/10ax057k1f35e1sg</a>



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## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

Market	Applications
Wireless	<ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>
Wireline	<ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>
Broadcast	<ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul>
Computing and Storage	<ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>
Medical	<ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>
Military	<ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Key Advantages of Intel Arria 10 Devices

**Table 2. Key Advantages of the Intel Arria 10 Device Family**

Advantage	Supporting Feature
Enhanced core architecture	<ul style="list-style-type: none"><li>Built on TSMC's 20 nm process technology</li><li>60% higher performance than the previous generation of mid-range FPGAs</li><li>15% higher performance than the fastest previous-generation FPGA</li></ul>
High-bandwidth integrated transceivers	<ul style="list-style-type: none"><li>Short-reach rates up to 25.8 Gigabits per second (Gbps)</li><li>Backplane capability up to 12.5 Gbps</li><li>Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)</li></ul>
Improved logic integration and hard IP blocks	<ul style="list-style-type: none"><li>8-input adaptive logic module (ALM)</li><li>Up to 65.6 megabits (Mb) of embedded memory</li><li>Variable-precision digital signal processing (DSP) blocks</li><li>Fractional synthesis phase-locked loops (PLLs)</li><li>Hard PCI Express Gen3 IP blocks</li><li>Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)</li></ul>
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	<ul style="list-style-type: none"><li>Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)</li><li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li></ul>
Advanced power savings	<ul style="list-style-type: none"><li>Comprehensive set of advanced power saving features</li><li>Power-optimized MultiTrack routing and core architecture</li><li>Up to 40% lower power compared to previous generation of mid-range FPGAs</li><li>Up to 60% lower power compared to previous generation of high-end FPGAs</li></ul>

## Summary of Intel Arria 10 Features

**Table 3. Summary of Features for Intel Arria 10 Devices**

Feature	Description
Technology	<ul style="list-style-type: none"><li>TSMC's 20-nm SoC process technology</li><li>Allows operation at a lower <math>V_{CC}</math> level of 0.82 V instead of the 0.9 V standard <math>V_{CC}</math> core voltage</li></ul>
Packaging	<ul style="list-style-type: none"><li>1.0 mm ball-pitch FINELINE BGA packaging</li><li>0.8 mm ball-pitch Ultra FINELINE BGA packaging</li><li>Multiple devices with identical package footprints for seamless migration between different FPGA densities</li><li>Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices</li><li>RoHS, leaded<sup>(1)</sup>, and lead-free (Pb-free) options</li></ul>
High-performance FPGA fabric	<ul style="list-style-type: none"><li>Enhanced 8-input ALM with four registers</li><li>Improved multi-track routing architecture to reduce congestion and improve compilation time</li><li>Hierarchical core clocking architecture</li><li>Fine-grained partial reconfiguration</li></ul>
Internal memory blocks	<ul style="list-style-type: none"><li>M20K—20-Kb memory blocks with hard error correction code (ECC)</li><li>Memory logic array block (MLAB)—640-bit memory</li></ul>
continued...	

(1) Contact Intel for availability.



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none"><li>Continuous operating range:<ul style="list-style-type: none"><li>Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>Backplane support:<ul style="list-style-type: none"><li>Intel Arria 10 GX—up to 12.5</li><li>Intel Arria 10 GT—up to 12.5</li></ul></li><li>Extended range down to 125 Mbps with oversampling</li><li>ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>Adaptive linear and decision feedback equalization</li><li>Transmitter pre-emphasis and de-emphasis</li><li>Dynamic partial reconfiguration of individual transceiver channels</li></ul>	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none"><li>Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>256 KB on-chip RAM and 64 KB on-chip ROM</li><li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>
	External interfaces	<ul style="list-style-type: none"><li>Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>
	Interconnects to core	<ul style="list-style-type: none"><li>High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul>
Configuration	<ul style="list-style-type: none"><li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>	
continued...		

(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Feature	Description
	<ul style="list-style-type: none"><li>Dynamic reconfiguration of the transceivers and PLLs</li><li>Fine-grained partial reconfiguration of the core fabric</li><li>Active Serial x4 Interface</li></ul>
Power management	<ul style="list-style-type: none"><li>SmartVID</li><li>Low static power device options</li><li>Programmable Power Technology</li><li>Intel Quartus Prime integrated power analysis</li></ul>
Software and tools	<ul style="list-style-type: none"><li>Intel Quartus Prime design suite</li><li>Transceiver toolkit</li><li>Platform Designer system integration tool</li><li>DSP Builder for Intel FPGAs</li><li>OpenCL™ support</li><li>Intel SoC FPGA Embedded Design Suite (EDS)</li></ul>

### Related Information

#### [Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: <ul style="list-style-type: none"><li>17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.</li><li>25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.</li></ul>
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

### Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

#### [Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





## Maximum Resources

**Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices**

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687
18 x 19 Multiplier		312	384	1,660	1,970	2,736	3,046	3,374
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO <sup>(8)</sup>		288	288	384	384	492	696	696
LVDS Pair <sup>(9)</sup>		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

## Package Plan

**Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
continued...												

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.





Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 480	—	—	—	—	—	—	48	312	12	48	444	24
SX 570	—	—	—	—	—	—	—	—	—	48	444	24
SX 660	—	—	—	—	—	—	—	—	—	48	444	24

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

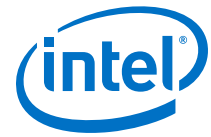
Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 270	48	336	24	—	—	—	—	—	—
SX 320	48	336	24	—	—	—	—	—	—
SX 480	48	348	36	—	—	—	—	—	—
SX 570	48	348	36	96	600	36	48	540	48
SX 660	48	348	36	96	600	36	48	540	48

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



## I/O Vertical Migration for Intel Arria 10 Devices

**Figure 4. Migration Capability Across Intel Arria 10 Product Lines**

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160	↑	↑	↑								
	GX 220	↓	↑	↑								
	GX 270		↑	↑	↑	↑						
	GX 320		↓	↑	↑	↑						
	GX 480			↓	↑	↑						
	GX 570				↑	↑	↑	↑				
	GX 660				↑	↓	↑	↑	↑	↑	↑	↑
	GX 900				↑			↑	↑	↑	↑	↑
	GX 1150				↑			↑	↑	↑	↑	↑
	GT 900										↑	↑
	GT 1150										↓	↑
Intel Arria 10 SX	SX 160	↑	↑	↑								
	SX 220	↓	↑	↑								
	SX 270		↑	↑	↑	↑						
	SX 320		↓	↑	↑	↑						
	SX 480			↓	↑	↑						
	SX 570				↑	↑	↑	↑				
	SX 660				↑	↑	↑	↑				

**Note:** To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

## Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

**Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices**

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

**Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
Intel Arria 10 GX	GX 160	156	312	156	156	156
	GX 220	192	384	192	192	192
	GX 270	830	1,660	830	830	830
	GX 320	984	1,968	984	984	984
	GX 480	1,368	2,736	1,368	1,368	1,368
	GX 570	1,523	3,046	1,523	1,523	1,523
	GX 660	1,687	3,374	1,687	1,687	1,687
	GX 900	1,518	3,036	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 GT	GT 900	1,518	3,036	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 SX	SX 160	156	312	156	156	156
	SX 220	192	384	192	192	192
	SX 270	830	1,660	830	830	830

*continued...*

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 <sup>(10)</sup>	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

---

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

## I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

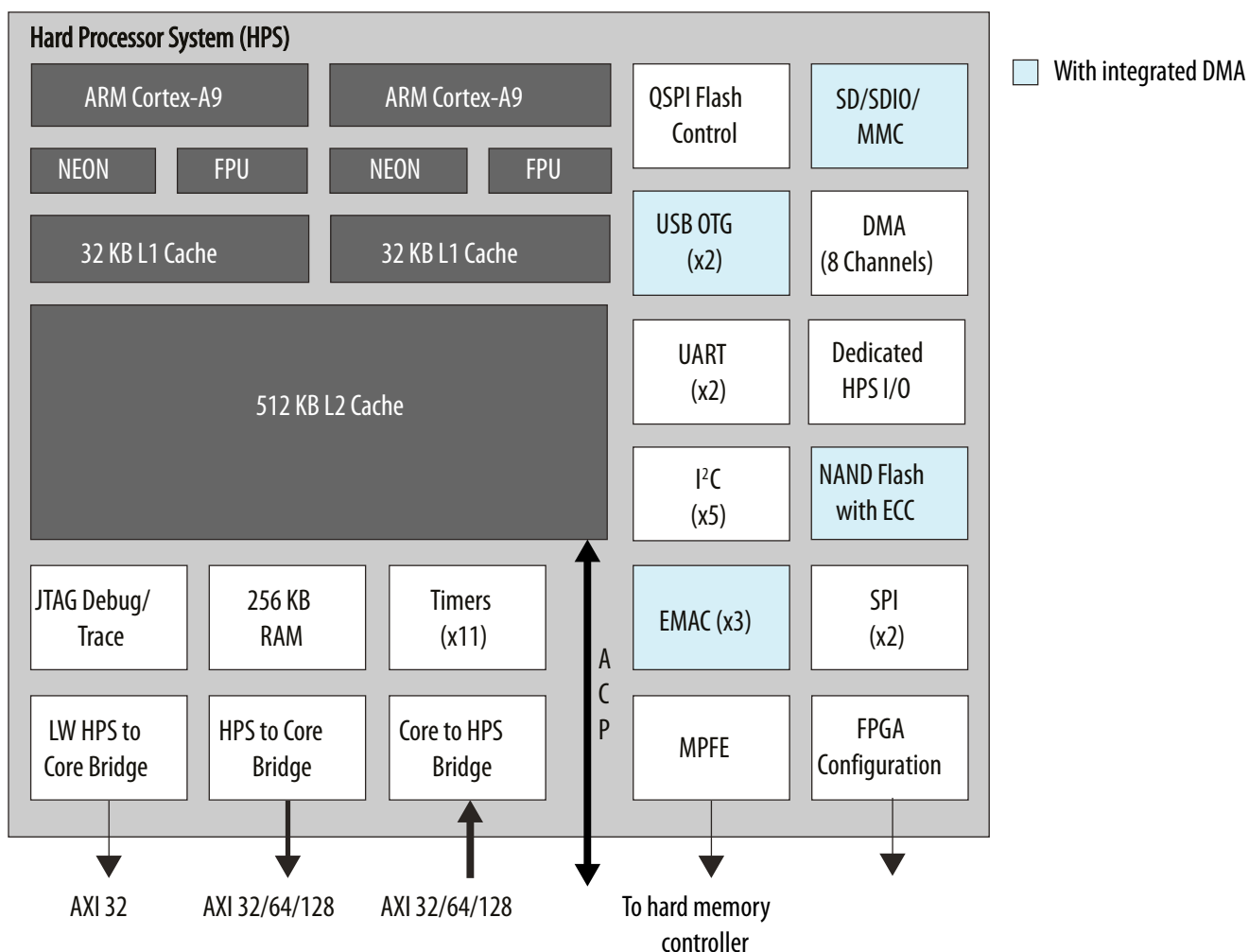
Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul>
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).





## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) <sup>(13)</sup>	Decompression	Design Security <sup>(14)</sup>	Partial Reconfiguration <sup>(15)</sup>	Remote System Update
Fast passive parallel (FPP) through CPLD or external microcontroller	8 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	PFL IP core
	16 bits			Yes	Yes		
	32 bits			Yes	Yes		
Configuration via HPS	16 bits	100	3200	Yes	Yes	Yes <sup>(17)</sup>	—
	32 bits			Yes	Yes		
Configuration via Protocol [CvP (PCIe*)]	x1, x2, x4, x8 lanes	—	8000	Yes	Yes	Yes <sup>(16)</sup>	—

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(17)</sup> Supported at a maximum clock rate of 100 MHz.



Date	Version	Changes
August 2014	2014.08.18	<ul style="list-style-type: none"> <li>Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.</li> <li>Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.</li> <li>Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.</li> <li>Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.</li> <li>Added variable precision DSP blocks support for floating-point arithmetic.</li> </ul>
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	<ul style="list-style-type: none"> <li>Updated the HPS memory standards support from LPDDR2 to LPDDR3.</li> <li>Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .</li> </ul>
December 2013	2013.12.02	Initial release.