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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	217080
Number of Logic Elements/Cells	570000
Total RAM Bits	42082304
Number of I/O	588
Number of Gates	-
Voltage - Supply	0.87V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FCBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10ax057n2f40e2lg



Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

Market	Applications
Wireless	<ul style="list-style-type: none"> • Channel and switch cards in remote radio heads • Mobile backhaul
Wireline	<ul style="list-style-type: none"> • 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation
Broadcast	<ul style="list-style-type: none"> • Studio switches • Servers and transport • Videoconferencing • Professional audio and video
Computing and Storage	<ul style="list-style-type: none"> • Flash cache • Cloud computing servers • Server acceleration
Medical	<ul style="list-style-type: none"> • Diagnostic scanners • Diagnostic imaging
Military	<ul style="list-style-type: none"> • Missile guidance and control • Radar • Electronic warfare • Secure communications

Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



Feature	Description	
Embedded Hard IP blocks	Variable-precision DSP	<ul style="list-style-type: none">Native support for signal processing precision levels from 18 x 19 to 54 x 54Native support for 27 x 27 multiplier mode64-bit accumulator and cascade for systolic finite impulse responses (FIRs)Internal coefficient memory banksPadder/subtractor for improved efficiencyAdditional pipeline register to increase performance and reduce powerSupports floating point arithmetic:<ul style="list-style-type: none">Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.Dynamic accumulator reset control.Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.
	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express*	PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port
	Transceiver I/O	<ul style="list-style-type: none">10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)PCS hard IPs that support:<ul style="list-style-type: none">10-Gbps Ethernet (10GbE)PCIe PIPE interfaceInterlakenGbps Ethernet (GbE)Common Public Radio Interface (CPRI) with deterministic latency supportGigabit-capable passive optical network (GPON) with fast lock-time support13.5G JESD204b8B/10B, 64B/66B, 64B/67B encoders and decodersCustom mode support for proprietary protocols
Core clock networks	<ul style="list-style-type: none">Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none">667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface800 MHz LVDS interface clocking with 1,600 Mbps LVDS interfaceGlobal, regional, and peripheral clock networksClock networks that are not used can be gated to reduce dynamic power	
Phase-locked loops (PLLs)	<ul style="list-style-type: none">High-resolution fractional synthesis PLLs:<ul style="list-style-type: none">Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)Support integer mode and fractional modeFractional mode support with third-order delta-sigma modulationInteger PLLs:<ul style="list-style-type: none">Adjacent to general purpose I/OsSupport external memory and LVDS interfaces	
FPGA General-purpose I/Os (GPIOs)	<ul style="list-style-type: none">1.6 Gbps LVDS—every pair can be configured as receiver or transmitterOn-chip termination (OCT)1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing	
External Memory Interface	<ul style="list-style-type: none">Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none">DDR4—speeds up to 1,200 MHz/2,400 MbpsDDR3—speeds up to 1,067 MHz/2,133 MbpsSoft memory controller—provides support for RLDRAM 3⁽²⁾, QDR IV⁽²⁾, and QDR II+	
continued...		



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none">Continuous operating range:<ul style="list-style-type: none">Intel Arria 10 GX—1 Gbps to 17.4 GbpsIntel Arria 10 GT—1 Gbps to 25.8 GbpsBackplane support:<ul style="list-style-type: none">Intel Arria 10 GX—up to 12.5Intel Arria 10 GT—up to 12.5Extended range down to 125 Mbps with oversamplingATX transmit PLLs with user-configurable fractional synthesis capabilityElectronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical moduleAdaptive linear and decision feedback equalizationTransmitter pre-emphasis and de-emphasisDynamic partial reconfiguration of individual transceiver channels	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none">Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability256 KB on-chip RAM and 64 KB on-chip ROMSystem peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managersSecurity features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage
	External interfaces	<ul style="list-style-type: none">Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controllerCommunication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I²C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)
	Interconnects to core	<ul style="list-style-type: none">High-performance ARM AMBA* AXI bus bridges that support simultaneous read and writeHPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versaConfiguration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration portFPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller
Configuration	<ul style="list-style-type: none">Tamper protection—comprehensive design protection to protect your valuable IP investmentsEnhanced 256-bit advanced encryption standard (AES) design security with authenticationConfiguration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3	
continued...		

⁽²⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

Resource		Product Line			
		GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		570	660	900	1,150
ALM		217,080	251,680	339,620	427,200
Register		868,320	1,006,720	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precision DSP Block		1,523	1,687	1,518	1,518
18 x 19 Multiplier		3,046	3,374	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	16	16	16
17.4 Gbps Transceiver		48	48	96	96
GPIO ⁽³⁾		696	696	768	768
LVDS Pair ⁽⁴⁾		324	324	384	384
PCIe Hard IP Block		2	2	4	4
Hard Memory Controller		16	16	16	16

Package Plan

Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 160	48	192	6	48	192	12	48	240	12
GX 220	48	192	6	48	192	12	48	240	12
GX 270	—	—	—	48	192	12	48	312	12
GX 320	—	—	—	48	192	12	48	312	12
GX 480	—	—	—	—	—	—	48	312	12



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





I/O Vertical Migration for Intel Arria 10 Devices

Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160	↑	↑	↑								
	GX 220	↓	↓	↓								
	GX 270		↓	↓	↑	↑						
	GX 320		↓	↓	↑	↑						
	GX 480			↓	↑	↑						
	GX 570				↑	↑	↑	↑				
	GX 660				↑	↑	↑	↑	↑	↑	↑	↑
	GX 900				↑			↑	↑	↑	↑	↑
	GX 1150				↑			↑	↑	↑	↑	↑
	GT 900										↑	↑
	GT 1150										↓	↓
Intel Arria 10 SX	SX 160	↑	↑	↑								
	SX 220	↓	↓	↓								
	SX 270		↓	↓	↑	↑						
	SX 320		↓	↓	↑	↑						
	SX 480			↓	↑	↑						
	SX 570				↑	↑	↑	↑				
	SX 660				↑	↑	↑	↑				

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

Figure 5. ALM for Intel Arria 10 Devices



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
	SX 320	984	1,968	984	984	984
	SX 480	1,368	2,736	1,368	1,368	1,368
	SX 570	1,523	3,046	1,523	1,523	1,523
	SX 660	1,687	3,374	1,687	1,687	1,687

Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Single Precision Floating-Point Multiplication Mode	Single-Precision Floating-Point Adder Mode	Single-Precision Floating-Point Multiply Accumulate Mode	Peak Giga Floating-Point Operations per Second (GFLOPs)
Intel Arria 10 GX	GX 160	156	156	156	156	140
	GX 220	192	192	192	192	173
	GX 270	830	830	830	830	747
	GX 320	984	984	984	984	886
	GX 480	1,369	1,368	1,368	1,368	1,231
	GX 570	1,523	1,523	1,523	1,523	1,371
	GX 660	1,687	1,687	1,687	1,687	1,518
	GX 900	1,518	1,518	1,518	1,518	1,366
	GX 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 GT	GT 900	1,518	1,518	1,518	1,518	1,366
	GT 1150	1,518	1,518	1,518	1,518	1,366
Intel Arria 10 SX	SX 160	156	156	156	156	140
	SX 220	192	192	192	192	173
	SX 270	830	830	830	830	747
	SX 320	984	984	984	984	886
	SX 480	1,369	1,368	1,368	1,368	1,231
	SX 570	1,523	1,523	1,523	1,523	1,371
	SX 660	1,687	1,687	1,687	1,687	1,518

Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Intel Arria 10 Devices

Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Intel Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	587	11,740	2,703	1,690	13,430
	GX 270	750	15,000	3,922	2,452	17,452
	GX 320	891	17,820	4,363	2,727	20,547
	GX 480	1,431	28,620	6,662	4,164	32,784
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,131	42,620	9,260	5,788	48,408
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	587	11,740	2,703	1,690	13,430
	SX 270	750	15,000	3,922	2,452	17,452
	SX 320	891	17,820	4,363	2,727	20,547
	SX 480	1,431	28,620	6,662	4,164	32,784
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,131	42,620	9,260	5,788	48,408

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 ⁽¹⁰⁾	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,200
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933
LPDDR3 SDRAM	Half rate	—	533
	Quarter rate	—	800

Table 21. Memory Standards Supported by the Soft Memory Controller

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 ⁽¹¹⁾	Quarter rate	1,200
QDR IV SRAM ⁽¹¹⁾	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

⁽¹¹⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Related Information

[Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

Related Information

[PCS Features](#) on page 30

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

Related Information

[PCS Features](#) on page 30

10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

Figure 6. Intel Arria 10 Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices) 1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 12.5 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.



PCS	Description
Standard PCS	<ul style="list-style-type: none"> Operates at a data rate up to 12 Gbps Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.
Enhanced PCS	<ul style="list-style-type: none"> Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA Handles data transfer to and from the FPGA fabric Handles data transfer internally to and from the PMA Provides frequency compensation Performs channel bonding for multi-channel low skew applications
PCIe Gen3 PCS	<ul style="list-style-type: none"> Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates Provides support for PIPE 3.0 features Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed

Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

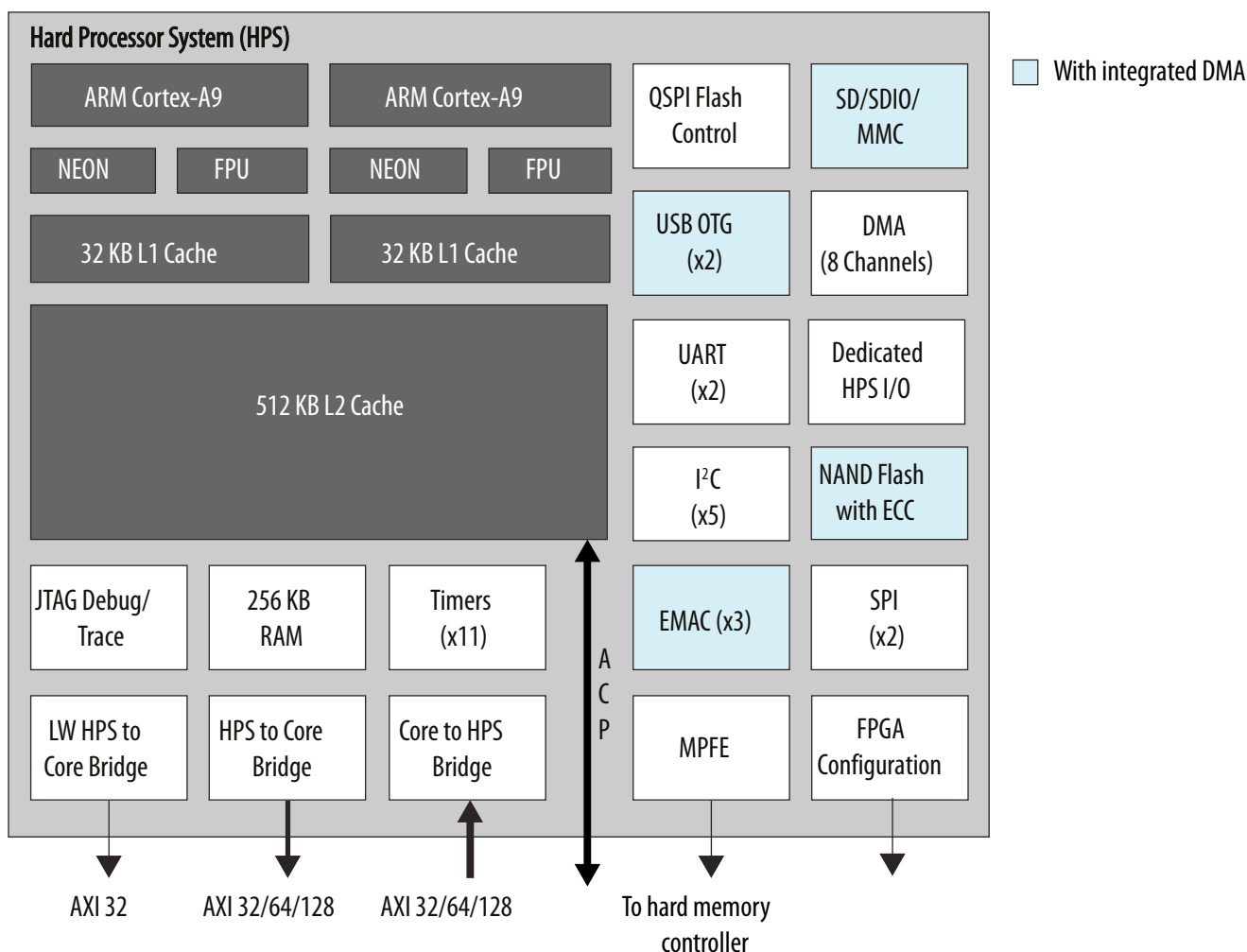
PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen3 x1, x2, x4, x8	8.0	Native PHY (PIPE)	Standard PCS and PCIe Gen3 PCS
PCIe Gen2 x1, x2, x4, x8	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4, x8	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS
1000BASE-X Gigabit Ethernet with IEEE 1588v2	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R with IEEE 1588v2	10.3125	Native PHY	Enhanced PCS
10GBASE-R with KR FEC	10.3125	Native PHY	Enhanced PCS
10GBASE-KR and 1000BASE-X	10.3125	1G/10GbE and 10GBASE-KR PHY	Standard PCS and Enhanced PCS
Interlaken (CEI-6G/11G)	3.125 to 17.4	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	11.2	Native PHY	Enhanced PCS
10G SDI	10.692	Native PHY	Enhanced PCS
continued...			

Figure 9. HPS Block Diagram

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.



Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none">• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I ² C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



Date	Version	Changes
August 2014	2014.08.18	<ul style="list-style-type: none"> Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620. Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table. Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration. Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller. Added variable precision DSP blocks support for floating-point arithmetic.
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	<ul style="list-style-type: none"> Updated the HPS memory standards support from LPDDR2 to LPDDR3. Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .
December 2013	2013.12.02	Initial release.