# Intel - 10AX090N1F40I1SG Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 339620 |
| Number of Logic Elements/Cells | 900000 |
| Total RAM Bits | 59234304 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.98V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FCBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10ax090n1f40i1sg |

# Key Advantages of Intel Arria 10 Devices

## Table 2. Key Advantages of the Intel Arria 10 Device Family

| Advantage | Supporting Feature |
|---|---|
| Enhanced core architecture | • Built on TSMC's 20 nm process technology<br>• 60% higher performance than the previous generation of mid-range FPGAs<br>• 15% higher performance than the fastest previous-generation FPGA |
| High-bandwidth integrated transceivers | • Short-reach rates up to 25.8 Gigabits per second (Gbps)<br>• Backplane capability up to 12.5 Gbps<br>• Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC) |
| Improved logic integration and hard IP blocks | • 8-input adaptive logic module (ALM)<br>• Up to 65.6 megabits (Mb) of embedded memory<br>• Variable-precision digital signal processing (DSP) blocks<br>• Fractional synthesis phase-locked loops (PLLs)<br>• Hard PCI Express Gen3 IP blocks<br>• Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps) |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | • Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)<br>• Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric |
| Advanced power savings | • Comprehensive set of advanced power saving features<br>• Power-optimized MultiTrack routing and core architecture<br>• Up to 40% lower power compared to previous generation of mid-range FPGAs<br>• Up to 60% lower power compared to previous generation of high-end FPGAs |

# Summary of Intel Arria 10 Features

## Table 3. Summary of Features for Intel Arria 10 Devices

| Feature | Description |
|---|---|
| Technology | • TSMC's 20-nm SoC process technology<br>• Allows operation at a lower $V_{CC}$ level of 0.82 V instead of the 0.9 V standard $V_{CC}$ core voltage |
| Packaging | • 1.0 mm ball-pitch Fineline BGA packaging<br>• 0.8 mm ball-pitch Ultra Fineline BGA packaging<br>• Multiple devices with identical package footprints for seamless migration between different FPGA densities<br>• Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices<br>• RoHS, leaded(1), and lead-free (Pb-free) options |
| High-performance FPGA fabric | • Enhanced 8-input ALM with four registers<br>• Improved multi-track routing architecture to reduce congestion and improve compilation time<br>• Hierarchical core clocking architecture<br>• Fine-grained partial reconfiguration |
| Internal memory blocks | • M20K—20-Kb memory blocks with hard error correction code (ECC)<br>• Memory logic array block (MLAB)—640-bit memory |

***continued...***

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(1) Contact Intel for availability.

| Feature | Description |
|---|---|
| | • Dynamic reconfiguration of the transceivers and PLLs<br>• Fine-grained partial reconfiguration of the core fabric<br>• Active Serial x4 Interface |
| Power management | • SmartVID<br>• Low static power device options<br>• Programmable Power Technology<br>• Intel Quartus Prime integrated power analysis |
| Software and tools | • Intel Quartus Prime design suite<br>• Transceiver toolkit<br>• Platform Designer system integration tool<br>• DSP Builder for Intel FPGAs<br>• OpenCL™ support<br>• Intel SoC FPGA Embedded Design Suite (EDS) |

### Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

| Variant | Description |
|---|---|
| Intel Arria 10 GX | FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |
| Intel Arria 10 GT | FPGA featuring:<br>• 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.<br>• 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules. |
| Intel Arria 10 SX | SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. |

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

## Maximum Resources

### Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|---|---|---|---|---|---|---|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO (3) | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair (4) | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

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(3) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(4) Each LVDS I/O pair can be used as differential input or output.

### Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|---|---|---|---|---|---|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO (3) | | 696 | 696 | 768 | 768 |
| LVDS Pair (4) | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

## Package Plan

### Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

### Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

### Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Maximum Resources

### Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

| Resource | | Product Line | |
|---|---|---|---|
| | | GT 900 | GT 1150 |
| Logic Elements (LE) (K) | | 900 | 1,150 |
| ALM | | 339,620 | 427,200 |
| Register | | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 48,460 | 54,260 |
| | MLAB | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 32 | 32 |
| | I/O | 16 | 16 |
| Transceiver | 17.4 Gbps | 72 (5) | 72 (5) |
| | 25.8 Gbps | 6 | 6 |
| GPIO(6) | | 624 | 624 |
| LVDS Pair(7) | | 312 | 312 |
| PCIe Hard IP Block | | 4 | 4 |
| Hard Memory Controller | | 16 | 16 |

### Related Information

Intel Arria 10 GT Channel Usage
Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

### Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45 (45 mm × 45 mm, 1932-pin FBGA) | | |
|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR |
| GT 900 | — | 624 | 72 |
| GT 1150 | — | 624 | 72 |

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(5) If all 6 GT channels are in use, 12 of the GX channels are not usable.

(6) The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

(7) Each LVDS I/O pair can be used as differential input or output.

| Product Line | U19<br>(19 mm × 19 mm, 484-pin UBGA) | | | F27<br>(27 mm × 27 mm, 672-pin FBGA) | | | F29<br>(29 mm × 29 mm, 780-pin FBGA) | | | F34<br>(35 mm × 35 mm, 1152-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 480 | — | — | — | — | — | — | 48 | 312 | 12 | 48 | 444 | 24 |
| SX 570 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |
| SX 660 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |

## Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35<br>(35 mm × 35 mm, 1152-pin FBGA) | | | KF40<br>(40 mm × 40 mm, 1517-pin FBGA) | | | NF40<br>(40 mm × 40 mm, 1517-pin FBGA) | | |
|---|---|---|---|---|---|---|---|---|---|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 270 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 320 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 480 | 48 | 348 | 36 | — | — | — | — | — | — |
| SX 570 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| SX 660 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |

### Related Information

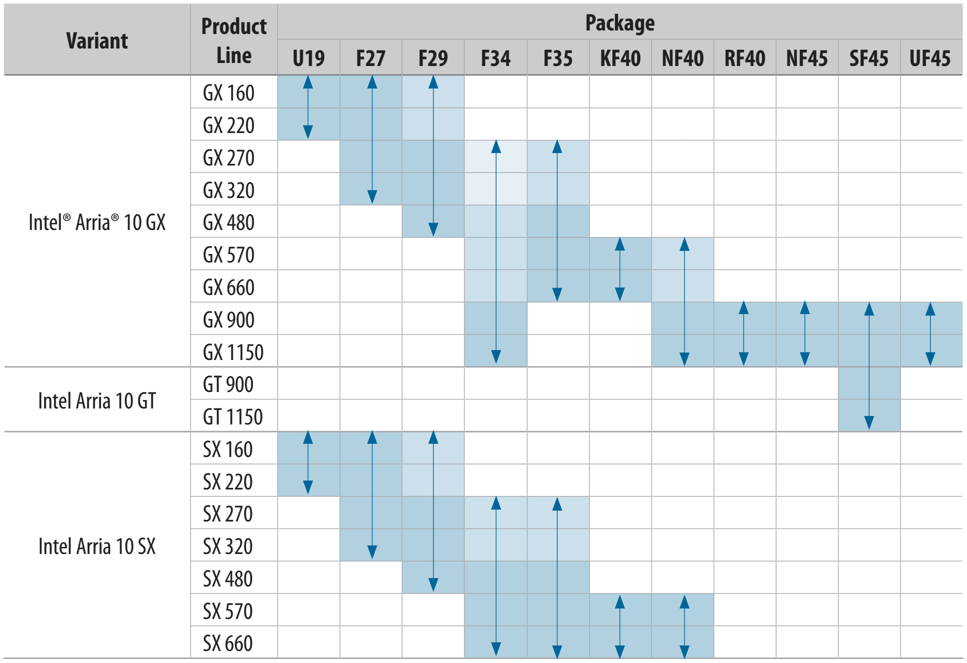
I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

# I/O Vertical Migration for Intel Arria 10 Devices

### Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.



| Variant | Product Line | Package | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | U19 | F27 | F29 | F34 | F35 | KF40 | NF40 | RF40 | NF45 | SF45 | UF45 |
| Intel® Arria® 10 GX | GX 160 | ▨ | ▨ | ▨ | | | | | | | | |
| | GX 220 | ▨ | ▨ | ▨ | | | | | | | | |
| | GX 270 | | ▨ | ▨ | ▨ | ▨ | | | | | | |
| | GX 320 | | ▨ | ▨ | ▨ | ▨ | | | | | | |
| | GX 480 | | | ▨ | ▨ | ▨ | | | | | | |
| | GX 570 | | | | ▨ | ▨ | ▨ | ▨ | | | | |
| | GX 660 | | | | ▨ | ▨ | ▨ | ▨ | | | | |
| | GX 900 | | | | ▨ | | | ▨ | ▨ | ▨ | ▨ | ▨ |
| | GX 1150 | | | | ▨ | | | ▨ | ▨ | ▨ | ▨ | ▨ |
| Intel Arria 10 GT | GT 900 | | | | | | | | | | ▨ | |
| | GT 1150 | | | | | | | | | | ▨ | |
| Intel Arria 10 SX | SX 160 | ▨ | ▨ | ▨ | | | | | | | | |
| | SX 220 | ▨ | ▨ | ▨ | | | | | | | | |
| | SX 270 | | ▨ | ▨ | ▨ | ▨ | | | | | | |
| | SX 320 | | ▨ | ▨ | ▨ | ▨ | | | | | | |
| | SX 480 | | | ▨ | ▨ | ▨ | | | | | | |
| | SX 570 | | | | ▨ | ▨ | ▨ | ▨ | | | | |
| | SX 660 | | | | ▨ | ▨ | ▨ | ▨ | | | | |

*Note:* To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

# Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.

## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

### Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

| Variant | Product Line | M20K | | MLAB | | Total RAM Bit (Kb) |
|---|---|---|---|---|---|---|
| | | Block | RAM Bit (Kb) | Block | RAM Bit (Kb) | |
| Intel Arria 10 GX | GX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | GX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | GX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | GX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | GX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | GX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | GX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |
| | GX 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GX 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 GT | GT 900 | 2,423 | 48,460 | 15,017 | 9,386 | 57,846 |
| | GT 1150 | 2,713 | 54,260 | 20,774 | 12,984 | 67,244 |
| Intel Arria 10 SX | SX 160 | 440 | 8,800 | 1,680 | 1,050 | 9,850 |
| | SX 220 | 587 | 11,740 | 2,703 | 1,690 | 13,430 |
| | SX 270 | 750 | 15,000 | 3,922 | 2,452 | 17,452 |
| | SX 320 | 891 | 17,820 | 4,363 | 2,727 | 20,547 |
| | SX 480 | 1,431 | 28,620 | 6,662 | 4,164 | 32,784 |
| | SX 570 | 1,800 | 36,000 | 8,153 | 5,096 | 41,096 |
| | SX 660 | 2,131 | 42,620 | 9,260 | 5,788 | 48,408 |

The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
    - Conventional integer mode equivalent to the general purpose PLL
    - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

### I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
    - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
    - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ($V_{OD}$) and programmable pre-emphasis

- Series ($R_S$) and parallel ($R_T$) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

External Memory Interface Spec Estimator
Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

### Table 20. Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

| Memory Standard | Rate Support | Ping Pong PHY Support | Maximum Frequency (MHz) |
|---|---|---|---|
| DDR4 SDRAM | Quarter rate | Yes | 1,067 |
| | | — | 1,200 |
| DDR3 SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 1,067 |
| | | — | 1,067 |
| DDR3L SDRAM | Half rate | Yes | 533 |
| | | — | 667 |
| | Quarter rate | Yes | 933 |
| | | — | 933 |
| LPDDR3 SDRAM | Half rate | — | 533 |
| | Quarter rate | — | 800 |

### Table 21. Memory Standards Supported by the Soft Memory Controller

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| RLDRAM 3 (11) | Quarter rate | 1,200 |
| QDR IV SRAM(11) | Quarter rate | 1,067 |
| QDR II SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ SRAM | Full rate | 333 |
| | Half rate | 633 |
| QDR II+ Xtreme SRAM | Full rate | 333 |
| | Half rate | 633 |

### Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

| Memory Standard | Rate Support | Maximum Frequency (MHz) |
|---|---|---|
| DDR4 SDRAM | Half rate | 1,200 |
| DDR3 SDRAM | Half rate | 1,067 |
| DDR3L SDRAM | Half rate | 933 |

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(11) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

**Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices**

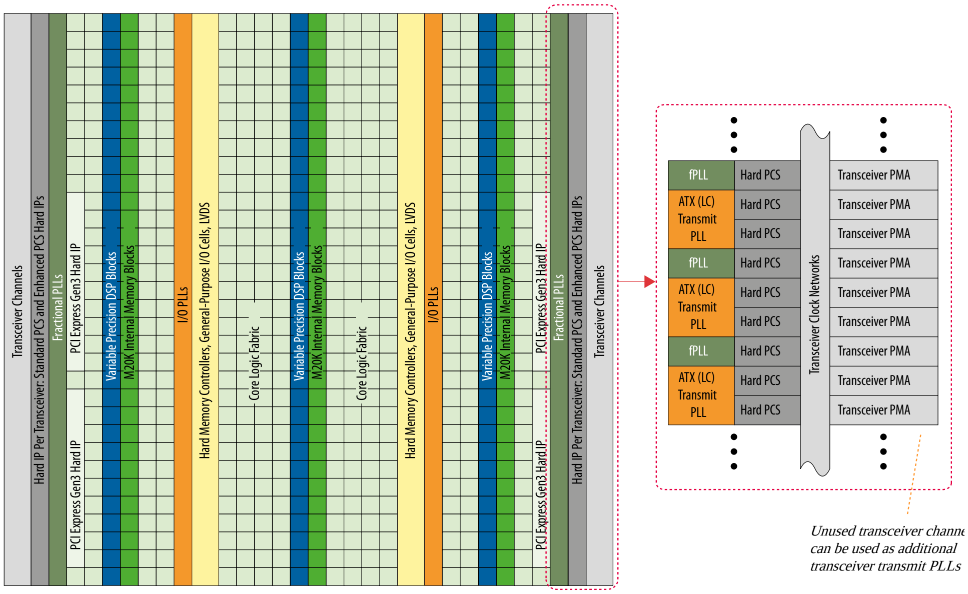
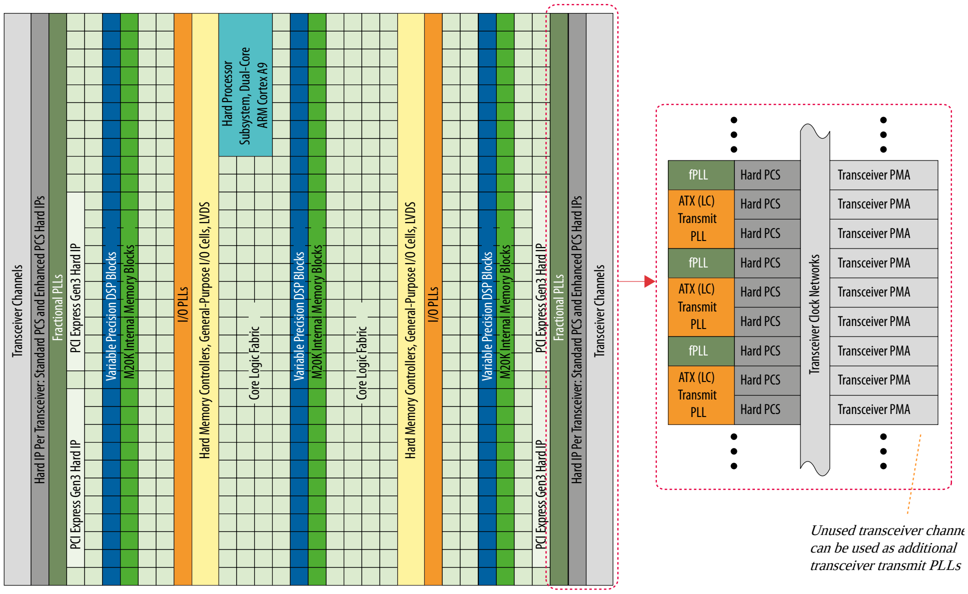


**Figure 8. Device Chip Overview for Intel Arria 10 SX Devices**



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.

Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

### Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices

| Feature | Capability |
|---|---|
| Chip-to-Chip Data Rates | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices) |
| Backplane Support | Drive backplanes at data rates up to 12.5 Gbps |
| Optical Module Support | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4 |
| Cable Driving Support | SFP+ Direct Attach, PCI Express over cable, eSATA |
| Transmit Pre-Emphasis | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss |
| Continuous Time Linear Equalizer (CTLE) | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss |
| Decision Feedback Equalizer (DFE) | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments |
| Variable Gain Amplifier | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes |
| Altera Digital Adaptive Parametric Tuning (ADAPT) | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance |
| Advanced Transmit (ATX) PLL | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols |
| Fractional PLLs | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost |
| Digitally Assisted Analog CDR | Superior jitter tolerance with fast lock time |
| Dynamic Partial Reconfiguration | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility |
| Multiple PCS-PMA and PCS-PLD interface widths | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

| PCS | Description |
|---|---|
| Standard PCS | • Operates at a data rate up to 12 Gbps<br>• Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS<br>• Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | • Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA<br>• Handles data transfer to and from the FPGA fabric<br>• Handles data transfer internally to and from the PMA<br>• Provides frequency compensation<br>• Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | • Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates<br>• Provides support for PIPE 3.0 features<br>• Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

### Related Information

- PCIe Gen1, Gen2, and Gen3 Hard IP on page 26
- Interlaken Support on page 26
- 10 Gbps Ethernet Support on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |

***continued...***

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|---|---|---|---|
| CPRI 6.0 (64B/66B) | 0.6144 to 10.1376 | Native PHY | Enhanced PCS |
| CPRI 4.2 (8B/10B) | 0.6144 to 9.8304 | Native PHY | Standard PCS |
| OBSAI RP3 v4.2 | 0.6144 to 6.144 | Native PHY | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143(12) to 2.97 | Native PHY | Standard PCS |

### Related Information

Intel Arria 10 Transceiver PHY User Guide
Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

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(12) The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I$^2$C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

### Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps)(13) | Decompression | Design Security(14) | Partial Reconfiguration(15) | Remote System Update |
|---|---|---|---|---|---|---|---|
| JTAG | 1 bit | 33 | 33 | — | — | Yes(16) | — |
| Active Serial (AS) through the EPCQ-L configuration device | 1 bit,<br>4 bits | 100 | 400 | Yes | Yes | Yes(16) | Yes |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit | 100 | 100 | Yes | Yes | Yes(16) | Parallel Flash Loader (PFL) IP core |

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(13) Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

(14) Encryption and compression cannot be used simultaneously.

(15) Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

(16) Partial configuration can be performed only when it is configured as internal host.

The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core $V_{CC}$ while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes |
|---|---|
| 2018.04.09 | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|---|---|---|
| January 2018 | 2018.01.17 | • Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.<br>• Updated maximum frequency supported for half rate QDRII and QDRII + SRAM to 633 MHz in *Memory Standards Supported by the Soft Memory Controller* table.<br>• Updated transceiver backplane capability to 12.5 Gbps.<br>• Removed transceiver speed grade 5 in *Sample Ordering Core and Available Options for Intel Arria 10 GX Devices* figure. |

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| Date | Version | Changes |
|---|---|---|
| | | • Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from *Sample Ordering Core and Available Options for Intel Arria 10 GT Devices* figure.<br>• Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.<br>• Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from *PMA Features of the Transceivers in Intel Arria 10 Devices* table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | • Corrected protocol names with "1588" to "IEEE 1588v2".<br>• Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.<br>• Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | • Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.<br>• Rebranded as Intel. |
| October 2016 | 2016.10.31 | • Removed package F36 from Intel Arria 10 GX devices.<br>• Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | • Updated the FPGA Configuration and HPS Booting topic.<br>• Remove $V_{CC}$ PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.<br>• Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.<br>• Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | • Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.<br>• Revised the state for Core clock networks in the Summary of Features topic.<br>• Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.<br>• Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.<br>• Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.<br>• Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.<br>• Changed transceiver parameters in the "Low Power Serial Transceivers" section.<br>• Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.<br>• Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.<br>• Changed the datarates for GT devices in the "PMA Features" section.<br>• Changed the datarates for GT devices in the "PCS Features" section. |

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