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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 339620  |
| Number of Logic Elements/Cells | 900000  |
| Total RAM Bits                 | 59234304  |
| Number of I/O                  | 768   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.87V ~ 0.98V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | -40°C ~ 100°C (TJ)  |
| Package / Case                 | 1932-BBGA, FCBGA  |
| Supplier Device Package        | 1932-FCBGA (45x45)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/10ax090n1f45i1sg">https://www.e-xfl.com/product-detail/intel/10ax090n1f45i1sg</a> |



## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market                | Applications  |
|-----------------------|---|
| Wireless              | <ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>   |
| Wireline              | <ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>            |
| Broadcast             | <ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul> |
| Computing and Storage | <ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>   |
| Medical               | <ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>   |
| Military              | <ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>          |

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Key Advantages of Intel Arria 10 Devices

**Table 2. Key Advantages of the Intel Arria 10 Device Family**

| Advantage  | Supporting Feature  |
|--|---|
| Enhanced core architecture   | <ul style="list-style-type: none"><li>Built on TSMC's 20 nm process technology</li><li>60% higher performance than the previous generation of mid-range FPGAs</li><li>15% higher performance than the fastest previous-generation FPGA</li></ul>  |
| High-bandwidth integrated transceivers   | <ul style="list-style-type: none"><li>Short-reach rates up to 25.8 Gigabits per second (Gbps)</li><li>Backplane capability up to 12.5 Gbps</li><li>Integrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)</li></ul>   |
| Improved logic integration and hard IP blocks  | <ul style="list-style-type: none"><li>8-input adaptive logic module (ALM)</li><li>Up to 65.6 megabits (Mb) of embedded memory</li><li>Variable-precision digital signal processing (DSP) blocks</li><li>Fractional synthesis phase-locked loops (PLLs)</li><li>Hard PCI Express Gen3 IP blocks</li><li>Hard memory controllers and PHY up to 2,400 Megabits per second (Mbps)</li></ul> |
| Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor | <ul style="list-style-type: none"><li>Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)</li><li>Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric</li></ul>  |
| Advanced power savings   | <ul style="list-style-type: none"><li>Comprehensive set of advanced power saving features</li><li>Power-optimized MultiTrack routing and core architecture</li><li>Up to 40% lower power compared to previous generation of mid-range FPGAs</li><li>Up to 60% lower power compared to previous generation of high-end FPGAs</li></ul>   |

## Summary of Intel Arria 10 Features

**Table 3. Summary of Features for Intel Arria 10 Devices**

| Feature                      | Description   |
|------------------------------|---|
| Technology                   | <ul style="list-style-type: none"><li>TSMC's 20-nm SoC process technology</li><li>Allows operation at a lower <math>V_{CC}</math> level of 0.82 V instead of the 0.9 V standard <math>V_{CC}</math> core voltage</li></ul>  |
| Packaging                    | <ul style="list-style-type: none"><li>1.0 mm ball-pitch FINELINE BGA packaging</li><li>0.8 mm ball-pitch Ultra FINELINE BGA packaging</li><li>Multiple devices with identical package footprints for seamless migration between different FPGA densities</li><li>Devices with compatible package footprints allow migration to next generation high-end Stratix® 10 devices</li><li>RoHS, leaded<sup>(1)</sup>, and lead-free (Pb-free) options</li></ul> |
| High-performance FPGA fabric | <ul style="list-style-type: none"><li>Enhanced 8-input ALM with four registers</li><li>Improved multi-track routing architecture to reduce congestion and improve compilation time</li><li>Hierarchical core clocking architecture</li><li>Fine-grained partial reconfiguration</li></ul>   |
| Internal memory blocks       | <ul style="list-style-type: none"><li>M20K—20-Kb memory blocks with hard error correction code (ECC)</li><li>Memory logic array block (MLAB)—640-bit memory</li></ul>   |
| continued...                 |   |

(1) Contact Intel for availability.



| Feature                           | Description  |   |
|-----------------------------------|--|---|
| Embedded Hard IP blocks           | Variable-precision DSP   | <ul style="list-style-type: none"><li>Native support for signal processing precision levels from 18 x 19 to 54 x 54</li><li>Native support for 27 x 27 multiplier mode</li><li>64-bit accumulator and cascade for systolic finite impulse responses (FIRs)</li><li>Internal coefficient memory banks</li><li>Padder/subtractor for improved efficiency</li><li>Additional pipeline register to increase performance and reduce power</li><li>Supports floating point arithmetic:<ul style="list-style-type: none"><li>Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.</li><li>Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.</li><li>Dynamic accumulator reset control.</li><li>Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.</li></ul></li></ul> |
|                                   | Memory controller  | DDR4, DDR3, and DDR3L   |
|                                   | PCI Express*   | PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port   |
|                                   | Transceiver I/O  | <ul style="list-style-type: none"><li>10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)</li><li>PCS hard IPs that support:<ul style="list-style-type: none"><li>10-Gbps Ethernet (10GbE)</li><li>PCIe PIPE interface</li><li>Interlaken</li><li>Gbps Ethernet (GbE)</li><li>Common Public Radio Interface (CPRI) with deterministic latency support</li><li>Gigabit-capable passive optical network (GPON) with fast lock-time support</li></ul></li><li>13.5G JESD204b</li><li>8B/10B, 64B/66B, 64B/67B encoders and decoders</li><li>Custom mode support for proprietary protocols</li></ul>  |
| Core clock networks               | <ul style="list-style-type: none"><li>Up to 800 MHz fabric clocking, depending on the application:<ul style="list-style-type: none"><li>667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface</li><li>800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface</li></ul></li><li>Global, regional, and peripheral clock networks</li><li>Clock networks that are not used can be gated to reduce dynamic power</li></ul>   |   |
| Phase-locked loops (PLLs)         | <ul style="list-style-type: none"><li>High-resolution fractional synthesis PLLs:<ul style="list-style-type: none"><li>Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)</li><li>Support integer mode and fractional mode</li><li>Fractional mode support with third-order delta-sigma modulation</li></ul></li><li>Integer PLLs:<ul style="list-style-type: none"><li>Adjacent to general purpose I/Os</li><li>Support external memory and LVDS interfaces</li></ul></li></ul> |   |
| FPGA General-purpose I/Os (GPIOs) | <ul style="list-style-type: none"><li>1.6 Gbps LVDS—every pair can be configured as receiver or transmitter</li><li>On-chip termination (OCT)</li><li>1.2 V to 3.0 V single-ended LVTTTL/LVCMOS interfacing</li></ul>  |   |
| External Memory Interface         | <ul style="list-style-type: none"><li>Hard memory controller—DDR4, DDR3, and DDR3L support<ul style="list-style-type: none"><li>DDR4—speeds up to 1,200 MHz/2,400 Mbps</li><li>DDR3—speeds up to 1,067 MHz/2,133 Mbps</li></ul></li><li>Soft memory controller—provides support for RLDRAM 3<sup>(2)</sup>, QDR IV<sup>(2)</sup>, and QDR II+</li></ul>  |   |
| continued...                      |  |   |



| Feature                                 | Description   |  |
|---|---|--|
| Low-power serial transceivers           | <ul style="list-style-type: none"><li>Continuous operating range:<ul style="list-style-type: none"><li>Intel Arria 10 GX—1 Gbps to 17.4 Gbps</li><li>Intel Arria 10 GT—1 Gbps to 25.8 Gbps</li></ul></li><li>Backplane support:<ul style="list-style-type: none"><li>Intel Arria 10 GX—up to 12.5</li><li>Intel Arria 10 GT—up to 12.5</li></ul></li><li>Extended range down to 125 Mbps with oversampling</li><li>ATX transmit PLLs with user-configurable fractional synthesis capability</li><li>Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module</li><li>Adaptive linear and decision feedback equalization</li><li>Transmitter pre-emphasis and de-emphasis</li><li>Dynamic partial reconfiguration of individual transceiver channels</li></ul> |  |
| HPS<br>(Intel Arria 10 SX devices only) | Processor and system  | <ul style="list-style-type: none"><li>Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability</li><li>256 KB on-chip RAM and 64 KB on-chip ROM</li><li>System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers</li><li>Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)</li><li>ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage</li></ul>   |
|   | External interfaces   | <ul style="list-style-type: none"><li>Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller</li><li>Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I<sup>2</sup>C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)</li></ul>   |
|   | Interconnects to core   | <ul style="list-style-type: none"><li>High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write</li><li>HPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa</li><li>Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port</li><li>FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller</li></ul> |
| Configuration                           | <ul style="list-style-type: none"><li>Tamper protection—comprehensive design protection to protect your valuable IP investments</li><li>Enhanced 256-bit advanced encryption standard (AES) design security with authentication</li><li>Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3</li></ul>   |  |
| continued...                            |   |  |

<sup>(2)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





## Maximum Resources

**Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices**

| Resource                     |                      | Product Line      |                   |
|------------------------------|----------------------|-------------------|-------------------|
|                              |                      | GT 900            | GT 1150           |
| Logic Elements (LE) (K)      |                      | 900               | 1,150             |
| ALM                          |                      | 339,620           | 427,200           |
| Register                     |                      | 1,358,480         | 1,708,800         |
| Memory (Kb)                  | M20K                 | 48,460            | 54,260            |
|                              | MLAB                 | 9,386             | 12,984            |
| Variable-precision DSP Block |                      | 1,518             | 1,518             |
| 18 x 19 Multiplier           |                      | 3,036             | 3,036             |
| PLL                          | Fractional Synthesis | 32                | 32                |
|                              | I/O                  | 16                | 16                |
| Transceiver                  | 17.4 Gbps            | 72 <sup>(5)</sup> | 72 <sup>(5)</sup> |
|                              | 25.8 Gbps            | 6                 | 6                 |
| GPIO <sup>(6)</sup>          |                      | 624               | 624               |
| LVDS Pair <sup>(7)</sup>     |                      | 312               | 312               |
| PCIe Hard IP Block           |                      | 4                 | 4                 |
| Hard Memory Controller       |                      | 16                | 16                |

### Related Information

#### Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

**Table 11. Package Plan for Intel Arria 10 GT Devices**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

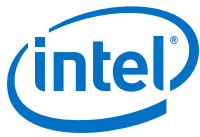
| Product Line | SF45<br>(45 mm x 45 mm, 1932-pin FBGA) |          |      |
|--------------|--|----------|------|
|              | 3 V I/O                                | LVDS I/O | XCVR |
| GT 900       | —                                      | 624      | 72   |
| GT 1150      | —                                      | 624      | 72   |

<sup>(5)</sup> If all 6 GT channels are in use, 12 of the GX channels are not usable.

<sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(7)</sup> Each LVDS I/O pair can be used as differential input or output.





| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 480       | —                                       | —           | —    | —                                       | —           | —    | 48                                      | 312         | 12   | 48                                       | 444         | 24   |
| SX 570       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |
| SX 660       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |          |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      |
|--------------|--|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                  | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR |
| SX 270       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 320       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 480       | 48                                       | 348      | 36   | —   | —        | —    | —   | —        | —    |
| SX 570       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |
| SX 660       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|         |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
|         | SX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|         | SX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|         | SX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|         | SX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | GX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | GX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | GX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | GX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | GX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | GX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |
|                   | GX 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GX 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GT 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 SX | SX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | SX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | SX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | SX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | SX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | SX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | SX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

**Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices**

| Variant           | Product Line | M20K  |              | MLAB   |              | Total RAM Bit (Kb) |
|-------------------|--------------|-------|--------------|--------|--------------|--------------------|
|                   |              | Block | RAM Bit (Kb) | Block  | RAM Bit (Kb) |                    |
| Intel Arria 10 GX | GX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | GX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | GX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | GX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | GX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | GX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | GX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |
|                   | GX 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GX 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 GT | GT 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GT 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 SX | SX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | SX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | SX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | SX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | SX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | SX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | SX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |

- Series ( $R_S$ ) and parallel ( $R_T$ ) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

## External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

### Related Information

#### [External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

## Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.



Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

**Table 23. PMA Features of the Transceivers in Intel Arria 10 Devices**

| Feature   | Capability   |
|---|--|
| Chip-to-Chip Data Rates                                 | 1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices)<br>1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)   |
| Backplane Support                                       | Drive backplanes at data rates up to 12.5 Gbps   |
| Optical Module Support                                  | SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4   |
| Cable Driving Support                                   | SFP+ Direct Attach, PCI Express over cable, eSATA  |
| Transmit Pre-Emphasis                                   | 4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss  |
| Continuous Time Linear Equalizer (CTLE)                 | Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss  |
| Decision Feedback Equalizer (DFE)                       | 7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments  |
| Variable Gain Amplifier                                 | Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes  |
| Altera Digital Adaptive Parametric Tuning (ADAPT)       | Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic |
| Precision Signal Integrity Calibration Engine (PreSICE) | Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance  |
| Advanced Transmit (ATX) PLL                             | Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols   |
| Fractional PLLs   | On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost   |
| Digitally Assisted Analog CDR                           | Superior jitter tolerance with fast lock time  |
| Dynamic Partial Reconfiguration                         | Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility   |
| Multiple PCS-PMA and PCS-PLD interface widths           | 8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency  |

## PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.



| PCS           | Description  |
|---------------|--|
| Standard PCS  | <ul style="list-style-type: none"> <li>Operates at a data rate up to 12 Gbps</li> <li>Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS</li> <li>Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.</li> </ul>   |
| Enhanced PCS  | <ul style="list-style-type: none"> <li>Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA</li> <li>Handles data transfer to and from the FPGA fabric</li> <li>Handles data transfer internally to and from the PMA</li> <li>Provides frequency compensation</li> <li>Performs channel bonding for multi-channel low skew applications</li> </ul> |
| PCIe Gen3 PCS | <ul style="list-style-type: none"> <li>Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates</li> <li>Provides support for PIPE 3.0 features</li> <li>Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed</li> </ul>  |

### Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol                                     | Data Rate (Gbps) | Transceiver IP              | PCS Support                    |
|--|------------------|-----------------------------|--------------------------------|
| PCIe Gen3 x1, x2, x4, x8                     | 8.0              | Native PHY (PIPE)           | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8                     | 5.0              | Native PHY (PIPE)           | Standard PCS                   |
| PCIe Gen1 x1, x2, x4, x8                     | 2.5              | Native PHY (PIPE)           | Standard PCS                   |
| 1000BASE-X Gigabit Ethernet                  | 1.25             | Native PHY                  | Standard PCS                   |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25             | Native PHY                  | Standard PCS                   |
| 10GBASE-R                                    | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-R with IEEE 1588v2                   | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-R with KR FEC                        | 10.3125          | Native PHY                  | Enhanced PCS                   |
| 10GBASE-KR and 1000BASE-X                    | 10.3125          | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS  |
| Interlaken (CEI-6G/11G)                      | 3.125 to 17.4    | Native PHY                  | Enhanced PCS                   |
| SFI-S/SFI-5.2                                | 11.2             | Native PHY                  | Enhanced PCS                   |
| 10G SDI                                      | 10.692           | Native PHY                  | Enhanced PCS                   |
| continued...                                 |                  |                             |                                |



| Protocol             | Data Rate (Gbps)              | Transceiver IP | PCS Support  |
|----------------------|-------------------------------|----------------|--------------|
| CPRI 6.0 (64B/66B)   | 0.6144 to 10.1376             | Native PHY     | Enhanced PCS |
| CPRI 4.2 (8B/10B)    | 0.6144 to 9.8304              | Native PHY     | Standard PCS |
| OBSAI RP3 v4.2       | 0.6144 to 6.144               | Native PHY     | Standard PCS |
| SD-SDI/HD-SDI/3G-SDI | 0.143 <sup>(12)</sup> to 2.97 | Native PHY     | Standard PCS |

### Related Information

#### [Intel Arria 10 Transceiver PHY User Guide](#)

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

## SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

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<sup>(12)</sup> The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.





**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/<br>Improvements                           | Description   |
|---|---|
| Increased performance and overdrive capability        | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.   |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.   |
| Flexible I/O sharing                                  | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul> |
| EMAC core   | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.  |
| On-chip memory  | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.  |
| ECC enhancements                                      | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.   |
| HPS to FPGA Interconnect Backbone                     | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.  |
| FPGA configuration and HPS booting                    | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.  |
| Security  | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).   |



## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core  $V_{CC}$  while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes  |
|------------------|--|
| 2018.04.09       | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date         | Version    | Changes   |
|--------------|------------|---|
| January 2018 | 2018.01.17 | <ul style="list-style-type: none"><li>• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li><li>• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.</li><li>• Updated transceiver backplane capability to 12.5 Gbps.</li><li>• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.</li></ul> |
| continued... |            |   |



| Date           | Version    | Changes  |
|----------------|------------|--|
| December 2015  | 2015.12.14 | <ul style="list-style-type: none"> <li>Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb.</li> <li>Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources.</li> </ul>  |
| November 2015  | 2015.11.02 | <ul style="list-style-type: none"> <li>Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660.</li> <li>Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in <b>Number of Multipliers in Intel Arria 10 Devices</b> table.</li> <li>Updated the available options for Arria 10 GX, GT, and SX.</li> <li>Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>.</li> </ul>   |
| June 2015      | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure.  |
| May 2015       | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller.   |
| May 2015       | 2015.05.04 | <ul style="list-style-type: none"> <li>Added support for 13.5G JESD204b in the Summary of Features table.</li> <li>Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic.</li> <li>Added a note to the table, Maximum Resource Counts for Arria 10 GT devices.</li> <li>Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic.</li> </ul>  |
| January 2015   | 2015.01.23 | <ul style="list-style-type: none"> <li>Added floating point arithmetic features in the Summary of Features table.</li> <li>Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb.</li> <li>Updated the table that lists the memory standards supported by Intel Arria 10 devices.</li> <li>Removed support for DDR3U, LPDDR3 SDRAM, RLDRAM 2, and DDR2.</li> <li>Moved RLDRAM 3 support from hard memory controller to soft memory controller. RLDRAM 3 support uses hard PHY with soft memory controller.</li> <li>Added soft memory controller support for QDR IV.</li> <li>Updated the maximum resource count table to include the number of hard memory controllers available in each device variant.</li> <li>Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps.</li> <li>Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz.</li> <li>Added a feature for fractional synthesis PLLs: PLL cascading.</li> <li>Updated the HPS programmable general-purpose I/Os from 54 to 62.</li> </ul> |
| September 2014 | 2014.09.30 | <ul style="list-style-type: none"> <li>Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX.</li> <li>Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660.</li> <li>Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150.</li> </ul>  |
| continued...   |            |  |