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Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	339620
Number of Logic Elements/Cells	900000
Total RAM Bits	59234304
Number of I/O	768
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10ax090n3f45i2sg

Contents

Feature		Description

Embedded Hard IP blocks	Variable-precision DSP	• Native support for signal processing precision levels from 18 x 19 to 54 x 54
		• Native support for 27 x 27 multiplier mode
		• 64-bit accumulator and cascade for systolic finite impulse responses (FIRs)
		• Internal coefficient memory banks
		• Preadder/subtractor for improved efficiency
		• Additional pipeline register to increase performance and reduce power
		• Supports floating point arithmetic:
		  — Perform multiplication, addition, subtraction, multiply-add, multiply-subtract, and complex multiplication.
		  — Supports multiplication with accumulation capability, cascade summation, and cascade subtraction capability.
		  — Dynamic accumulator reset control.
		  — Support direct vector dot and complex multiplication chaining multiply floating point DSP blocks.

	Memory controller	DDR4, DDR3, and DDR3L
	PCI Express*	PCI Express (PCIe*) Gen3 (x1, x2, x4, or x8), Gen2 (x1, x2, x4, or x8) and Gen1 (x1, x2, x4, or x8) hard IP with complete protocol stack, endpoint, and root port

	Transceiver I/O	• 10GBASE-KR/40GBASE-KR4 Forward Error Correction (FEC)
		• PCS hard IPs that support:
		  — 10-Gbps Ethernet (10GbE)
		  — PCIe PIPE interface
		  — Interlaken
		  — Gbps Ethernet (GbE)
		  — Common Public Radio Interface (CPRI) with deterministic latency support
		  — Gigabit-capable passive optical network (GPON) with fast lock-time support
		• 13.5G JESD204b
		• 8B/10B, 64B/66B, 64B/67B encoders and decoders
		• Custom mode support for proprietary protocols

Core clock networks		• Up to 800 MHz fabric clocking, depending on the application:
		  — 667 MHz external memory interface clocking with 2,400 Mbps DDR4 interface
		  — 800 MHz LVDS interface clocking with 1,600 Mbps LVDS interface
		• Global, regional, and peripheral clock networks
		• Clock networks that are not used can be gated to reduce dynamic power

Phase-locked loops (PLLs)		• High-resolution fractional synthesis PLLs:
		  — Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)
		  — Support integer mode and fractional mode
		  — Fractional mode support with third-order delta-sigma modulation
		• Integer PLLs:
		  — Adjacent to general purpose I/Os
		  — Support external memory and LVDS interfaces

FPGA General-purpose I/Os (GPIOs)		• 1.6 Gbps LVDS—every pair can be configured as receiver or transmitter • On-chip termination (OCT) • 1.2 V to 3.0 V single-ended LVTTL/LVCMOS interfacing

External Memory Interface		• Hard memory controller— DDR4, DDR3, and DDR3L support
		  — DDR4—speeds up to 1,200 MHz/2,400 Mbps
		  — DDR3—speeds up to 1,067 MHz/2,133 Mbps
		• Soft memory controller—provides support for RLDRAM 3[2], QDR IV[2], and QDR II+

<div align="right">continued...</div>

Feature	Description

Low-power serial transceivers	• Continuous operating range:
	  — Intel Arria 10 GX—1 Gbps to 17.4 Gbps
	  — Intel Arria 10 GT—1 Gbps to 25.8 Gbps
	• Backplane support:
	  — Intel Arria 10 GX—up to 12.5
	  — Intel Arria 10 GT—up to 12.5
	• Extended range down to 125 Mbps with oversampling
	• ATX transmit PLLs with user-configurable fractional synthesis capability
	• Electronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical module
	• Adaptive linear and decision feedback equalization
	• Transmitter pre-emphasis and de-emphasis
	• Dynamic partial reconfiguration of individual transceiver channels

Feature		Description
HPS (Intel Arria 10 SX devices only)	Processor and system	• Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability • 256 KB on-chip RAM and 64 KB on-chip ROM • System peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers • Security features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA) • ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage
	External interfaces	• Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controller • Communication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-GO (OTG) controllers, I²C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)
	Interconnects to core	• High-performance ARM AMBA* AXI bus bridges that support simultaneous read and write • HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versa • Configuration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration port • FPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller

Feature	Description
Configuration	• Tamper protection—comprehensive design protection to protect your valuable IP investments • Enhanced 256-bit advanced encryption standard (AES) design security with authentication • Configuration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3

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(2) Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

Feature	Description
	• Dynamic reconfiguration of the transceivers and PLLs • Fine-grained partial reconfiguration of the core fabric • Active Serial x4 Interface
Power management	• SmartVID • Low static power device options • Programmable Power Technology • Intel Quartus Prime integrated power analysis
Software and tools	• Intel Quartus Prime design suite • Transceiver toolkit • Platform Designer system integration tool • DSP Builder for Intel FPGAs • OpenCL™ support • Intel SoC FPGA Embedded Design Suite (EDS)

Related Information

Intel Arria 10 Transceiver PHY Overview
Provides details on Intel Arria 10 transceivers.

Intel Arria 10 Device Variants and Packages

Table 4.   Device Variants for the Intel Arria 10 Device Family

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: • 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability. • 25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

Intel FPGA Product Selector
Provides the latest information on Intel products.

Maximum Resources

Table 5.   Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	80,330	101,620	119,900	183,590
Register		246,040	321,320	406,480	479,600	734,360
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620
	MLAB	1,050	1,690	2,452	2,727	4,164
Variable-precision DSP Block		156	192	830	985	1,368
18 x 19 Multiplier		312	384	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO [3]		288	288	384	384	492
LVDS Pair [4]		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

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[3] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

[4] Each LVDS I/O pair can be used as differential input or output.
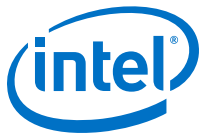
Available Options

Figure 2.   Sample Ordering Code and Available Options for Intel Arria 10 GT Devices

Operating Temperature
E   :   Extended (T$_J$ = 0° C to 100° C)

Package Type
F   :   FineLine BGA (FBGA), 1.0 mm pitch

Transceiver Count
S   :   72

Power Option
S   :   Standard

| 10A | T | 115 | S | 2 | F | 40 | I | 2 | S | G | ES |

Family Signature
10A : Intel Arria 10

Optional Suffix
Indicates specific device
options or shipment method
ES : Engineering sample

Family Variant
T   :   GT variant
       25.8 Gbps transceivers

RoHS
G   :   RoHS6
N   :   RoHS5   } Contact Intel
P   :   Leaded   for availability

Logic Density
090   :   900K logic elements
115   :   1,150K logic elements

Transceiver
Speed Grade
1 (fastest)
2

Package Code
45 :   1,932 pins, 45 mm x 45 mm

FPGA Fabric
Speed Grade
1 (fastest)
2
3

Maximum Resources

Table 10.   Maximum Resource Counts for Intel Arria 10 GT Devices

Resource		Product Line	
		GT 900	**GT 1150**
Logic Elements (LE) (K)		900	1,150
ALM		339,620	427,200
Register		1,358,480	1,708,800
Memory (Kb)	M20K	48,460	54,260
	MLAB	9,386	12,984
Variable-precision DSP Block		1,518	1,518
18 x 19 Multiplier		3,036	3,036
PLL	Fractional Synthesis	32	32
	I/O	16	16
Transceiver	17.4 Gbps	72 [5]	72 [5]
	25.8 Gbps	6	6
GPIO[6]		624	624
LVDS Pair[7]		312	312
PCIe Hard IP Block		4	4
Hard Memory Controller		16	16

Related Information

Intel Arria 10 GT Channel Usage
Configuring GT/GX channels in Intel Arria 10 GT devices.

Package Plan

Table 11.   Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	SF45 (45 mm × 45 mm, 1932-pin FBGA)		
	3 V I/O	**LVDS I/O**	**XCVR**
GT 900	—	624	72
GT 1150	—	624	72

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[5] If all 6 GT channels are in use, 12 of the GX channels are not usable.

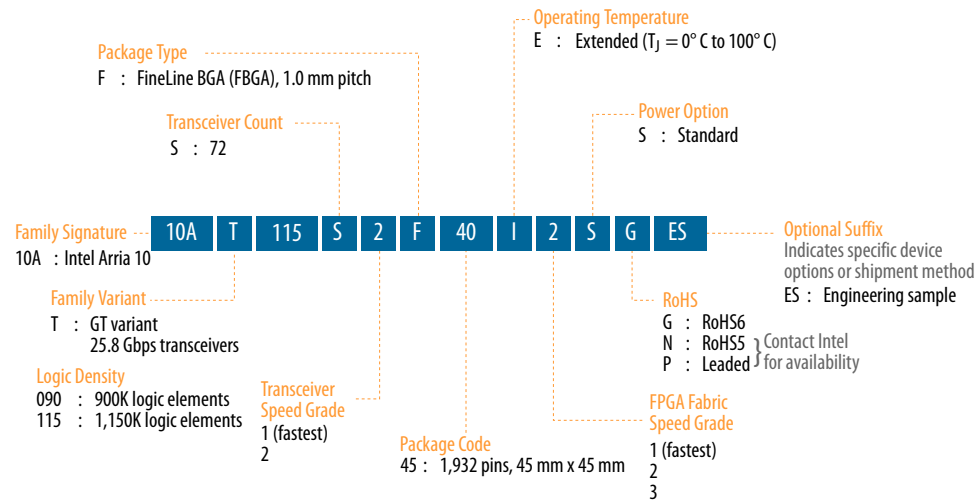[6] The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

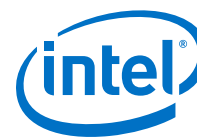[7] Each LVDS I/O pair can be used as differential input or output.
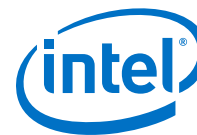
I/O Vertical Migration for Intel Arria 10 Devices

Figure 4.   Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.

- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.

- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.

- There may be nominal 0.15 mm package height difference between some product lines in the same package type.

- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

Variant	Product Line	Package										
		U19	F27	F29	F34	F35	KF40	NF40	RF40	NF45	SF45	UF45
Intel® Arria® 10 GX	GX 160											
	GX 220											
	GX 270											
	GX 320											
	GX 480											
	GX 570											
	GX 660											
	GX 900											
	GX 1150											
Intel Arria 10 GT	GT 900											
	GT 1150											
Intel Arria 10 SX	SX 160											
	SX 220											
	SX 270											
	SX 320											
	SX 480											
	SX 570											
	SX 660											

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.
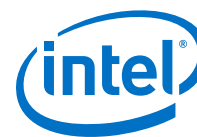
Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15.   Variable-Precision DSP Block Configurations for Intel Arria 10 Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 16.   Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
AIntel Arria 10 GX	GX 160	156	312	156	156	156
	GX 220	192	384	192	192	192
	GX 270	830	1,660	830	830	830
	GX 320	984	1,968	984	984	984
	GX 480	1,368	2,736	1,368	1,368	1,368
	GX 570	1,523	3,046	1,523	1,523	1,523
	GX 660	1,687	3,374	1,687	1,687	1,687
	GX 900	1,518	3,036	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 GT	GT 900	1,518	3,036	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 SX	SX 160	156	312	156	156	156
	SX 220	192	384	192	192	192
	SX 270	830	1,660	830	830	830

continued...

Embedded Memory Configurations for Single-port Mode

Table 19.   Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 [(10)]	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

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[(10)] Supported through software emulation and consumes additional MLAB blocks.
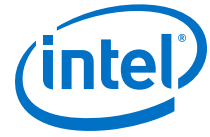
The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs

- Clock network delay compensation

- Zero-delay buffering

- Direct transmit clocking for transceivers

- Independently configurable into two modes:

  — Conventional integer mode equivalent to the general purpose PLL

  — Enhanced fractional mode with third order delta-sigma modulation

- PLL cascading

I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling

  — Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards

  — LVDS I/O banks that support up to 1.8 V I/O standards

- Support a wide range of single-ended and differential I/O interfaces

- LVDS speeds up to 1.6 Gbps

- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.

- Programmable bus hold and weak pull-up

- Programmable differential output voltage (V_{OD}) and programmable pre-emphasis

Table 20.   Memory Standards Supported by the Hard Memory Controller

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,200
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933
LPDDR3 SDRAM	Half rate	—	533
	Quarter rate	—	800

**Table 21.   Memory Standards Supported by the Soft Memory Controller**

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 [11]	Quarter rate	1,200
QDR IV SRAM[11]	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

Table 22.   Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

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[11] Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.
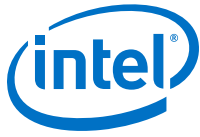
Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.

- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.

- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.

- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.

- Provides improved end-to-end datapath protection using ECC.

- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.
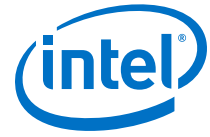
The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.

- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.

- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW

- 10 Gbps transceivers at as low as 168 mW

- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps

- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization

- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption

- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity

- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps

- All channels feature continuous data rate support up to the maximum rated speed

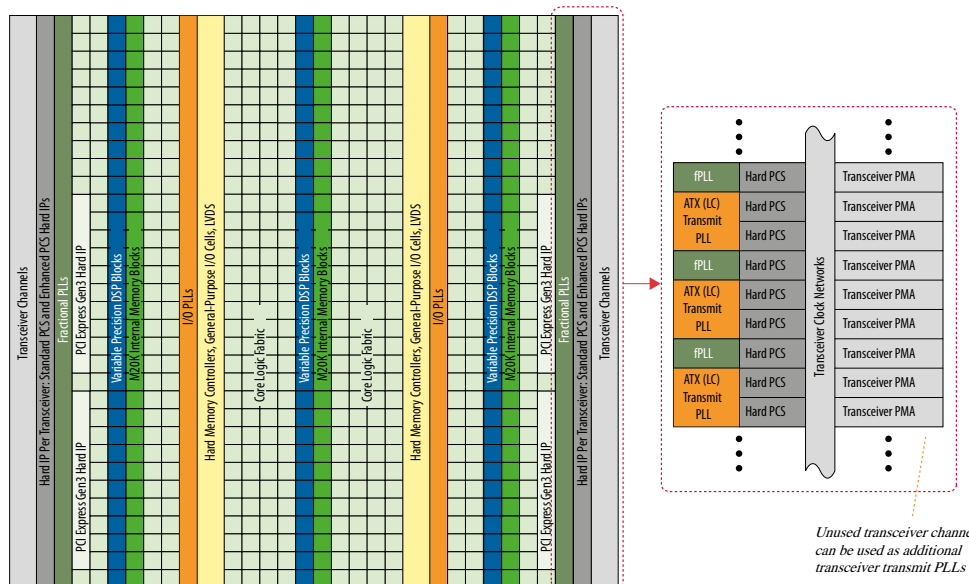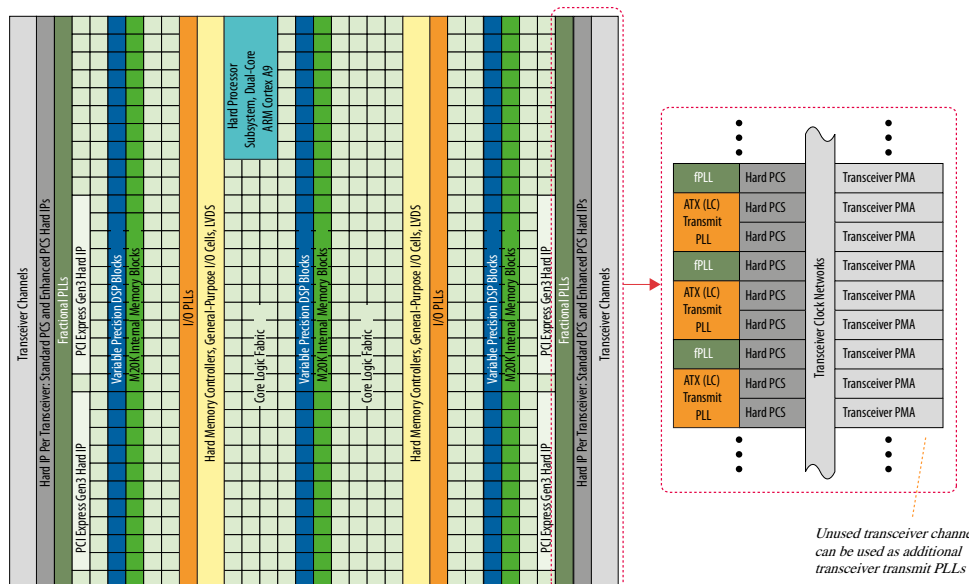**Figure 7.** **Device Chip Overview for Intel Arria 10 GX and GT Devices**

Unused transceiver channe can be used as additional transceiver transmit PLLs

Figure 8. **Device Chip Overview for Intel Arria 10 SX Devices**

Unused transceiver channe can be used as additional transceiver transmit PLLs

PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.
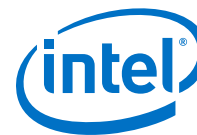
Each transceiver channel contains a channel PLL that can be used as the CMU PLL or clock data recovery (CDR) PLL. In CDR mode, the channel PLL recovers the receiver clock and data in the transceiver channel. Up to 80 independent data rates can be configured on a single Intel Arria 10 device.

Table 23.   PMA Features of the Transceivers in Intel Arria 10 Devices

Feature	Capability
Chip-to-Chip Data Rates	1 Gbps to 17.4 Gbps (Intel Arria 10 GX devices) 1 Gbps to 25.8 Gbps (Intel Arria 10 GT devices)
Backplane Support	Drive backplanes at data rates up to 12.5 Gbps
Optical Module Support	SFP+/SFP, XFP, CXP, QSFP/QSFP28, CFP/CFP2/CFP4
Cable Driving Support	SFP+ Direct Attach, PCI Express over cable, eSATA
Transmit Pre-Emphasis	4-tap transmit pre-emphasis and de-emphasis to compensate for system channel loss
Continuous Time Linear Equalizer (CTLE)	Dual mode, high-gain, and high-data rate, linear receive equalization to compensate for system channel loss
Decision Feedback Equalizer (DFE)	7-fixed and 4-floating tap DFE to equalize backplane channel loss in the presence of crosstalk and noisy environments
Variable Gain Amplifier	Optimizes the signal amplitude prior to the CDR sampling and operates in fixed and adaptive modes
Altera Digital Adaptive Parametric Tuning (ADAPT)	Fully digital adaptation engine to automatically adjust all link equalization parameters—including CTLE, DFE, and variable gain amplifier blocks—that provide optimal link margin without intervention from user logic
Precision Signal Integrity Calibration Engine (PreSICE)	Hardened calibration controller to quickly calibrate all transceiver control parameters on power-up, which provides the optimal signal integrity and jitter performance
Advanced Transmit (ATX) PLL	Low jitter ATX (LC tank based) PLLs with continuous tuning range to cover a wide range of standard and proprietary protocols
Fractional PLLs	On-chip fractional frequency synthesizers to replace on-board crystal oscillators and reduce system cost
Digitally Assisted Analog CDR	Superior jitter tolerance with fast lock time
Dynamic Partial Reconfiguration	Allows independent control of the Avalon memory-mapped interface of each transceiver channel for the highest transceiver flexibility
Multiple PCS-PMA and PCS-PLD interface widths	8-, 10-, 16-, 20-, 32-, 40-, or 64-bit interface widths for flexibility of deserialization width, encoding, and reduced latency

PCS Features

This table summarizes the Intel Arria 10 transceiver PCS features. You can use the transceiver PCS to support a wide range of protocols ranging from 1 Gbps to 25.8 Gbps.

| PCS	Description
Standard PCS	• Operates at a data rate up to 12 Gbps • Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS • Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.
Enhanced PCS	• Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA • Handles data transfer to and from the FPGA fabric • Handles data transfer internally to and from the PMA • Provides frequency compensation • Performs channel bonding for multi-channel low skew applications
PCIe Gen3 PCS	• Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates • Provides support for PIPE 3.0 features • Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed

Related Information

PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen3 x1, x2, x4, x8	8.0	Native PHY (PIPE)	Standard PCS and PCIe Gen3 PCS
PCIe Gen2 x1, x2, x4, x8	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4, x8	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS
1000BASE-X Gigabit Ethernet with IEEE 1588v2	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R with IEEE 1588v2	10.3125	Native PHY	Enhanced PCS
10GBASE-R with KR FEC	10.3125	Native PHY	Enhanced PCS
10GBASE-KR and 1000BASE-X	10.3125	1G/10GbE and 10GBASE-KR PHY	Standard PCS and Enhanced PCS
Interlaken (CEI-6G/11G)	3.125 to 17.4	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	11.2	Native PHY	Enhanced PCS
10G SDI	10.692	Native PHY	Enhanced PCS

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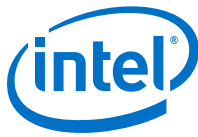
Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
CPRI 6.0 (64B/66B)	0.6144 to 10.1376	Native PHY	Enhanced PCS
CPRI 4.2 (8B/10B)	0.6144 to 9.8304	Native PHY	Standard PCS
OBSAI RP3 v4.2	0.6144 to 6.144	Native PHY	Standard PCS
SD-SDI/HD-SDI/3G-SDI	0.143[12] to 2.97	Native PHY	Standard PCS

Related Information

Intel Arria 10 Transceiver PHY User Guide

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor

- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard

- Extends the product life and revenue through in-field hardware and software updates

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[12] The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.

Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive

    — ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style

    — Superscalar, variable length, out-of-order pipeline with dynamic branch prediction

    — Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz

- Each processor core includes:

    — 32 KB of L1 instruction cache, 32 KB of L1 data cache

    — Single- and double-precision floating-point unit and NEON media engine

    — CoreSight debug and trace technology

    — Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)

- 512 KB of shared L2 cache

- 256 KB of scratch RAM

- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support

- Multiport Front End (MPFE) Scheduler interface to the hard memory controller

- 8-channel direct memory access (DMA) controller

- QSPI flash controller with SIO, DIO, QIO SPI Flash support

- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery

- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support

- 3 10/100/1000 Ethernet media access control (MAC) with DMA

- 2 USB On-the-Go (OTG) controllers with DMA

- 5 I^{2}C controllers (3 can be used by EMAC for MIO to external PHY)

- 2 UART 16550 Compatible controllers

- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)

- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os

- 7 general-purpose timers

- 4 watchdog timers

- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  — All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  — Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

Enhanced Configuration and Configuration via Protocol

Table 25.   Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) [13]	Decompression	Design Security [14]	Partial Reconfiguration [15]	Remote System Update
JTAG	1 bit	33	33	—	—	Yes [16]	—
Active Serial (AS) through the EPCQ-L configuration device	1 bit, 4 bits	100	400	Yes	Yes	Yes [16]	Yes
Passive serial (PS) through CPLD or external microcontroller	1 bit	100	100	Yes	Yes	Yes [16]	Parallel Flash Loader (PFL) IP core

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[13] Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

[14] Encryption and compression cannot be used simultaneously.

[15] Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

[16] Partial configuration can be performed only when it is configured as internal host.