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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |   |
|--------------------------------|---|
| Product Status                 | Active  |
| Number of LABs/CLBs            | 339620  |
| Number of Logic Elements/Cells | 900000  |
| Total RAM Bits                 | 59234304  |
| Number of I/O                  | 624   |
| Number of Gates                | -   |
| Voltage - Supply               | 0.87V ~ 0.98V   |
| Mounting Type                  | Surface Mount   |
| Operating Temperature          | 0°C ~ 100°C (TJ)  |
| Package / Case                 | 1932-BBGA, FCBGA  |
| Supplier Device Package        | 1932-FCBGA (45x45)  |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/10ax090s1f45e1sg">https://www.e-xfl.com/product-detail/intel/10ax090s1f45e1sg</a> |



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## Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

**Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices**

| Market                | Applications  |
|-----------------------|---|
| Wireless              | <ul style="list-style-type: none"> <li>• Channel and switch cards in remote radio heads</li> <li>• Mobile backhaul</li> </ul>   |
| Wireline              | <ul style="list-style-type: none"> <li>• 40G/100G muxponders and transponders</li> <li>• 100G line cards</li> <li>• Bridging</li> <li>• Aggregation</li> </ul>            |
| Broadcast             | <ul style="list-style-type: none"> <li>• Studio switches</li> <li>• Servers and transport</li> <li>• Videoconferencing</li> <li>• Professional audio and video</li> </ul> |
| Computing and Storage | <ul style="list-style-type: none"> <li>• Flash cache</li> <li>• Cloud computing servers</li> <li>• Server acceleration</li> </ul>   |
| Medical               | <ul style="list-style-type: none"> <li>• Diagnostic scanners</li> <li>• Diagnostic imaging</li> </ul>   |
| Military              | <ul style="list-style-type: none"> <li>• Missile guidance and control</li> <li>• Radar</li> <li>• Electronic warfare</li> <li>• Secure communications</li> </ul>          |

### Related Information

#### Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

| Resource                     |                      | Product Line |         |         |         |         |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
|                              |                      | GX 160       | GX 220  | GX 270  | GX 320  | GX 480  |
| Logic Elements (LE) (K)      |                      | 160          | 220     | 270     | 320     | 480     |
| ALM                          |                      | 61,510       | 80,330  | 101,620 | 119,900 | 183,590 |
| Register                     |                      | 246,040      | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb)                  | M20K                 | 8,800        | 11,740  | 15,000  | 17,820  | 28,620  |
|                              | MLAB                 | 1,050        | 1,690   | 2,452   | 2,727   | 4,164   |
| Variable-precision DSP Block |                      | 156          | 192     | 830     | 985     | 1,368   |
| 18 x 19 Multiplier           |                      | 312          | 384     | 1,660   | 1,970   | 2,736   |
| PLL                          | Fractional Synthesis | 6            | 6       | 8       | 8       | 12      |
|                              | I/O                  | 6            | 6       | 8       | 8       | 12      |
| 17.4 Gbps Transceiver        |                      | 12           | 12      | 24      | 24      | 36      |
| GPIO <sup>(3)</sup>          |                      | 288          | 288     | 384     | 384     | 492     |
| LVDS Pair <sup>(4)</sup>     |                      | 120          | 120     | 168     | 168     | 222     |
| PCIe Hard IP Block           |                      | 1            | 1       | 2       | 2       | 2       |
| Hard Memory Controller       |                      | 6            | 6       | 8       | 8       | 12      |

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.



**Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)**

| Resource                     |                      | Product Line |           |           |           |
|------------------------------|----------------------|--------------|-----------|-----------|-----------|
|                              |                      | GX 570       | GX 660    | GX 900    | GX 1150   |
| Logic Elements (LE) (K)      |                      | 570          | 660       | 900       | 1,150     |
| ALM                          |                      | 217,080      | 251,680   | 339,620   | 427,200   |
| Register                     |                      | 868,320      | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb)                  | M20K                 | 36,000       | 42,620    | 48,460    | 54,260    |
|                              | MLAB                 | 5,096        | 5,788     | 9,386     | 12,984    |
| Variable-precision DSP Block |                      | 1,523        | 1,687     | 1,518     | 1,518     |
| 18 x 19 Multiplier           |                      | 3,046        | 3,374     | 3,036     | 3,036     |
| PLL                          | Fractional Synthesis | 16           | 16        | 32        | 32        |
|                              | I/O                  | 16           | 16        | 16        | 16        |
| 17.4 Gbps Transceiver        |                      | 48           | 48        | 96        | 96        |
| GPIO <sup>(3)</sup>          |                      | 696          | 696       | 768       | 768       |
| LVDS Pair <sup>(4)</sup>     |                      | 324          | 324       | 384       | 384       |
| PCIe Hard IP Block           |                      | 2            | 2         | 4         | 4         |
| Hard Memory Controller       |                      | 16           | 16        | 16        | 16        |

## Package Plan

**Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |          |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |          |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |          |      |
|--------------|---|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                 | LVDS I/O | XCVR | 3 V I/O                                 | LVDS I/O | XCVR | 3 V I/O                                 | LVDS I/O | XCVR |
| GX 160       | 48                                      | 192      | 6    | 48                                      | 192      | 12   | 48                                      | 240      | 12   |
| GX 220       | 48                                      | 192      | 6    | 48                                      | 192      | 12   | 48                                      | 240      | 12   |
| GX 270       | —                                       | —        | —    | 48                                      | 192      | 12   | 48                                      | 312      | 12   |
| GX 320       | —                                       | —        | —    | 48                                      | 192      | 12   | 48                                      | 312      | 12   |
| GX 480       | —                                       | —        | —    | —                                       | —        | —    | 48                                      | 312      | 12   |



## Maximum Resources

**Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices**

| Resource                     |                      | Product Line      |                   |
|------------------------------|----------------------|-------------------|-------------------|
|                              |                      | GT 900            | GT 1150           |
| Logic Elements (LE) (K)      |                      | 900               | 1,150             |
| ALM                          |                      | 339,620           | 427,200           |
| Register                     |                      | 1,358,480         | 1,708,800         |
| Memory (Kb)                  | M20K                 | 48,460            | 54,260            |
|                              | MLAB                 | 9,386             | 12,984            |
| Variable-precision DSP Block |                      | 1,518             | 1,518             |
| 18 x 19 Multiplier           |                      | 3,036             | 3,036             |
| PLL                          | Fractional Synthesis | 32                | 32                |
|                              | I/O                  | 16                | 16                |
| Transceiver                  | 17.4 Gbps            | 72 <sup>(5)</sup> | 72 <sup>(5)</sup> |
|                              | 25.8 Gbps            | 6                 | 6                 |
| GPIO <sup>(6)</sup>          |                      | 624               | 624               |
| LVDS Pair <sup>(7)</sup>     |                      | 312               | 312               |
| PCIe Hard IP Block           |                      | 4                 | 4                 |
| Hard Memory Controller       |                      | 16                | 16                |

### Related Information

#### Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

## Package Plan

**Table 11. Package Plan for Intel Arria 10 GT Devices**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | SF45<br>(45 mm x 45 mm, 1932-pin FBGA) |          |      |
|--------------|--|----------|------|
|              | 3 V I/O                                | LVDS I/O | XCVR |
| GT 900       | —                                      | 624      | 72   |
| GT 1150      | —                                      | 624      | 72   |

<sup>(5)</sup> If all 6 GT channels are in use, 12 of the GX channels are not usable.

<sup>(6)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(7)</sup> Each LVDS I/O pair can be used as differential input or output.



| Product Line | U19<br>(19 mm × 19 mm,<br>484-pin UBGA) |             |      | F27<br>(27 mm × 27 mm,<br>672-pin FBGA) |             |      | F29<br>(29 mm × 29 mm,<br>780-pin FBGA) |             |      | F34<br>(35 mm × 35 mm,<br>1152-pin FBGA) |             |      |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
|              | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                              | LVDS<br>I/O | XCVR | 3 V<br>I/O                               | LVDS<br>I/O | XCVR |
| SX 480       | —                                       | —           | —    | —                                       | —           | —    | 48                                      | 312         | 12   | 48                                       | 444         | 24   |
| SX 570       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |
| SX 660       | —                                       | —           | —    | —                                       | —           | —    | —                                       | —           | —    | 48                                       | 444         | 24   |

**Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35<br>(35 mm × 35 mm,<br>1152-pin FBGA) |          |      | KF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      | NF40<br>(40 mm × 40 mm,<br>1517-pin FBGA) |          |      |
|--------------|--|----------|------|---|----------|------|---|----------|------|
|              | 3 V I/O                                  | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR | 3 V I/O                                   | LVDS I/O | XCVR |
| SX 270       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 320       | 48                                       | 336      | 24   | —   | —        | —    | —   | —        | —    |
| SX 480       | 48                                       | 348      | 36   | —   | —        | —    | —   | —        | —    |
| SX 570       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |
| SX 660       | 48                                       | 348      | 36   | 96  | 600      | 36   | 48  | 540      | 48   |

#### Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.





Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

**Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices**

| Usage Example   | Multiplier Size (Bit)           | DSP Block Resources |
|---|---------------------------------|---------------------|
| Medium precision fixed point                            | Two 18 x 19                     | 1                   |
| High precision fixed or Single precision floating point | One 27 x 27                     | 1                   |
| Fixed point FFTs  | One 19 x 36 with external adder | 1                   |
| Very high precision fixed point                         | One 36 x 36 with external adder | 2                   |
| Double precision floating point                         | One 54 x 54 with external adder | 4                   |

**Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|-------------------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|                   |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
| Intel Arria 10 GX | GX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | GX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | GX 270       | 830                          | 1,660   | 830                | 830                               | 830   |
|                   | GX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|                   | GX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|                   | GX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|                   | GX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |
|                   | GX 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GX 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
|                   | GT 1150      | 1,518                        | 3,036   | 1,518              | 1,518                             | 1,518   |
| Intel Arria 10 SX | SX 160       | 156                          | 312   | 156                | 156                               | 156   |
|                   | SX 220       | 192                          | 384   | 192                | 192                               | 192   |
|                   | SX 270       | 830                          | 1,660   | 830                | 830                               | 830   |

*continued...*



| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator |                    | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|---------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
|         |              |                              | 18 x 19 Multiplier                                    | 27 x 27 Multiplier |                                   |   |
|         | SX 320       | 984                          | 1,968   | 984                | 984                               | 984   |
|         | SX 480       | 1,368                        | 2,736   | 1,368              | 1,368                             | 1,368   |
|         | SX 570       | 1,523                        | 3,046   | 1,523              | 1,523                             | 1,523   |
|         | SX 660       | 1,687                        | 3,374   | 1,687              | 1,687                             | 1,687   |

**Table 17. Resources for Floating-Point Arithmetic in Intel Arria 10 Devices**

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant           | Product Line | Variable-precision DSP Block | Single Precision Floating-Point Multiplication Mode | Single-Precision Floating-Point Adder Mode | Single-Precision Floating-Point Multiply Accumulate Mode | Peak Giga Floating-Point Operations per Second (GFLOPs) |
|-------------------|--------------|------------------------------|---|--|--|---|
| Intel Arria 10 GX | GX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | GX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | GX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | GX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | GX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | GX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | GX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |
|                   | GX 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GX 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 GT | GT 900       | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
|                   | GT 1150      | 1,518                        | 1,518   | 1,518                                      | 1,518  | 1,366   |
| Intel Arria 10 SX | SX 160       | 156                          | 156   | 156  | 156  | 140   |
|                   | SX 220       | 192                          | 192   | 192  | 192  | 173   |
|                   | SX 270       | 830                          | 830   | 830  | 830  | 747   |
|                   | SX 320       | 984                          | 984   | 984  | 984  | 886   |
|                   | SX 480       | 1,369                        | 1,368   | 1,368                                      | 1,368  | 1,231   |
|                   | SX 570       | 1,523                        | 1,523   | 1,523                                      | 1,523  | 1,371   |
|                   | SX 660       | 1,687                        | 1,687   | 1,687                                      | 1,687  | 1,518   |

## Embedded Memory Blocks

The embedded memory blocks in the devices are flexible and designed to provide an optimal amount of small- and large-sized memory arrays to fit your design requirements.



## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

**Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices**

| Variant           | Product Line | M20K  |              | MLAB   |              | Total RAM Bit (Kb) |
|-------------------|--------------|-------|--------------|--------|--------------|--------------------|
|                   |              | Block | RAM Bit (Kb) | Block  | RAM Bit (Kb) |                    |
| Intel Arria 10 GX | GX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | GX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | GX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | GX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | GX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | GX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | GX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |
|                   | GX 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GX 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 GT | GT 900       | 2,423 | 48,460       | 15,017 | 9,386        | 57,846             |
|                   | GT 1150      | 2,713 | 54,260       | 20,774 | 12,984       | 67,244             |
| Intel Arria 10 SX | SX 160       | 440   | 8,800        | 1,680  | 1,050        | 9,850              |
|                   | SX 220       | 587   | 11,740       | 2,703  | 1,690        | 13,430             |
|                   | SX 270       | 750   | 15,000       | 3,922  | 2,452        | 17,452             |
|                   | SX 320       | 891   | 17,820       | 4,363  | 2,727        | 20,547             |
|                   | SX 480       | 1,431 | 28,620       | 6,662  | 4,164        | 32,784             |
|                   | SX 570       | 1,800 | 36,000       | 8,153  | 5,096        | 41,096             |
|                   | SX 660       | 2,131 | 42,620       | 9,260  | 5,788        | 48,408             |

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits)       | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB         | 32                 | x16, x18, or x20   |
|              | 64 <sup>(10)</sup> | x8, x9, x10        |
| M20K         | 512                | x40, x32           |
|              | 1K                 | x20, x16           |
|              | 2K                 | x10, x8            |
|              | 4K                 | x5, x4             |
|              | 8K                 | x2                 |
|              | 16K                | x1                 |

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

---

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

## I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

#### **Related Information**

[PCS Features](#) on page 30

## **Low Power Serial Transceivers**

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed



**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/<br>Improvements                           | Description   |
|---|---|
| Increased performance and overdrive capability        | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.   |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.   |
| Flexible I/O sharing                                  | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul> |
| EMAC core   | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.  |
| On-chip memory  | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.  |
| ECC enhancements                                      | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.   |
| HPS to FPGA Interconnect Backbone                     | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.  |
| FPGA configuration and HPS booting                    | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.<br>You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.  |
| Security  | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).   |



## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



## System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

## HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

## HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



## FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

## Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux\*, VxWorks\*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

## Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

### Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

### Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
  - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
  - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

## Enhanced Configuration and Configuration via Protocol

**Table 25. Configuration Schemes and Features of Intel Arria 10 Devices**

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme   | Data Width    | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update                |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG   | 1 bit         | 33                   | 33                                   | —             | —                               | Yes <sup>(16)</sup>                     | —                                   |
| Active Serial (AS) through the EPCQ-L configuration device   | 1 bit, 4 bits | 100                  | 400                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Yes                                 |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit         | 100                  | 100                                  | Yes           | Yes                             | Yes <sup>(16)</sup>                     | Parallel Flash Loader (PFL) IP core |

*continued...*

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(16)</sup> Partial configuration can be performed only when it is configured as internal host.



| Scheme   | Data Width           | Max Clock Rate (MHz) | Max Data Rate (Mbps) <sup>(13)</sup> | Decompression | Design Security <sup>(14)</sup> | Partial Reconfiguration <sup>(15)</sup> | Remote System Update |
|--|----------------------|----------------------|--------------------------------------|---------------|---------------------------------|---|----------------------|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits               | 100                  | 3200                                 | Yes           | Yes                             | Yes <sup>(17)</sup>                     | PFL IP core          |
|  | 16 bits              |                      |                                      | Yes           | Yes                             |   |                      |
|  | 32 bits              |                      |                                      | Yes           | Yes                             |   |                      |
| Configuration via HPS  | 16 bits              | 100                  | 3200                                 | Yes           | Yes                             | Yes <sup>(17)</sup>                     | —                    |
|  | 32 bits              |                      |                                      | Yes           | Yes                             |   |                      |
| Configuration via Protocol [CvP (PCIe*)]                             | x1, x2, x4, x8 lanes | —                    | 8000                                 | Yes           | Yes                             | Yes <sup>(16)</sup>                     | —                    |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

## SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

## Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

<sup>(13)</sup> Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

<sup>(14)</sup> Encryption and compression cannot be used simultaneously.

<sup>(15)</sup> Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

<sup>(17)</sup> Supported at a maximum clock rate of 100 MHz.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core  $V_{CC}$  while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes  |
|------------------|--|
| 2018.04.09       | Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date         | Version    | Changes   |
|--------------|------------|---|
| January 2018 | 2018.01.17 | <ul style="list-style-type: none"><li>• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li><li>• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.</li><li>• Updated transceiver backplane capability to 12.5 Gbps.</li><li>• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.</li></ul> |
| continued... |            |   |