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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	504
Number of Gates	-
Voltage - Supply	0.87V ~ 0.98V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10ax115h1f34i1sg



Contents

Intel® Arria® 10 Device Overview.....	3
Key Advantages of Intel Arria 10 Devices.....	4
Summary of Intel Arria 10 Features.....	4
Intel Arria 10 Device Variants and Packages.....	7
Intel Arria 10 GX.....	7
Intel Arria 10 GT.....	11
Intel Arria 10 SX.....	14
I/O Vertical Migration for Intel Arria 10 Devices.....	17
Adaptive Logic Module.....	17
Variable-Precision DSP Block.....	18
Embedded Memory Blocks.....	20
Types of Embedded Memory.....	21
Embedded Memory Capacity in Intel Arria 10 Devices.....	21
Embedded Memory Configurations for Single-port Mode.....	22
Clock Networks and PLL Clock Sources.....	22
Clock Networks.....	22
Fractional Synthesis and I/O PLLs.....	22
FPGA General Purpose I/O.....	23
External Memory Interface.....	24
Memory Standards Supported by Intel Arria 10 Devices.....	24
PCIe Gen1, Gen2, and Gen3 Hard IP.....	26
Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet.....	26
Interlaken Support.....	26
10 Gbps Ethernet Support.....	26
Low Power Serial Transceivers.....	27
Transceiver Channels.....	28
PMA Features.....	29
PCS Features.....	30
SoC with Hard Processor System.....	32
Key Advantages of 20-nm HPS.....	33
Features of the HPS.....	35
FPGA Configuration and HPS Booting.....	37
Hardware and Software Development.....	37
Dynamic and Partial Reconfiguration.....	37
Dynamic Reconfiguration.....	37
Partial Reconfiguration.....	37
Enhanced Configuration and Configuration via Protocol.....	38
SEU Error Detection and Correction.....	39
Power Management.....	39
Incremental Compilation.....	40
Document Revision History for Intel Arria 10 Device Overview.....	40



Key Advantages of Intel Arria 10 Devices

Table 2. Key Advantages of the Intel Arria 10 Device Family

Advantage	Supporting Feature
Enhanced core architecture	<ul style="list-style-type: none">Built on TSMC's 20 nm process technology60% higher performance than the previous generation of mid-range FPGAs15% higher performance than the fastest previous-generation FPGA
High-bandwidth integrated transceivers	<ul style="list-style-type: none">Short-reach rates up to 25.8 Gigabits per second (Gbps)Backplane capability up to 12.5 GbpsIntegrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)
Improved logic integration and hard IP blocks	<ul style="list-style-type: none">8-input adaptive logic module (ALM)Up to 65.6 megabits (Mb) of embedded memoryVariable-precision digital signal processing (DSP) blocksFractional synthesis phase-locked loops (PLLs)Hard PCI Express Gen3 IP blocksHard memory controllers and PHY up to 2,400 Megabits per second (Mbps)
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	<ul style="list-style-type: none">Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Advanced power savings	<ul style="list-style-type: none">Comprehensive set of advanced power saving featuresPower-optimized MultiTrack routing and core architectureUp to 40% lower power compared to previous generation of mid-range FPGAsUp to 60% lower power compared to previous generation of high-end FPGAs

Summary of Intel Arria 10 Features

Table 3. Summary of Features for Intel Arria 10 Devices

Feature	Description
Technology	<ul style="list-style-type: none">TSMC's 20-nm SoC process technologyAllows operation at a lower V_{CC} level of 0.82 V instead of the 0.9 V standard V_{CC} core voltage
Packaging	<ul style="list-style-type: none">1.0 mm ball-pitch FINELINE BGA packaging0.8 mm ball-pitch Ultra FINELINE BGA packagingMultiple devices with identical package footprints for seamless migration between different FPGA densitiesDevices with compatible package footprints allow migration to next generation high-end Stratix® 10 devicesRoHS, leaded⁽¹⁾, and lead-free (Pb-free) options
High-performance FPGA fabric	<ul style="list-style-type: none">Enhanced 8-input ALM with four registersImproved multi-track routing architecture to reduce congestion and improve compilation timeHierarchical core clocking architectureFine-grained partial reconfiguration
Internal memory blocks	<ul style="list-style-type: none">M20K—20-Kb memory blocks with hard error correction code (ECC)Memory logic array block (MLAB)—640-bit memory
continued...	

(1) Contact Intel for availability.



Feature	Description	
Low-power serial transceivers	<ul style="list-style-type: none">Continuous operating range:<ul style="list-style-type: none">Intel Arria 10 GX—1 Gbps to 17.4 GbpsIntel Arria 10 GT—1 Gbps to 25.8 GbpsBackplane support:<ul style="list-style-type: none">Intel Arria 10 GX—up to 12.5Intel Arria 10 GT—up to 12.5Extended range down to 125 Mbps with oversamplingATX transmit PLLs with user-configurable fractional synthesis capabilityElectronic Dispersion Compensation (EDC) support for XFP, SFP+, QSFP, and CFP optical moduleAdaptive linear and decision feedback equalizationTransmitter pre-emphasis and de-emphasisDynamic partial reconfiguration of individual transceiver channels	
HPS (Intel Arria 10 SX devices only)	Processor and system	<ul style="list-style-type: none">Dual-core ARM Cortex-A9 MPCore processor—1.2 GHz CPU with 1.5 GHz overdrive capability256 KB on-chip RAM and 64 KB on-chip ROMSystem peripherals—general-purpose timers, watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managersSecurity features—anti-tamper, secure boot, Advanced Encryption Standard (AES) and authentication (SHA)ARM CoreSight* JTAG debug access port, trace port, and on-chip trace storage
	External interfaces	<ul style="list-style-type: none">Hard memory interface—Hard memory controller (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash controller, NAND flash controller, direct memory access (DMA) controller, Secure Digital/MultiMediaCard (SD/MMC) controllerCommunication interface— 10/100/1000 Ethernet media access control (MAC), USB On-The-Go (OTG) controllers, I²C controllers, UART 16550, serial peripheral interface (SPI), and up to 62 HPS GPIO interfaces (48 direct-share I/Os)
	Interconnects to core	<ul style="list-style-type: none">High-performance ARM AMBA* AXI bus bridges that support simultaneous read and writeHPS-FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to issue transactions to slaves in the HPS, and vice versaConfiguration bridge that allows HPS configuration manager to configure the core logic via dedicated 32-bit configuration portFPGA-to-HPS SDRAM controller bridge—provides configuration interfaces for the multiport front end (MPFE) of the HPS SDRAM controller
Configuration	<ul style="list-style-type: none">Tamper protection—comprehensive design protection to protect your valuable IP investmentsEnhanced 256-bit advanced encryption standard (AES) design security with authenticationConfiguration via protocol (CvP) using PCIe Gen1, Gen2, or Gen3	
continued...		

⁽²⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F34 (35 mm × 35 mm, 1152-pin FBGA)			F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 270	48	336	24	48	336	24	—	—	—	—	—	—
GX 320	48	336	24	48	336	24	—	—	—	—	—	—
GX 480	48	444	24	48	348	36	—	—	—	—	—	—
GX 570	48	444	24	48	348	36	96	600	36	48	540	48
GX 660	48	444	24	48	348	36	96	600	36	48	540	48
GX 900	—	504	24	—	—	—	—	—	—	—	600	48
GX 1150	—	504	24	—	—	—	—	—	—	—	600	48

Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	RF40 (40 mm × 40 mm, 1517-pin FBGA)			NF45 (45 mm × 45 mm) 1932-pin FBGA)			SF45 (45 mm × 45 mm) 1932-pin FBGA)			UF45 (45 mm × 45 mm) 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 900	—	342	66	—	768	48	—	624	72	—	480	96
GX 1150	—	342	66	—	768	48	—	624	72	—	480	96

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 GT

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





Maximum Resources

Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

Resource		Product Line	
		GT 900	GT 1150
Logic Elements (LE) (K)		900	1,150
ALM		339,620	427,200
Register		1,358,480	1,708,800
Memory (Kb)	M20K	48,460	54,260
	MLAB	9,386	12,984
Variable-precision DSP Block		1,518	1,518
18 x 19 Multiplier		3,036	3,036
PLL	Fractional Synthesis	32	32
	I/O	16	16
Transceiver	17.4 Gbps	72 ⁽⁵⁾	72 ⁽⁵⁾
	25.8 Gbps	6	6
GPIO ⁽⁶⁾		624	624
LVDS Pair ⁽⁷⁾		312	312
PCIe Hard IP Block		4	4
Hard Memory Controller		16	16

Related Information

Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

Package Plan

Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	SF45 (45 mm x 45 mm, 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR
GT 900	—	624	72
GT 1150	—	624	72

⁽⁵⁾ If all 6 GT channels are in use, 12 of the GX channels are not usable.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁷⁾ Each LVDS I/O pair can be used as differential input or output.



Maximum Resources

Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687
18 x 19 Multiplier		312	384	1,660	1,970	2,736	3,046	3,374
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO ⁽⁸⁾		288	288	384	384	492	696	696
LVDS Pair ⁽⁹⁾		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

Package Plan

Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
continued...												

⁽⁸⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁹⁾ Each LVDS I/O pair can be used as differential input or output.



Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 480	—	—	—	—	—	—	48	312	12	48	444	24
SX 570	—	—	—	—	—	—	—	—	—	48	444	24
SX 660	—	—	—	—	—	—	—	—	—	48	444	24

Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	F35 (35 mm × 35 mm, 1152-pin FBGA)			KF40 (40 mm × 40 mm, 1517-pin FBGA)			NF40 (40 mm × 40 mm, 1517-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 270	48	336	24	—	—	—	—	—	—
SX 320	48	336	24	—	—	—	—	—	—
SX 480	48	348	36	—	—	—	—	—	—
SX 570	48	348	36	96	600	36	48	540	48
SX 660	48	348	36	96	600	36	48	540	48

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
Intel Arria 10 GX	GX 160	156	312	156	156	156
	GX 220	192	384	192	192	192
	GX 270	830	1,660	830	830	830
	GX 320	984	1,968	984	984	984
	GX 480	1,368	2,736	1,368	1,368	1,368
	GX 570	1,523	3,046	1,523	1,523	1,523
	GX 660	1,687	3,374	1,687	1,687	1,687
	GX 900	1,518	3,036	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 GT	GT 900	1,518	3,036	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 SX	SX 160	156	312	156	156	156
	SX 220	192	384	192	192	192
	SX 270	830	1,660	830	830	830

continued...

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 ⁽¹⁰⁾	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
 - Conventional integer mode equivalent to the general purpose PLL
 - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
 - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
 - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage (V_{OD}) and programmable pre-emphasis

- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Related Information

[External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,200
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933
LPDDR3 SDRAM	Half rate	—	533
	Quarter rate	—	800

Table 21. Memory Standards Supported by the Soft Memory Controller

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 ⁽¹¹⁾	Quarter rate	1,200
QDR IV SRAM ⁽¹¹⁾	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

Table 22. Memory Standards Supported by the HPS Hard Memory Controller

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

⁽¹¹⁾ Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



Related Information

[Intel Arria 10 Device Datasheet](#)

Lists the memory interface performance according to memory interface standards, rank or chip select configurations, and Intel Arria 10 device speed grades.

PCIe Gen1, Gen2, and Gen3 Hard IP

Intel Arria 10 devices contain PCIe hard IP that is designed for performance and ease-of-use:

- Includes all layers of the PCIe stack—transaction, data link and physical layers.
- Supports PCIe Gen3, Gen2, and Gen1 Endpoint and Root Port in x1, x2, x4, or x8 lane configuration.
- Operates independently from the core logic—optional configuration via protocol (CvP) allows the PCIe link to power up and complete link training in less than 100 ms while the Intel Arria 10 device completes loading the programming file for the rest of the FPGA.
- Provides added functionality that makes it easier to support emerging features such as Single Root I/O Virtualization (SR-IOV) and optional protocol extensions.
- Provides improved end-to-end datapath protection using ECC.
- Supports FPGA configuration via protocol (CvP) using PCIe at Gen3, Gen2, or Gen1 speed.

Related Information

[PCS Features](#) on page 30

Enhanced PCS Hard IP for Interlaken and 10 Gbps Ethernet

Interlaken Support

The Intel Arria 10 enhanced PCS hard IP provides integrated Interlaken PCS supporting rates up to 25.8 Gbps per lane.

The Interlaken PCS is based on the proven functionality of the PCS developed for Intel's previous generation FPGAs, which demonstrated interoperability with Interlaken ASSP vendors and third-party IP suppliers. The Interlaken PCS is present in every transceiver channel in Intel Arria 10 devices.

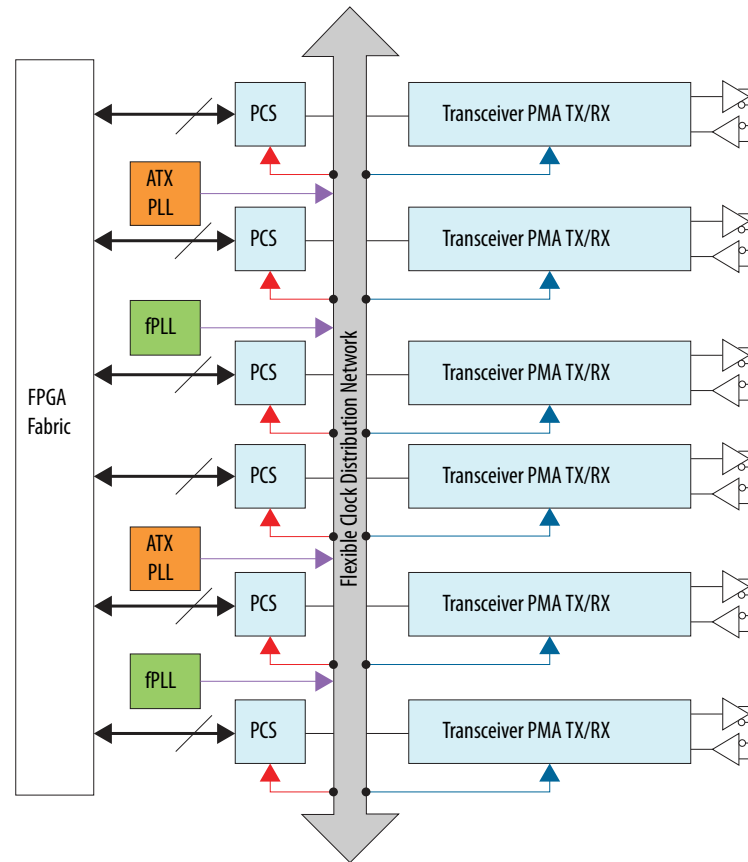
Related Information

[PCS Features](#) on page 30

10 Gbps Ethernet Support

The Intel Arria 10 enhanced PCS hard IP supports 10GBASE-R PCS compliant with IEEE 802.3 10 Gbps Ethernet (10GbE). The integrated hard IP support for 10GbE and the 10 Gbps transceivers save external PHY cost, board space, and system power.

Figure 6. Intel Arria 10 Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
CPRI 6.0 (64B/66B)	0.6144 to 10.1376	Native PHY	Enhanced PCS
CPRI 4.2 (8B/10B)	0.6144 to 9.8304	Native PHY	Standard PCS
OBSAI RP3 v4.2	0.6144 to 6.144	Native PHY	Standard PCS
SD-SDI/HD-SDI/3G-SDI	0.143 ⁽¹²⁾ to 2.97	Native PHY	Standard PCS

Related Information

[Intel Arria 10 Transceiver PHY User Guide](#)

Provides more information about the supported transceiver protocols and PHY IP, the PMA architecture, and the standard, enhanced, and PCIe Gen3 PCS architecture.

SoC with Hard Processor System

Each SoC device combines an FPGA fabric and a hard processor system (HPS) in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in these ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

⁽¹²⁾ The 0.143 Gbps data rate is supported using oversampling of user logic that you must implement in the FPGA fabric.



Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
 - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
 - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
 - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
 - 32 KB of L1 instruction cache, 32 KB of L1 data cache
 - Single- and double-precision floating-point unit and NEON media engine
 - CoreSight debug and trace technology
 - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I²C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



FPGA Configuration and HPS Booting

The FPGA fabric and HPS in the SoC FPGA must be powered at the same time. You can reduce the clock frequencies or gate the clocks to reduce dynamic power.

Once powered, the FPGA fabric and HPS can be configured independently thus providing you with more design flexibility:

- You can boot the HPS independently. After the HPS is running, the HPS can fully or partially reconfigure the FPGA fabric at any time under software control. The HPS can also configure other FPGAs on the board through the FPGA configuration controller.
- Configure the FPGA fabric first, and then boot the HPS from memory accessible to the FPGA fabric.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Platform Designer system integration tool in the Intel Quartus Prime software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Intel SoC FPGAs follows the same steps as those for other SoC devices from other manufacturers. Support for Linux*, VxWorks*, and other operating systems are available for the SoC FPGAs. For more information on the operating systems support availability, contact the Intel FPGA sales team.

You can begin device-specific firmware and software development on the Intel SoC FPGA Virtual Target. The Virtual Target is a fast PC-based functional simulation of a target development system—a model of a complete development board. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Dynamic and Partial Reconfiguration

The Intel Arria 10 devices support dynamic and partial reconfiguration. You can use dynamic and partial reconfiguration simultaneously to enable seamless reconfiguration of both the device core and transceivers.

Dynamic Reconfiguration

You can reconfigure the PMA and PCS blocks while the device continues to operate. This feature allows you to change the data rates, protocol, and analog settings of a channel in a transceiver bank without affecting on-going data transfer in other transceiver banks. This feature is ideal for applications that require dynamic multiprotocol or multirate support.

Partial Reconfiguration

Using partial reconfiguration, you can reconfigure some parts of the device while keeping the device in operation.



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
 - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
 - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

Enhanced Configuration and Configuration via Protocol

Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) ⁽¹³⁾	Decompression	Design Security ⁽¹⁴⁾	Partial Reconfiguration ⁽¹⁵⁾	Remote System Update
JTAG	1 bit	33	33	—	—	Yes ⁽¹⁶⁾	—
Active Serial (AS) through the EPCQ-L configuration device	1 bit, 4 bits	100	400	Yes	Yes	Yes ⁽¹⁶⁾	Yes
Passive serial (PS) through CPLD or external microcontroller	1 bit	100	100	Yes	Yes	Yes ⁽¹⁶⁾	Parallel Flash Loader (PFL) IP core

continued...

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁶⁾ Partial configuration can be performed only when it is configured as internal host.