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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	504
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FCBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/10ax115h3f34i2lg">https://www.e-xfl.com/product-detail/intel/10ax115h3f34i2lg</a>



Feature	Description
	<ul style="list-style-type: none"><li>Dynamic reconfiguration of the transceivers and PLLs</li><li>Fine-grained partial reconfiguration of the core fabric</li><li>Active Serial x4 Interface</li></ul>
Power management	<ul style="list-style-type: none"><li>SmartVID</li><li>Low static power device options</li><li>Programmable Power Technology</li><li>Intel Quartus Prime integrated power analysis</li></ul>
Software and tools	<ul style="list-style-type: none"><li>Intel Quartus Prime design suite</li><li>Transceiver toolkit</li><li>Platform Designer system integration tool</li><li>DSP Builder for Intel FPGAs</li><li>OpenCL™ support</li><li>Intel SoC FPGA Embedded Design Suite (EDS)</li></ul>

### Related Information

#### [Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

## Intel Arria 10 Device Variants and Packages

**Table 4. Device Variants for the Intel Arria 10 Device Family**

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: <ul style="list-style-type: none"><li>17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.</li><li>25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.</li></ul>
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

## Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

### Related Information

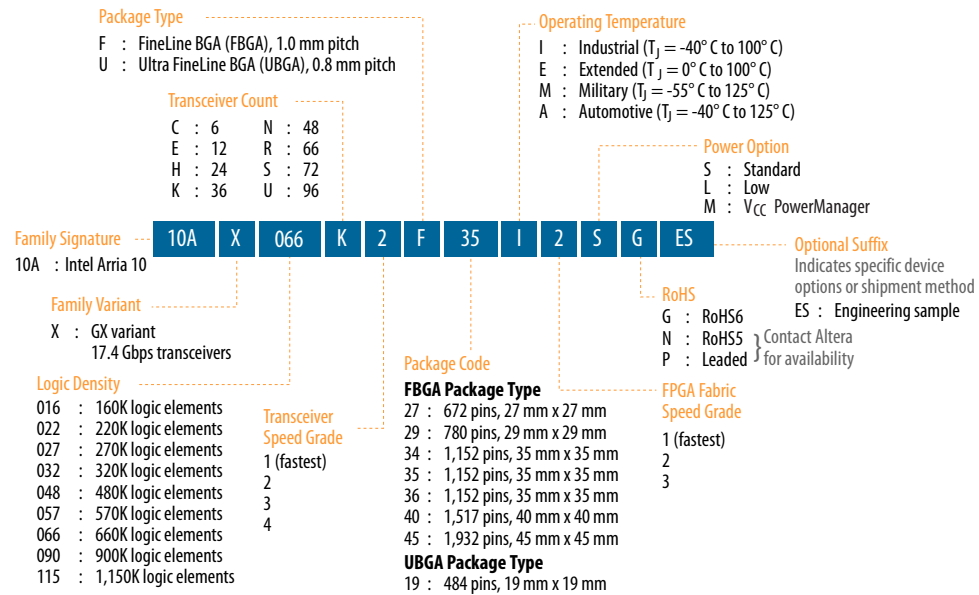
#### [Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



## Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



## Related Information

### Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



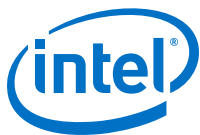
## Maximum Resources

**Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)**

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	80,330	101,620	119,900	183,590
Register		246,040	321,320	406,480	479,600	734,360
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620
	MLAB	1,050	1,690	2,452	2,727	4,164
Variable-precision DSP Block		156	192	830	985	1,368
18 x 19 Multiplier		312	384	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO <sup>(3)</sup>		288	288	384	384	492
LVDS Pair <sup>(4)</sup>		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

<sup>(3)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(4)</sup> Each LVDS I/O pair can be used as differential input or output.



**Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)**

Resource		Product Line			
		GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		570	660	900	1,150
ALM		217,080	251,680	339,620	427,200
Register		868,320	1,006,720	1,358,480	1,708,800
Memory (Kb)	M20K	36,000	42,620	48,460	54,260
	MLAB	5,096	5,788	9,386	12,984
Variable-precision DSP Block		1,523	1,687	1,518	1,518
18 x 19 Multiplier		3,046	3,374	3,036	3,036
PLL	Fractional Synthesis	16	16	32	32
	I/O	16	16	16	16
17.4 Gbps Transceiver		48	48	96	96
GPIO <sup>(3)</sup>		696	696	768	768
LVDS Pair <sup>(4)</sup>		324	324	384	384
PCIe Hard IP Block		2	2	4	4
Hard Memory Controller		16	16	16	16

## Package Plan

**Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
GX 160	48	192	6	48	192	12	48	240	12
GX 220	48	192	6	48	192	12	48	240	12
GX 270	—	—	—	48	192	12	48	312	12
GX 320	—	—	—	48	192	12	48	312	12
GX 480	—	—	—	—	—	—	48	312	12



### Related Information

I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

## Intel Arria 10 SX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 SX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

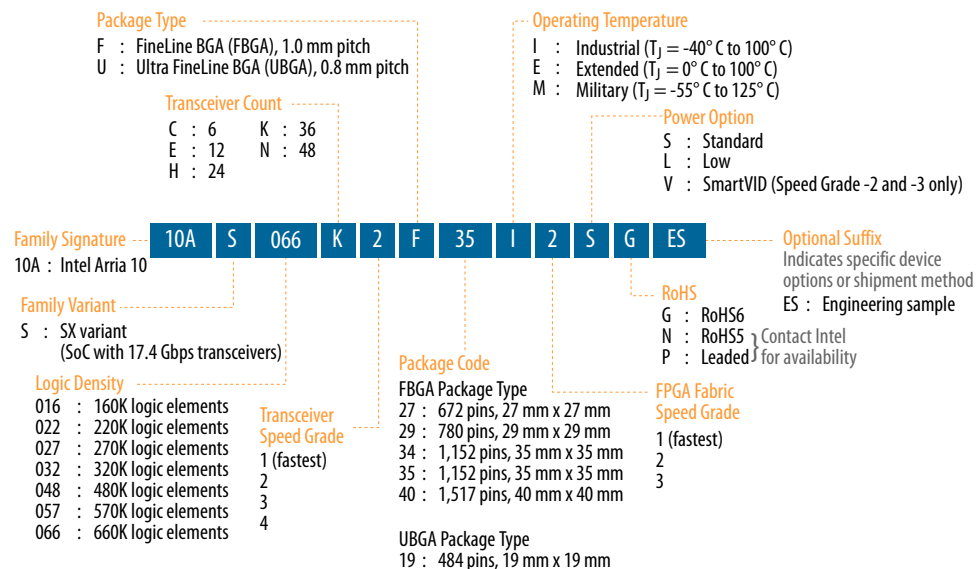
### Related Information

Intel FPGA Product Selector

Provides the latest information on Intel products.

## Available Options

**Figure 3. Sample Ordering Code and Available Options for Intel Arria 10 SX Devices**



### Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



## Maximum Resources

**Table 12. Maximum Resource Counts for Intel Arria 10 SX Devices**

Resource		Product Line						
		SX 160	SX 220	SX 270	SX 320	SX 480	SX 570	SX 660
Logic Elements (LE) (K)		160	220	270	320	480	570	660
ALM		61,510	80,330	101,620	119,900	183,590	217,080	251,680
Register		246,040	321,320	406,480	479,600	734,360	868,320	1,006,720
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620	36,000	42,620
	MLAB	1,050	1,690	2,452	2,727	4,164	5,096	5,788
Variable-precision DSP Block		156	192	830	985	1,368	1,523	1,687
18 x 19 Multiplier		312	384	1,660	1,970	2,736	3,046	3,374
PLL	Fractional Synthesis	6	6	8	8	12	16	16
	I/O	6	6	8	8	12	16	16
17.4 Gbps Transceiver		12	12	24	24	36	48	48
GPIO <sup>(8)</sup>		288	288	384	384	492	696	696
LVDS Pair <sup>(9)</sup>		120	120	168	168	174	324	324
PCIe Hard IP Block		1	1	2	2	2	2	2
Hard Memory Controller		6	6	8	8	12	16	16
ARM Cortex-A9 MPCore Processor		Yes	Yes	Yes	Yes	Yes	Yes	Yes

## Package Plan

**Table 13. Package Plan for Intel Arria 10 SX Devices (U19, F27, F29, and F34)**

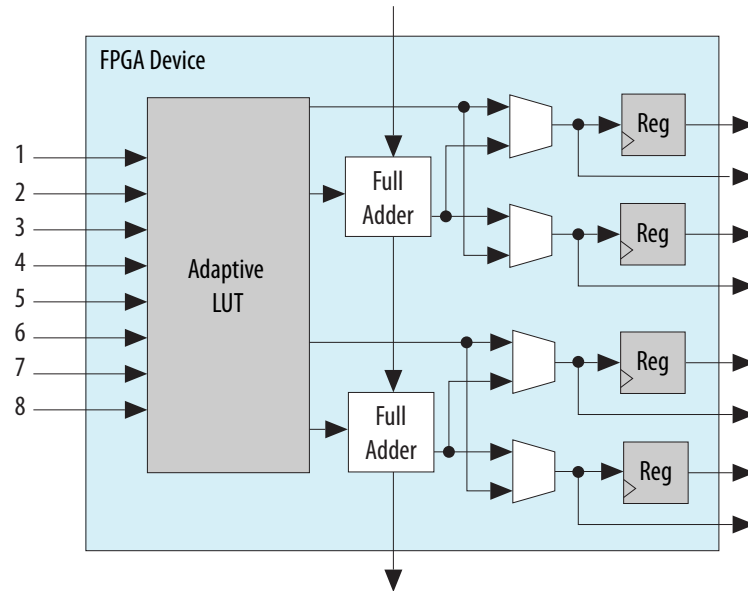
Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	U19 (19 mm × 19 mm, 484-pin UBGGA)			F27 (27 mm × 27 mm, 672-pin FBGA)			F29 (29 mm × 29 mm, 780-pin FBGA)			F34 (35 mm × 35 mm, 1152-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR	3 V I/O	LVDS I/O	XCVR
SX 160	48	144	6	48	192	12	48	240	12	—	—	—
SX 220	48	144	6	48	192	12	48	240	12	—	—	—
SX 270	—	—	—	48	192	12	48	312	12	48	336	24
SX 320	—	—	—	48	192	12	48	312	12	48	336	24
continued...												

<sup>(8)</sup> The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

<sup>(9)</sup> Each LVDS I/O pair can be used as differential input or output.

**Figure 5. ALM for Intel Arria 10 Devices**



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

## Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support





## Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

## Embedded Memory Capacity in Intel Arria 10 Devices

**Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices**

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Intel Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	587	11,740	2,703	1,690	13,430
	GX 270	750	15,000	3,922	2,452	17,452
	GX 320	891	17,820	4,363	2,727	20,547
	GX 480	1,431	28,620	6,662	4,164	32,784
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,131	42,620	9,260	5,788	48,408
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	587	11,740	2,703	1,690	13,430
	SX 270	750	15,000	3,922	2,452	17,452
	SX 320	891	17,820	4,363	2,727	20,547
	SX 480	1,431	28,620	6,662	4,164	32,784
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,131	42,620	9,260	5,788	48,408

## Embedded Memory Configurations for Single-port Mode

**Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices**

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 <sup>(10)</sup>	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

## Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

### Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

### Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

### Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

<sup>(10)</sup> Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
  - Conventional integer mode equivalent to the general purpose PLL
  - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

## I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

## FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
  - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
  - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage ( $V_{OD}$ ) and programmable pre-emphasis

**Table 20. Memory Standards Supported by the Hard Memory Controller**

This table lists the overall capability of the hard memory controller. For specific details, refer to the External Memory Interface Spec Estimator and Intel Arria 10 Device Datasheet.

Memory Standard	Rate Support	Ping Pong PHY Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	Yes	1,067
		—	1,200
DDR3 SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	1,067
		—	1,067
DDR3L SDRAM	Half rate	Yes	533
		—	667
	Quarter rate	Yes	933
		—	933
LPDDR3 SDRAM	Half rate	—	533
	Quarter rate	—	800

**Table 21. Memory Standards Supported by the Soft Memory Controller**

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 <sup>(11)</sup>	Quarter rate	1,200
QDR IV SRAM <sup>(11)</sup>	Quarter rate	1,067
QDR II SRAM	Full rate	333
	Half rate	633
QDR II+ SRAM	Full rate	333
	Half rate	633
QDR II+ Xtreme SRAM	Full rate	333
	Half rate	633

**Table 22. Memory Standards Supported by the HPS Hard Memory Controller**

The hard processor system (HPS) is available in Intel Arria 10 SoC devices only.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Half rate	1,200
DDR3 SDRAM	Half rate	1,067
DDR3L SDRAM	Half rate	933

<sup>(11)</sup> Intel Arria 10 devices support this external memory interface using hard PHY with soft memory controller.



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

#### **Related Information**

[PCS Features](#) on page 30

## **Low Power Serial Transceivers**

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed

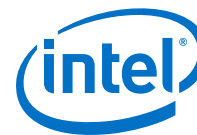


Figure 7. Device Chip Overview for Intel Arria 10 GX and GT Devices

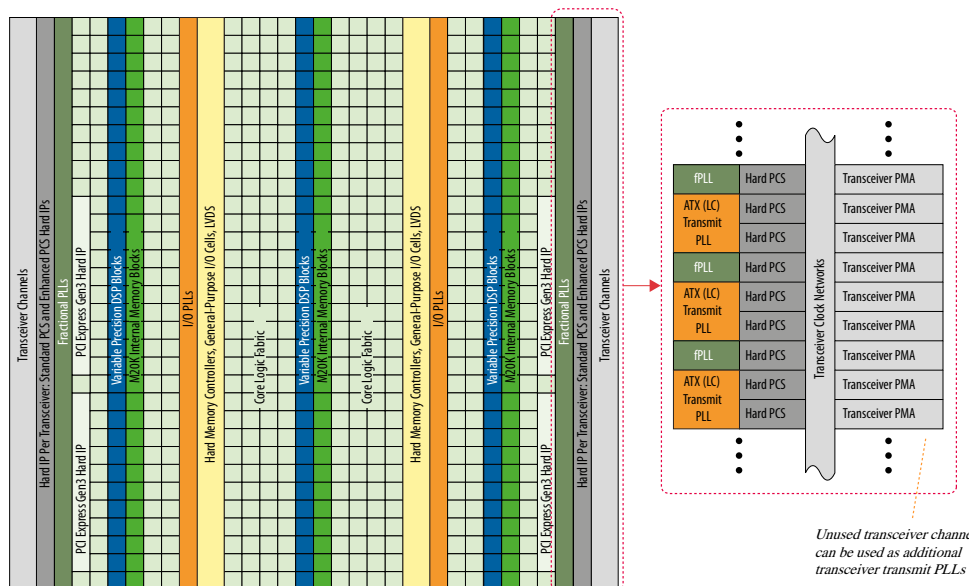
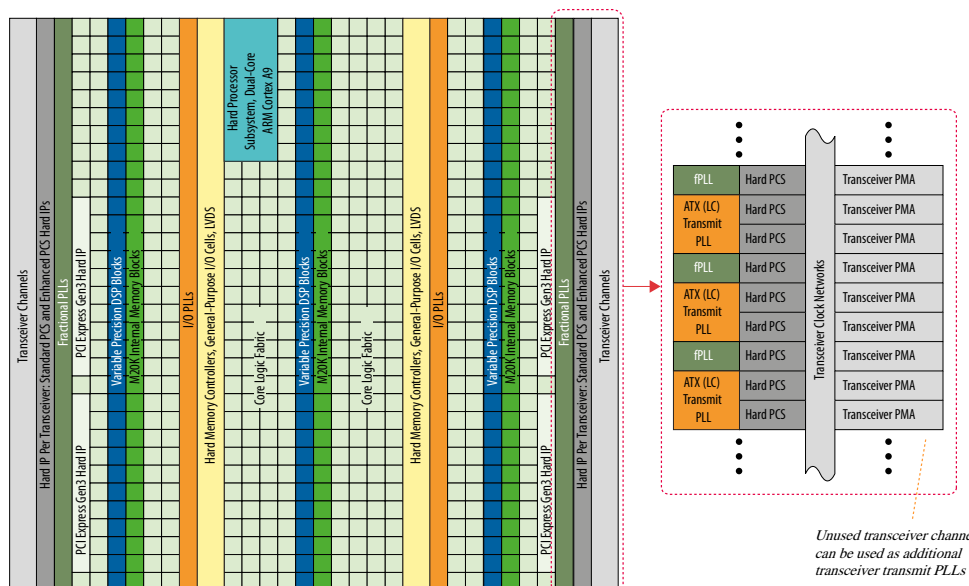


Figure 8. Device Chip Overview for Intel Arria 10 SX Devices



## PMA Features

Intel Arria 10 transceivers provide exceptional signal integrity at data rates up to 25.8 Gbps. Clocking options include ultra-low jitter ATX PLLs (LC tank based), clock multiplier unit (CMU) PLLs, and fractional PLLs.



PCS	Description
Standard PCS	<ul style="list-style-type: none"> <li>Operates at a data rate up to 12 Gbps</li> <li>Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS</li> <li>Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.</li> </ul>
Enhanced PCS	<ul style="list-style-type: none"> <li>Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA</li> <li>Handles data transfer to and from the FPGA fabric</li> <li>Handles data transfer internally to and from the PMA</li> <li>Provides frequency compensation</li> <li>Performs channel bonding for multi-channel low skew applications</li> </ul>
PCIe Gen3 PCS	<ul style="list-style-type: none"> <li>Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates</li> <li>Provides support for PIPE 3.0 features</li> <li>Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed</li> </ul>

### Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

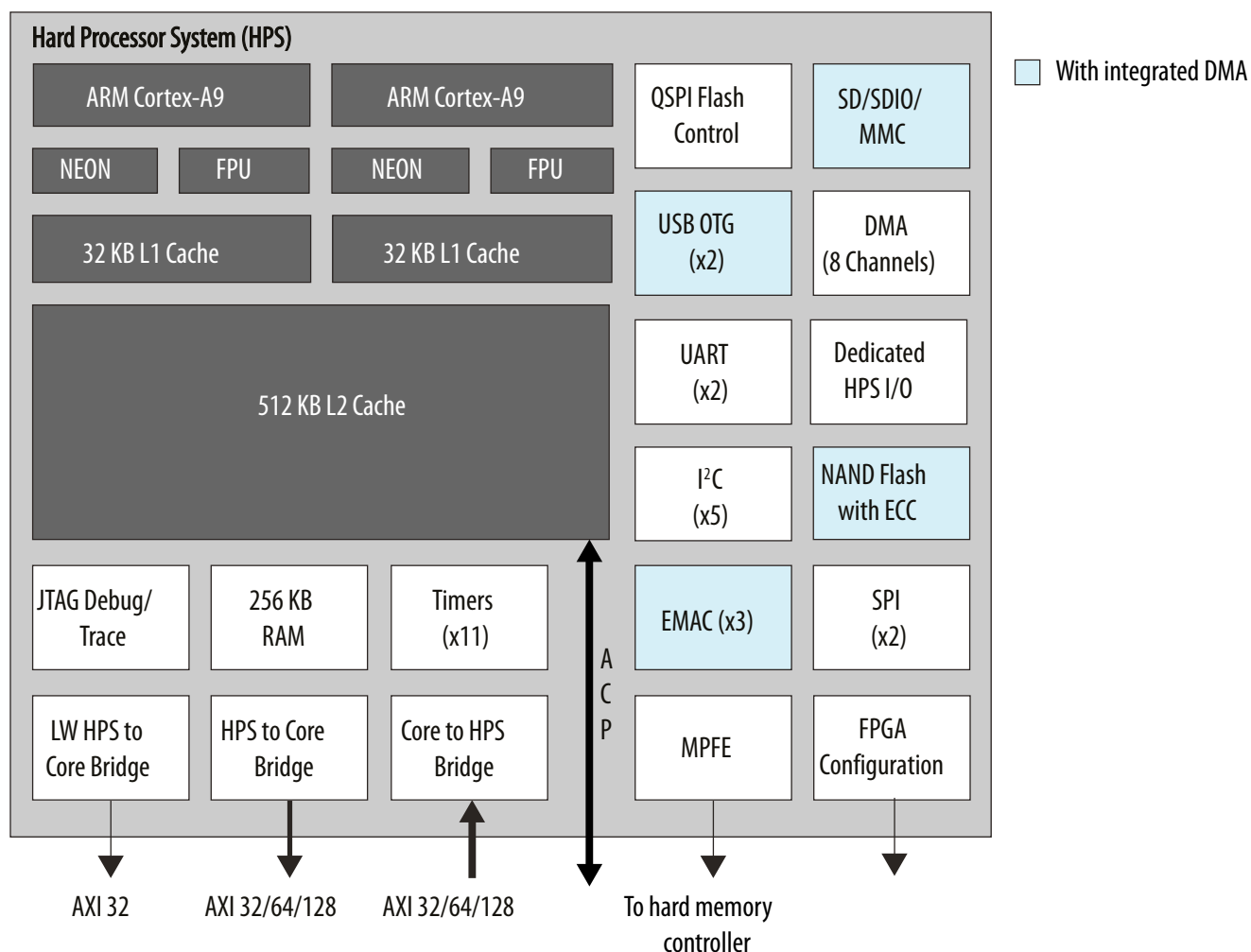
## PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen3 x1, x2, x4, x8	8.0	Native PHY (PIPE)	Standard PCS and PCIe Gen3 PCS
PCIe Gen2 x1, x2, x4, x8	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4, x8	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS
1000BASE-X Gigabit Ethernet with IEEE 1588v2	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R with IEEE 1588v2	10.3125	Native PHY	Enhanced PCS
10GBASE-R with KR FEC	10.3125	Native PHY	Enhanced PCS
10GBASE-KR and 1000BASE-X	10.3125	1G/10GbE and 10GBASE-KR PHY	Standard PCS and Enhanced PCS
Interlaken (CEI-6G/11G)	3.125 to 17.4	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	11.2	Native PHY	Enhanced PCS
10G SDI	10.692	Native PHY	Enhanced PCS
continued...			

**Figure 9. HPS Block Diagram**

This figure shows a block diagram of the HPS with the dual ARM Cortex-A9 MPCore processor.



## Key Advantages of 20-nm HPS

The 20-nm HPS strikes a balance between enabling maximum software compatibility with 28-nm SoCs while still improving upon the 28-nm HPS architecture. These improvements address the requirements of the next generation target markets such as wireless and wireline communications, compute and storage equipment, broadcast and military in terms of performance, memory bandwidth, connectivity via backplane and security.

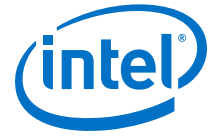




**Table 24. Improvements in 20 nm HPS**

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none"><li>• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.</li><li>• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.</li><li>• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.</li></ul>
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I <sup>2</sup> C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).



## Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
  - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
  - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
  - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
  - 32 KB of L1 instruction cache, 32 KB of L1 data cache
  - Single- and double-precision floating-point unit and NEON media engine
  - CoreSight debug and trace technology
  - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I<sup>2</sup>C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core  $V_{CC}$  while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

## Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

## Document Revision History for Intel Arria 10 Device Overview

Document Version	Changes
2018.04.09	Updated the lowest $V_{CC}$ from 0.83 V to 0.82 V in the topic listing a summary of the device features.

Date	Version	Changes
January 2018	2018.01.17	<ul style="list-style-type: none"><li>• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.</li><li>• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.</li><li>• Updated transceiver backplane capability to 12.5 Gbps.</li><li>• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure.</li></ul>
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Date	Version	Changes
		<ul style="list-style-type: none"> <li>Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure.</li> <li>Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps.</li> <li>Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.</li> </ul>
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> <li>Corrected protocol names with "1588" to "IEEE 1588v2".</li> <li>Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants.</li> <li>Removed all "Preliminary" marks.</li> </ul>
March 2017	2017.03.15	<ul style="list-style-type: none"> <li>Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices.</li> <li>Rebranded as Intel.</li> </ul>
October 2016	2016.10.31	<ul style="list-style-type: none"> <li>Removed package F36 from Intel Arria 10 GX devices.</li> <li>Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.</li> </ul>
May 2016	2016.05.02	<ul style="list-style-type: none"> <li>Updated the FPGA Configuration and HPS Booting topic.</li> <li>Remove V<sub>CC</sub> PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices.</li> <li>Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA.</li> <li>Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.</li> </ul>
February 2016	2016.02.11	<ul style="list-style-type: none"> <li>Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally.</li> <li>Revised the state for Core clock networks in the Summary of Features topic.</li> <li>Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table.</li> <li>Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table.</li> <li>Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table.</li> <li>Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure.</li> <li>Changed transceiver parameters in the "Low Power Serial Transceivers" section.</li> <li>Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table.</li> <li>Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure.</li> <li>Changed the datarates for GT devices in the "PMA Features" section.</li> <li>Changed the datarates for GT devices in the "PCS Features" section.</li> </ul>
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Date	Version	Changes
August 2014	2014.08.18	<ul style="list-style-type: none"> <li>Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620.</li> <li>Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table.</li> <li>Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration.</li> <li>Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller.</li> <li>Added variable precision DSP blocks support for floating-point arithmetic.</li> </ul>
June 2014	2014.06.19	Updated number of dedicated I/Os in the HPS block to 17.
February 2014	2014.02.21	Updated transceiver speed grade options for GT devices in Figure 2.
February 2014	2014.02.06	Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps.
December 2013	2013.12.10	<ul style="list-style-type: none"> <li>Updated the HPS memory standards support from LPDDR2 to LPDDR3.</li> <li>Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks .</li> </ul>
December 2013	2013.12.02	Initial release.