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Understanding Embedded - FPGAs (Field Programmable Gate Array)

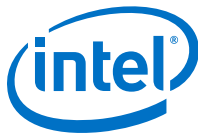
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

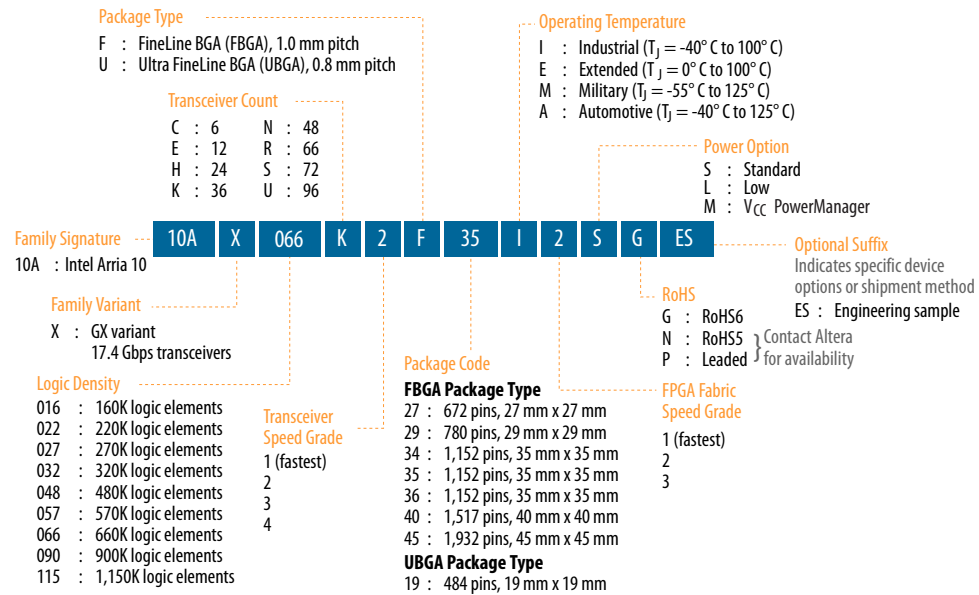
Details

| | |
|--------------------------------|---|
| Product Status | Discontinued at Digi-Key |
| Number of LABs/CLBs | 427200 |
| Number of Logic Elements/Cells | 1150000 |
| Total RAM Bits | 68857856 |
| Number of I/O | 504 |
| Number of Gates | - |
| Voltage - Supply | 0.87V ~ 0.93V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1152-BBGA, FCBGA |
| Supplier Device Package | 1152-FCBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/10ax115h4f34i3sge2 |



Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Maximum Resources

Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

| Resource | | Product Line | | | | |
|------------------------------|----------------------|--------------|---------|---------|---------|---------|
| | | GX 160 | GX 220 | GX 270 | GX 320 | GX 480 |
| Logic Elements (LE) (K) | | 160 | 220 | 270 | 320 | 480 |
| ALM | | 61,510 | 80,330 | 101,620 | 119,900 | 183,590 |
| Register | | 246,040 | 321,320 | 406,480 | 479,600 | 734,360 |
| Memory (Kb) | M20K | 8,800 | 11,740 | 15,000 | 17,820 | 28,620 |
| | MLAB | 1,050 | 1,690 | 2,452 | 2,727 | 4,164 |
| Variable-precision DSP Block | | 156 | 192 | 830 | 985 | 1,368 |
| 18 x 19 Multiplier | | 312 | 384 | 1,660 | 1,970 | 2,736 |
| PLL | Fractional Synthesis | 6 | 6 | 8 | 8 | 12 |
| | I/O | 6 | 6 | 8 | 8 | 12 |
| 17.4 Gbps Transceiver | | 12 | 12 | 24 | 24 | 36 |
| GPIO ⁽³⁾ | | 288 | 288 | 384 | 384 | 492 |
| LVDS Pair ⁽⁴⁾ | | 120 | 120 | 168 | 168 | 222 |
| PCIe Hard IP Block | | 1 | 1 | 2 | 2 | 2 |
| Hard Memory Controller | | 6 | 6 | 8 | 8 | 12 |

⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁴⁾ Each LVDS I/O pair can be used as differential input or output.



Table 6. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 570, GX 660, GX 900, and GX 1150)

| Resource | | Product Line | | | |
|------------------------------|----------------------|--------------|-----------|-----------|-----------|
| | | GX 570 | GX 660 | GX 900 | GX 1150 |
| Logic Elements (LE) (K) | | 570 | 660 | 900 | 1,150 |
| ALM | | 217,080 | 251,680 | 339,620 | 427,200 |
| Register | | 868,320 | 1,006,720 | 1,358,480 | 1,708,800 |
| Memory (Kb) | M20K | 36,000 | 42,620 | 48,460 | 54,260 |
| | MLAB | 5,096 | 5,788 | 9,386 | 12,984 |
| Variable-precision DSP Block | | 1,523 | 1,687 | 1,518 | 1,518 |
| 18 x 19 Multiplier | | 3,046 | 3,374 | 3,036 | 3,036 |
| PLL | Fractional Synthesis | 16 | 16 | 32 | 32 |
| | I/O | 16 | 16 | 16 | 16 |
| 17.4 Gbps Transceiver | | 48 | 48 | 96 | 96 |
| GPIO ⁽³⁾ | | 696 | 696 | 768 | 768 |
| LVDS Pair ⁽⁴⁾ | | 324 | 324 | 384 | 384 |
| PCIe Hard IP Block | | 2 | 2 | 4 | 4 |
| Hard Memory Controller | | 16 | 16 | 16 | 16 |

Package Plan

Table 7. Package Plan for Intel Arria 10 GX Devices (U19, F27, and F29)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | |
|--------------|---|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 160 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 220 | 48 | 192 | 6 | 48 | 192 | 12 | 48 | 240 | 12 |
| GX 270 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 320 | — | — | — | 48 | 192 | 12 | 48 | 312 | 12 |
| GX 480 | — | — | — | — | — | — | 48 | 312 | 12 |

**Table 8. Package Plan for Intel Arria 10 GX Devices (F34, F35, NF40, and KF40)**

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F34 (35 mm × 35 mm, 1152-pin FBGA) | | | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|-------------|------|--|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 270 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 320 | 48 | 336 | 24 | 48 | 336 | 24 | — | — | — | — | — | — |
| GX 480 | 48 | 444 | 24 | 48 | 348 | 36 | — | — | — | — | — | — |
| GX 570 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 660 | 48 | 444 | 24 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| GX 900 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |
| GX 1150 | — | 504 | 24 | — | — | — | — | — | — | — | 600 | 48 |

Table 9. Package Plan for Intel Arria 10 GX Devices (RF40, NF45, SF45, and UF45)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | RF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF45 (45 mm × 45 mm) 1932-pin FBGA) | | | SF45 (45 mm × 45 mm) 1932-pin FBGA) | | | UF45 (45 mm × 45 mm) 1932-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|---|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| GX 900 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |
| GX 1150 | — | 342 | 66 | — | 768 | 48 | — | 624 | 72 | — | 480 | 96 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.

Intel Arria 10 GT

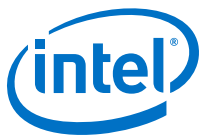
This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GT devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



| Product Line | U19 (19 mm × 19 mm, 484-pin UBGA) | | | F27 (27 mm × 27 mm, 672-pin FBGA) | | | F29 (29 mm × 29 mm, 780-pin FBGA) | | | F34 (35 mm × 35 mm, 1152-pin FBGA) | | |
|--------------|---|-------------|------|---|-------------|------|---|-------------|------|--|-------------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 480 | — | — | — | — | — | — | 48 | 312 | 12 | 48 | 444 | 24 |
| SX 570 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |
| SX 660 | — | — | — | — | — | — | — | — | — | 48 | 444 | 24 |

Table 14. Package Plan for Intel Arria 10 SX Devices (F35, KF40, and NF40)

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

| Product Line | F35 (35 mm × 35 mm, 1152-pin FBGA) | | | KF40 (40 mm × 40 mm, 1517-pin FBGA) | | | NF40 (40 mm × 40 mm, 1517-pin FBGA) | | |
|--------------|--|----------|------|---|----------|------|---|----------|------|
| | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR | 3 V I/O | LVDS I/O | XCVR |
| SX 270 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 320 | 48 | 336 | 24 | — | — | — | — | — | — |
| SX 480 | 48 | 348 | 36 | — | — | — | — | — | — |
| SX 570 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |
| SX 660 | 48 | 348 | 36 | 96 | 600 | 36 | 48 | 540 | 48 |

Related Information

[I/O and High-Speed Differential I/O Interfaces in Intel Arria 10 Devices chapter, Intel Arria 10 Device Handbook](#)

Provides the number of 3 V and LVDS I/Os, and LVDS channels for each Intel Arria 10 device package.



I/O Vertical Migration for Intel Arria 10 Devices

Figure 4. Migration Capability Across Intel Arria 10 Product Lines

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- An LVDS I/O bank in the source device may be mapped to a 3 V I/O bank in the target device. To use memory interface clock frequency higher than 533 MHz, assign external memory interface pins only to banks that are LVDS I/O in both devices.
- There may be nominal 0.15 mm package height difference between some product lines in the same package type.
- Some migration paths are not shown in the Intel Quartus Prime software **Pin Migration View**.

| Variant | Product Line | Package | | | | | | | | | | |
|---------------------|--------------|---------|-----|-----|-----|-----|------|------|------|------|------|------|
| | | U19 | F27 | F29 | F34 | F35 | KF40 | NF40 | RF40 | NF45 | SF45 | UF45 |
| Intel® Arria® 10 GX | GX 160 | ↕ | ↕ | ↕ | | | | | | | | |
| | GX 220 | ↕ | ↕ | | | | | | | | | |
| | GX 270 | | ↕ | | ↕ | ↕ | | | | | | |
| | GX 320 | | ↕ | ↕ | | ↕ | | | | | | |
| | GX 480 | | | ↕ | | | | | | | | |
| | GX 570 | | | | ↕ | ↕ | ↕ | ↕ | | | | |
| | GX 660 | | | | ↕ | ↕ | ↕ | ↕ | ↕ | ↕ | ↕ | ↕ |
| | GX 900 | | | | | | | | | | | |
| | GX 1150 | | | | ↕ | | | ↕ | ↕ | ↕ | ↕ | ↕ |
| Intel Arria 10 GT | GT 900 | | | | | | | ↕ | ↕ | ↕ | ↕ | ↕ |
| | GT 1150 | | | | | | | | | | ↕ | |
| Intel Arria 10 SX | SX 160 | ↕ | ↕ | ↕ | | | | | | | | |
| | SX 220 | ↕ | | | | | | | | | | |
| | SX 270 | | ↕ | | ↕ | ↕ | | | | | | |
| | SX 320 | | ↕ | ↕ | | | | | | | | |
| | SX 480 | | | ↕ | | | | | | | | |
| | SX 570 | | | | ↕ | ↕ | ↕ | ↕ | | | | |
| | SX 660 | | | | ↕ | ↕ | ↕ | ↕ | | | | |

Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner.

Adaptive Logic Module

Intel Arria 10 devices use a 20 nm ALM as the basic building block of the logic fabric.

The ALM architecture is the same as the previous generation FPGAs, allowing for efficient implementation of logic functions and easy conversion of IP between the device generations.

The ALM, as shown in following figure, uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than the traditional two-register per LUT architecture.



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices

| Usage Example | Multiplier Size (Bit) | DSP Block Resources |
|---|---------------------------------|---------------------|
| Medium precision fixed point | Two 18 x 19 | 1 |
| High precision fixed or Single precision floating point | One 27 x 27 | 1 |
| Fixed point FFTs | One 19 x 36 with external adder | 1 |
| Very high precision fixed point | One 36 x 36 with external adder | 2 |
| Double precision floating point | One 54 x 54 with external adder | 4 |

Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

| Variant | Product Line | Variable-precision DSP Block | Independent Input and Output Multiplications Operator | | 18 x 19 Multiplier Adder Sum Mode | 18 x 18 Multiplier Adder Summed with 36 bit Input |
|-------------------|--------------|------------------------------|---|--------------------|-----------------------------------|---|
| | | | 18 x 19 Multiplier | 27 x 27 Multiplier | | |
| Intel Arria 10 GX | GX 160 | 156 | 312 | 156 | 156 | 156 |
| | GX 220 | 192 | 384 | 192 | 192 | 192 |
| | GX 270 | 830 | 1,660 | 830 | 830 | 830 |
| | GX 320 | 984 | 1,968 | 984 | 984 | 984 |
| | GX 480 | 1,368 | 2,736 | 1,368 | 1,368 | 1,368 |
| | GX 570 | 1,523 | 3,046 | 1,523 | 1,523 | 1,523 |
| | GX 660 | 1,687 | 3,374 | 1,687 | 1,687 | 1,687 |
| | GX 900 | 1,518 | 3,036 | 1,518 | 1,518 | 1,518 |
| | GX 1150 | 1,518 | 3,036 | 1,518 | 1,518 | 1,518 |
| Intel Arria 10 GT | GT 900 | 1,518 | 3,036 | 1,518 | 1,518 | 1,518 |
| | GT 1150 | 1,518 | 3,036 | 1,518 | 1,518 | 1,518 |
| Intel Arria 10 SX | SX 160 | 156 | 312 | 156 | 156 | 156 |
| | SX 220 | 192 | 384 | 192 | 192 | 192 |
| | SX 270 | 830 | 1,660 | 830 | 830 | 830 |

continued...

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

| Memory Block | Depth (bits) | Programmable Width |
|--------------|--------------------|--------------------|
| MLAB | 32 | x16, x18, or x20 |
| | 64 ⁽¹⁰⁾ | x8, x9, x10 |
| M20K | 512 | x40, x32 |
| | 1K | x20, x16 |
| | 2K | x10, x8 |
| | 4K | x5, x4 |
| | 8K | x2 |
| | 16K | x1 |

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.



The fractional synthesis PLLs support the following features:

- Reference clock frequency synthesis for transceiver CMU and Advanced Transmit (ATX) PLLs
- Clock network delay compensation
- Zero-delay buffering
- Direct transmit clocking for transceivers
- Independently configurable into two modes:
 - Conventional integer mode equivalent to the general purpose PLL
 - Enhanced fractional mode with third order delta-sigma modulation
- PLL cascading

I/O PLLs

The integer mode I/O PLLs are located in each bank of 48 I/Os. You can use the I/O PLLs to simplify the design of external memory and high-speed LVDS interfaces.

In each I/O bank, the I/O PLLs are adjacent to the hard memory controllers and LVDS SERDES. Because these PLLs are tightly coupled with the I/Os that need to use them, it makes it easier to close timing.

You can use the I/O PLLs for general purpose applications in the core such as clock network delay compensation and zero-delay buffering.

Intel Arria 10 devices support PLL-to-PLL cascading.

FPGA General Purpose I/O

Intel Arria 10 devices offer highly configurable GPIOs. Each I/O bank contains 48 general purpose I/Os and a high-efficiency hard memory controller.

The following list describes the features of the GPIOs:

- Consist of 3 V I/Os for high-voltage application and LVDS I/Os for differential signaling
 - Up to two 3 V I/O banks, available in some devices, that support up to 3 V I/O standards
 - LVDS I/O banks that support up to 1.8 V I/O standards
- Support a wide range of single-ended and differential I/O interfaces
- LVDS speeds up to 1.6 Gbps
- Each LVDS pair of pins has differential input and output buffers, allowing you to configure the LVDS direction for each pair.
- Programmable bus hold and weak pull-up
- Programmable differential output voltage (V_{OD}) and programmable pre-emphasis



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

[PCS Features](#) on page 30

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

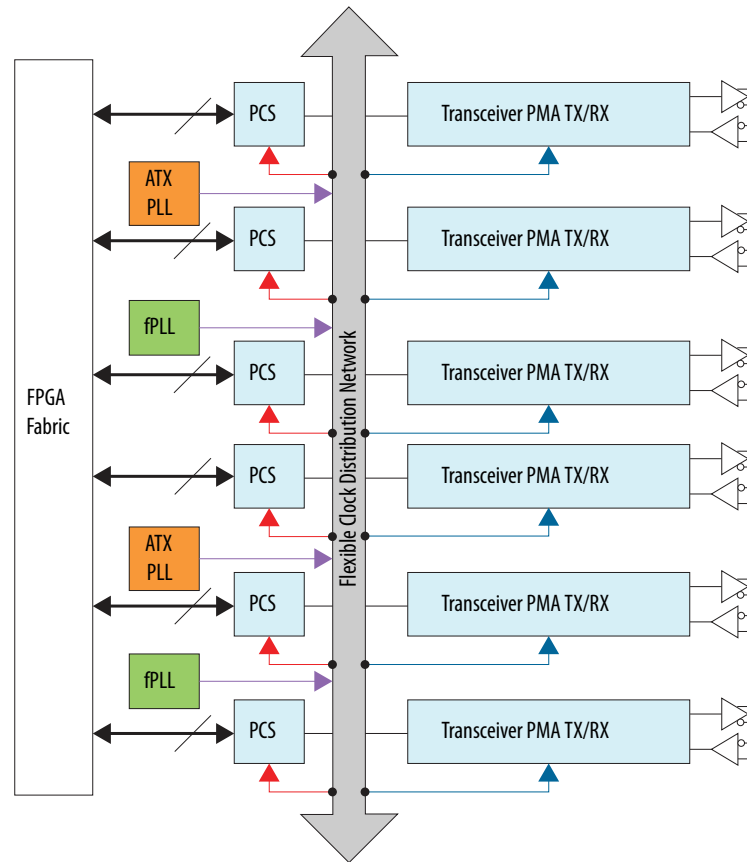
Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed

Figure 6. Intel Arria 10 Transceiver Block Architecture



Transceiver Channels

All transceiver channels feature a dedicated Physical Medium Attachment (PMA) and a hardened Physical Coding Sublayer (PCS).

- The PMA provides primary interfacing capabilities to physical channels.
- The PCS typically handles encoding/decoding, word alignment, and other pre-processing functions before transferring data to the FPGA core fabric.

A transceiver channel consists of a PMA and a PCS block. Most transceiver banks have 6 channels. There are some transceiver banks that contain only 3 channels.

A wide variety of bonded and non-bonded data rate configurations is possible using a highly configurable clock distribution network. Up to 80 independent transceiver data rates can be configured.

The following figures are graphical representations of top views of the silicon die, which correspond to reverse views for flip chip packages. Different Intel Arria 10 devices may have different floorplans than the ones shown in the figures.



| PCS | Description |
|---------------|--|
| Standard PCS | <ul style="list-style-type: none"> Operates at a data rate up to 12 Gbps Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules. |
| Enhanced PCS | <ul style="list-style-type: none"> Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA Handles data transfer to and from the FPGA fabric Handles data transfer internally to and from the PMA Provides frequency compensation Performs channel bonding for multi-channel low skew applications |
| PCIe Gen3 PCS | <ul style="list-style-type: none"> Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates Provides support for PIPE 3.0 features Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed |

Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

| Protocol | Data Rate (Gbps) | Transceiver IP | PCS Support |
|--|------------------|-----------------------------|--------------------------------|
| PCIe Gen3 x1, x2, x4, x8 | 8.0 | Native PHY (PIPE) | Standard PCS and PCIe Gen3 PCS |
| PCIe Gen2 x1, x2, x4, x8 | 5.0 | Native PHY (PIPE) | Standard PCS |
| PCIe Gen1 x1, x2, x4, x8 | 2.5 | Native PHY (PIPE) | Standard PCS |
| 1000BASE-X Gigabit Ethernet | 1.25 | Native PHY | Standard PCS |
| 1000BASE-X Gigabit Ethernet with IEEE 1588v2 | 1.25 | Native PHY | Standard PCS |
| 10GBASE-R | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with IEEE 1588v2 | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-R with KR FEC | 10.3125 | Native PHY | Enhanced PCS |
| 10GBASE-KR and 1000BASE-X | 10.3125 | 1G/10GbE and 10GBASE-KR PHY | Standard PCS and Enhanced PCS |
| Interlaken (CEI-6G/11G) | 3.125 to 17.4 | Native PHY | Enhanced PCS |
| SFI-S/SFI-5.2 | 11.2 | Native PHY | Enhanced PCS |
| 10G SDI | 10.692 | Native PHY | Enhanced PCS |
| continued... | | | |



Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

| Advantages/ Improvements | Description |
|---|---|
| Increased performance and overdrive capability | While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator. |
| Increased processor memory bandwidth and DDR4 support | Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller. |
| Flexible I/O sharing | An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none">• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic. |
| EMAC core | Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I ² C interface. |
| On-chip memory | The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms. |
| ECC enhancements | Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals. |
| HPS to FPGA Interconnect Backbone | Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port. |
| FPGA configuration and HPS booting | The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility. |
| Security | New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA). |



Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
 - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
 - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
 - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
 - 32 KB of L1 instruction cache, 32 KB of L1 data cache
 - Single- and double-precision floating-point unit and NEON media engine
 - CoreSight debug and trace technology
 - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I²C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)



Instead of placing all device functions in the FPGA fabric, you can store some functions that do not run simultaneously in external memory and load them only when required. This capability increases the effective logic density of the device, and lowers cost and power consumption.

In the Intel solution, you do not have to worry about intricate device architecture to perform a partial reconfiguration. The partial reconfiguration capability is built into the Intel Quartus Prime design software, making such time-intensive task simple.

Intel Arria 10 devices support partial reconfiguration in the following configuration options:

- Using an internal host:
 - All supported configuration modes where the FPGA has access to external memory devices such as serial and parallel flash memory.
 - Configuration via Protocol [CvP (PCIe)]
- Using an external host—passive serial (PS), fast passive parallel (FPP) x8, FPP x16, and FPP x32 I/O interface.

Enhanced Configuration and Configuration via Protocol

Table 25. Configuration Schemes and Features of Intel Arria 10 Devices

Intel Arria 10 devices support 1.8 V programming voltage and several configuration schemes.

| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) ⁽¹³⁾ | Decompression | Design Security ⁽¹⁴⁾ | Partial Reconfiguration ⁽¹⁵⁾ | Remote System Update |
|--|---------------|----------------------|--------------------------------------|---------------|---------------------------------|---|-------------------------------------|
| JTAG | 1 bit | 33 | 33 | — | — | Yes ⁽¹⁶⁾ | — |
| Active Serial (AS) through the EPCQ-L configuration device | 1 bit, 4 bits | 100 | 400 | Yes | Yes | Yes ⁽¹⁶⁾ | Yes |
| Passive serial (PS) through CPLD or external microcontroller | 1 bit | 100 | 100 | Yes | Yes | Yes ⁽¹⁶⁾ | Parallel Flash Loader (PFL) IP core |

continued...

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁶⁾ Partial configuration can be performed only when it is configured as internal host.



| Scheme | Data Width | Max Clock Rate (MHz) | Max Data Rate (Mbps) ⁽¹³⁾ | Decompression | Design Security ⁽¹⁴⁾ | Partial Reconfiguration ⁽¹⁵⁾ | Remote System Update |
|--|----------------------|----------------------|--------------------------------------|---------------|---------------------------------|---|----------------------|
| Fast passive parallel (FPP) through CPLD or external microcontroller | 8 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | PFL IP core |
| | 16 bits | | | Yes | Yes | | |
| | 32 bits | | | Yes | Yes | | |
| Configuration via HPS | 16 bits | 100 | 3200 | Yes | Yes | Yes ⁽¹⁷⁾ | — |
| | 32 bits | | | Yes | Yes | | |
| Configuration via Protocol [CvP (PCIe*)] | x1, x2, x4, x8 lanes | — | 8000 | Yes | Yes | Yes ⁽¹⁶⁾ | — |

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁷⁾ Supported at a maximum clock rate of 100 MHz.



The optional power reduction techniques in Intel Arria 10 devices include:

- **SmartVID**—a code is programmed into each device during manufacturing that allows a smart regulator to operate the device at lower core V_{CC} while maintaining performance
- **Programmable Power Technology**—non-critical timing paths are identified by the Intel Quartus Prime software and the logic in these paths is biased for low power instead of high performance
- **Low Static Power Options**—devices are available with either standard static power or low static power while maintaining performance

Furthermore, Intel Arria 10 devices feature Intel's industry-leading low power transceivers and include a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings compared to soft implementations. In general, hard IP blocks consume up to 90% less power than the equivalent soft logic implementations.

Incremental Compilation

The Intel Quartus Prime software incremental compilation feature reduces compilation time and helps preserve performance to ease timing closure. The incremental compilation feature enables the partial reconfiguration flow for Intel Arria 10 devices.

Incremental compilation supports top-down, bottom-up, and team-based design flows. This feature facilitates modular, hierarchical, and team-based design flows where different designers compile their respective design sections in parallel. Furthermore, different designers or IP providers can develop and optimize different blocks of the design independently. These blocks can then be imported into the top level project.

Document Revision History for Intel Arria 10 Device Overview

| Document Version | Changes |
|------------------|--|
| 2018.04.09 | Updated the lowest V_{CC} from 0.83 V to 0.82 V in the topic listing a summary of the device features. |

| Date | Version | Changes |
|--------------|------------|---|
| January 2018 | 2018.01.17 | <ul style="list-style-type: none">• Updated the maximum data rate for HPS (Intel Arria 10 SX devices external memory interface DDR3 controller from 2,166 Mbps to 2,133 Mbps.• Updated maximum frequency supported for half rate QDR II and QDR II + SRAM to 633 MHz in <i>Memory Standards Supported by the Soft Memory Controller</i> table.• Updated transceiver backplane capability to 12.5 Gbps.• Removed transceiver speed grade 5 in <i>Sample Ordering Core and Available Options for Intel Arria 10 GX Devices</i> figure. |
| continued... | | |



| Date | Version | Changes |
|----------------|------------|--|
| | | <ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table. |
| September 2017 | 2017.09.20 | Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps. |
| July 2017 | 2017.07.13 | Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C". |
| July 2017 | 2017.07.06 | Added automotive temperature option to Intel Arria 10 GX device family. |
| May 2017 | 2017.05.08 | <ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks. |
| March 2017 | 2017.03.15 | <ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel. |
| October 2016 | 2016.10.31 | <ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers. |
| May 2016 | 2016.05.02 | <ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices. |
| February 2016 | 2016.02.11 | <ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section. |
| continued... | | |



| Date | Version | Changes |
|----------------|------------|---|
| December 2015 | 2015.12.14 | <ul style="list-style-type: none"> Updated the number of M20K memory blocks for Arria 10 GX 660 from 2133 to 2131 and corrected the total RAM bit from 48,448 Kb to 48,408 Kb. Corrected the number of DSP blocks for Arria 10 GX 660 from 1688 to 1687 in the table listing floating-point arithmetic resources. |
| November 2015 | 2015.11.02 | <ul style="list-style-type: none"> Updated the maximum resources for Arria 10 GX 220, GX 320, GX 480, GX 660, SX 220, SX 320, SX 480, and SX 660. Updated resource count for Arria 10 GX 320, GX 480, GX 660, SX 320, SX 480, a SX 660 devices in Number of Multipliers in Intel Arria 10 Devices table. Updated the available options for Arria 10 GX, GT, and SX. Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>. |
| June 2015 | 2015.06.15 | Corrected label for Intel Arria 10 GT product lines in the vertical migration figure. |
| May 2015 | 2015.05.15 | Corrected the DDR3 half rate and quarter rate maximum frequencies in the table that lists the memory standards supported by the Intel Arria 10 hard memory controller. |
| May 2015 | 2015.05.04 | <ul style="list-style-type: none"> Added support for 13.5G JESD204b in the Summary of Features table. Added a link to Arria 10 GT Channel Usage in the Arria 10 GT Package Plan topic. Added a note to the table, Maximum Resource Counts for Arria 10 GT devices. Updated the power requirements of the transceivers in the Low Power Serial Transceivers topic. |
| January 2015 | 2015.01.23 | <ul style="list-style-type: none"> Added floating point arithmetic features in the Summary of Features table. Updated the total embedded memory from 38.38 megabits (Mb) to 65.6 Mb. Updated the table that lists the memory standards supported by Intel Arria 10 devices. Removed support for DDR3U, LPDDR3 SDRAM, RLD RAM 2, and DDR2. Moved RLD RAM 3 support from hard memory controller to soft memory controller. RLD RAM 3 support uses hard PHY with soft memory controller. Added soft memory controller support for QDR IV. Updated the maximum resource count table to include the number of hard memory controllers available in each device variant. Updated the transceiver PCS data rate from 12.5 Gbps to 12 Gbps. Updated the max clock rate of PS, FPP x8, FPP x16, and Configuration via HPS from 125 MHz to 100 MHz. Added a feature for fractional synthesis PLLs: PLL cascading. Updated the HPS programmable general-purpose I/Os from 54 to 62. |
| September 2014 | 2014.09.30 | <ul style="list-style-type: none"> Corrected the 3 V I/O and LVDS I/O counts for F35 and F36 packages of Arria 10 GX. Corrected the 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 570 and 660. Removed 3 V I/O, LVDS I/O, and transceiver counts for the NF40 package of the Arria GX 900 and 1150. The NF40 package is not available for Arria 10 GX 900 and 1150. |
| continued... | | |



| Date | Version | Changes |
|---------------|------------|--|
| August 2014 | 2014.08.18 | <ul style="list-style-type: none"> Updated Memory (Kb) M20K maximum resources for Arria 10 GX 660 devices from 42,660 to 42,620. Added GPIO columns consisting of LVDS I/O Bank and 3V I/O Bank in the Package Plan table. Added how to use memory interface clock frequency higher than 533 MHz in the I/O vertical migration. Added information to clarify that RLDRAM3 support uses hard PHY with soft memory controller. Added variable precision DSP blocks support for floating-point arithmetic. |
| June 2014 | 2014.06.19 | Updated number of dedicated I/Os in the HPS block to 17. |
| February 2014 | 2014.02.21 | Updated transceiver speed grade options for GT devices in Figure 2. |
| February 2014 | 2014.02.06 | Updated data rate for Arria 10 GT devices from 28.1 Gbps to 28.3 Gbps. |
| December 2013 | 2013.12.10 | <ul style="list-style-type: none"> Updated the HPS memory standards support from LPDDR2 to LPDDR3. Updated HPS block diagram to include dedicated HPS I/O and FPGA Configuration blocks as well as repositioned SD/SDIO/MMC, DMA, SPI and NAND Flash with ECC blocks . |
| December 2013 | 2013.12.02 | Initial release. |