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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	427200
Number of Logic Elements/Cells	1150000
Total RAM Bits	68857856
Number of I/O	768
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FCBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/10ax115n3f45e2sg



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Intel® Arria® 10 Device Overview

The Intel® Arria® 10 device family consists of high-performance and power-efficient 20 nm mid-range FPGAs and SoCs.

Intel Arria 10 device family delivers:

- Higher performance than the previous generation of mid-range and high-end FPGAs.
- Power efficiency attained through a comprehensive set of power-saving technologies.

The Intel Arria 10 devices are ideal for high performance, power-sensitive, midrange applications in diverse markets.

Table 1. Sample Markets and Ideal Applications for Intel Arria 10 Devices

Market	Applications
Wireless	<ul style="list-style-type: none"> • Channel and switch cards in remote radio heads • Mobile backhaul
Wireline	<ul style="list-style-type: none"> • 40G/100G muxponders and transponders • 100G line cards • Bridging • Aggregation
Broadcast	<ul style="list-style-type: none"> • Studio switches • Servers and transport • Videoconferencing • Professional audio and video
Computing and Storage	<ul style="list-style-type: none"> • Flash cache • Cloud computing servers • Server acceleration
Medical	<ul style="list-style-type: none"> • Diagnostic scanners • Diagnostic imaging
Military	<ul style="list-style-type: none"> • Missile guidance and control • Radar • Electronic warfare • Secure communications

Related Information

Intel Arria 10 Device Handbook: Known Issues

Lists the planned updates to the *Intel Arria 10 Device Handbook* chapters.



Key Advantages of Intel Arria 10 Devices

Table 2. Key Advantages of the Intel Arria 10 Device Family

Advantage	Supporting Feature
Enhanced core architecture	<ul style="list-style-type: none">Built on TSMC's 20 nm process technology60% higher performance than the previous generation of mid-range FPGAs15% higher performance than the fastest previous-generation FPGA
High-bandwidth integrated transceivers	<ul style="list-style-type: none">Short-reach rates up to 25.8 Gigabits per second (Gbps)Backplane capability up to 12.5 GbpsIntegrated 10GBASE-KR and 40GBASE-KR4 Forward Error Correction (FEC)
Improved logic integration and hard IP blocks	<ul style="list-style-type: none">8-input adaptive logic module (ALM)Up to 65.6 megabits (Mb) of embedded memoryVariable-precision digital signal processing (DSP) blocksFractional synthesis phase-locked loops (PLLs)Hard PCI Express Gen3 IP blocksHard memory controllers and PHY up to 2,400 Megabits per second (Mbps)
Second generation hard processor system (HPS) with integrated ARM* Cortex*-A9* MPCore* processor	<ul style="list-style-type: none">Tight integration of a dual-core ARM Cortex-A9 MPCore processor, hard IP, and an FPGA in a single Intel Arria 10 system-on-a-chip (SoC)Supports over 128 Gbps peak bandwidth with integrated data coherency between the processor and the FPGA fabric
Advanced power savings	<ul style="list-style-type: none">Comprehensive set of advanced power saving featuresPower-optimized MultiTrack routing and core architectureUp to 40% lower power compared to previous generation of mid-range FPGAsUp to 60% lower power compared to previous generation of high-end FPGAs

Summary of Intel Arria 10 Features

Table 3. Summary of Features for Intel Arria 10 Devices

Feature	Description
Technology	<ul style="list-style-type: none">TSMC's 20-nm SoC process technologyAllows operation at a lower V_{CC} level of 0.82 V instead of the 0.9 V standard V_{CC} core voltage
Packaging	<ul style="list-style-type: none">1.0 mm ball-pitch FINELINE BGA packaging0.8 mm ball-pitch Ultra FINELINE BGA packagingMultiple devices with identical package footprints for seamless migration between different FPGA densitiesDevices with compatible package footprints allow migration to next generation high-end Stratix® 10 devicesRoHS, leaded⁽¹⁾, and lead-free (Pb-free) options
High-performance FPGA fabric	<ul style="list-style-type: none">Enhanced 8-input ALM with four registersImproved multi-track routing architecture to reduce congestion and improve compilation timeHierarchical core clocking architectureFine-grained partial reconfiguration
Internal memory blocks	<ul style="list-style-type: none">M20K—20-Kb memory blocks with hard error correction code (ECC)Memory logic array block (MLAB)—640-bit memory
continued...	

(1) Contact Intel for availability.



Feature	Description
	<ul style="list-style-type: none">Dynamic reconfiguration of the transceivers and PLLsFine-grained partial reconfiguration of the core fabricActive Serial x4 Interface
Power management	<ul style="list-style-type: none">SmartVIDLow static power device optionsProgrammable Power TechnologyIntel Quartus Prime integrated power analysis
Software and tools	<ul style="list-style-type: none">Intel Quartus Prime design suiteTransceiver toolkitPlatform Designer system integration toolDSP Builder for Intel FPGAsOpenCL™ supportIntel SoC FPGA Embedded Design Suite (EDS)

Related Information

[Intel Arria 10 Transceiver PHY Overview](#)

Provides details on Intel Arria 10 transceivers.

Intel Arria 10 Device Variants and Packages

Table 4. Device Variants for the Intel Arria 10 Device Family

Variant	Description
Intel Arria 10 GX	FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.
Intel Arria 10 GT	FPGA featuring: <ul style="list-style-type: none">17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.25.8 Gbps transceivers for supporting CAUI-4 and CEI-25G applications with CFP2 and CFP4 modules.
Intel Arria 10 SX	SoC integrating ARM-based HPS and FPGA featuring 17.4 Gbps transceivers for short reach applications with 12.5 backplane driving capability.

Intel Arria 10 GX

This section provides the available options, maximum resource counts, and package plan for the Intel Arria 10 GX devices.

The information in this section is correct at the time of publication. For the latest information and to get more details, refer to the Intel FPGA Product Selector.

Related Information

[Intel FPGA Product Selector](#)

Provides the latest information on Intel products.



Available Options

Figure 1. Sample Ordering Code and Available Options for Intel Arria 10 GX Devices



Related Information

Transceiver Performance for Intel Arria 10 GX/SX Devices

Provides more information about the transceiver speed grade.



Maximum Resources

Table 5. Maximum Resource Counts for Intel Arria 10 GX Devices (GX 160, GX 220, GX 270, GX 320, and GX 480)

Resource		Product Line				
		GX 160	GX 220	GX 270	GX 320	GX 480
Logic Elements (LE) (K)		160	220	270	320	480
ALM		61,510	80,330	101,620	119,900	183,590
Register		246,040	321,320	406,480	479,600	734,360
Memory (Kb)	M20K	8,800	11,740	15,000	17,820	28,620
	MLAB	1,050	1,690	2,452	2,727	4,164
Variable-precision DSP Block		156	192	830	985	1,368
18 x 19 Multiplier		312	384	1,660	1,970	2,736
PLL	Fractional Synthesis	6	6	8	8	12
	I/O	6	6	8	8	12
17.4 Gbps Transceiver		12	12	24	24	36
GPIO ⁽³⁾		288	288	384	384	492
LVDS Pair ⁽⁴⁾		120	120	168	168	222
PCIe Hard IP Block		1	1	2	2	2
Hard Memory Controller		6	6	8	8	12

⁽³⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁴⁾ Each LVDS I/O pair can be used as differential input or output.



Available Options

Figure 2. Sample Ordering Code and Available Options for Intel Arria 10 GT Devices





Maximum Resources

Table 10. Maximum Resource Counts for Intel Arria 10 GT Devices

Resource		Product Line	
		GT 900	GT 1150
Logic Elements (LE) (K)		900	1,150
ALM		339,620	427,200
Register		1,358,480	1,708,800
Memory (Kb)	M20K	48,460	54,260
	MLAB	9,386	12,984
Variable-precision DSP Block		1,518	1,518
18 x 19 Multiplier		3,036	3,036
PLL	Fractional Synthesis	32	32
	I/O	16	16
Transceiver	17.4 Gbps	72 ⁽⁵⁾	72 ⁽⁵⁾
	25.8 Gbps	6	6
GPIO ⁽⁶⁾		624	624
LVDS Pair ⁽⁷⁾		312	312
PCIe Hard IP Block		4	4
Hard Memory Controller		16	16

Related Information

Intel Arria 10 GT Channel Usage

Configuring GT/GX channels in Intel Arria 10 GT devices.

Package Plan

Table 11. Package Plan for Intel Arria 10 GT Devices

Refer to I/O and High Speed I/O in Intel Arria 10 Devices chapter for the number of 3 V I/O, LVDS I/O, and LVDS channels in each device package.

Product Line	SF45 (45 mm x 45 mm, 1932-pin FBGA)		
	3 V I/O	LVDS I/O	XCVR
GT 900	—	624	72
GT 1150	—	624	72

⁽⁵⁾ If all 6 GT channels are in use, 12 of the GX channels are not usable.

⁽⁶⁾ The number of GPIOs does not include transceiver I/Os. In the Intel Quartus Prime software, the number of user I/Os includes transceiver I/Os.

⁽⁷⁾ Each LVDS I/O pair can be used as differential input or output.

Figure 5. ALM for Intel Arria 10 Devices



The Intel Quartus Prime software optimizes your design according to the ALM logic structure and automatically maps legacy designs into the Intel Arria 10 ALM architecture.

Variable-Precision DSP Block

The Intel Arria 10 variable precision DSP blocks support fixed-point arithmetic and floating-point arithmetic.

Features for fixed-point arithmetic:

- High-performance, power-optimized, and fully registered multiplication operations
- 18-bit and 27-bit word lengths
- Two 18 x 19 multipliers or one 27 x 27 multiplier per DSP block
- Built-in addition, subtraction, and 64-bit double accumulation register to combine multiplication results
- Cascading 19-bit or 27-bit when pre-adder is disabled and cascading 18-bit when pre-adder is used to form the tap-delay line for filtering applications
- Cascading 64-bit output bus to propagate output results from one block to the next block without external logic support
- Hard pre-adder supported in 19-bit and 27-bit modes for symmetric filters
- Internal coefficient register bank in both 18-bit and 27-bit modes for filter implementation
- 18-bit and 27-bit systolic finite impulse response (FIR) filters with distributed output adder
- Biased rounding support



Features for floating-point arithmetic:

- A completely hardened architecture that supports multiplication, addition, subtraction, multiply-add, and multiply-subtract
- Multiplication with accumulation capability and a dynamic accumulator reset control
- Multiplication with cascade summation capability
- Multiplication with cascade subtraction capability
- Complex multiplication
- Direct vector dot product
- Systolic FIR filter

Table 15. Variable-Precision DSP Block Configurations for Intel Arria 10 Devices

Usage Example	Multiplier Size (Bit)	DSP Block Resources
Medium precision fixed point	Two 18 x 19	1
High precision fixed or Single precision floating point	One 27 x 27	1
Fixed point FFTs	One 19 x 36 with external adder	1
Very high precision fixed point	One 36 x 36 with external adder	2
Double precision floating point	One 54 x 54 with external adder	4

Table 16. Resources for Fixed-Point Arithmetic in Intel Arria 10 Devices

The table lists the variable-precision DSP resources by bit precision for each Intel Arria 10 device.

Variant	Product Line	Variable-precision DSP Block	Independent Input and Output Multiplications Operator		18 x 19 Multiplier Adder Sum Mode	18 x 18 Multiplier Adder Summed with 36 bit Input
			18 x 19 Multiplier	27 x 27 Multiplier		
Intel Arria 10 GX	GX 160	156	312	156	156	156
	GX 220	192	384	192	192	192
	GX 270	830	1,660	830	830	830
	GX 320	984	1,968	984	984	984
	GX 480	1,368	2,736	1,368	1,368	1,368
	GX 570	1,523	3,046	1,523	1,523	1,523
	GX 660	1,687	3,374	1,687	1,687	1,687
	GX 900	1,518	3,036	1,518	1,518	1,518
	GX 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 GT	GT 900	1,518	3,036	1,518	1,518	1,518
	GT 1150	1,518	3,036	1,518	1,518	1,518
Intel Arria 10 SX	SX 160	156	312	156	156	156
	SX 220	192	384	192	192	192
	SX 270	830	1,660	830	830	830

continued...



Types of Embedded Memory

The Intel Arria 10 devices contain two types of memory blocks:

- 20 Kb M20K blocks—blocks of dedicated memory resources. The M20K blocks are ideal for larger memory arrays while still providing a large number of independent ports.
- 640 bit memory logic array blocks (MLABs)—enhanced memory blocks that are configured from dual-purpose logic array blocks (LABs). The MLABs are ideal for wide and shallow memory arrays. The MLABs are optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines. Each MLAB is made up of ten adaptive logic modules (ALMs). In the Intel Arria 10 devices, you can configure these ALMs as ten 32 x 2 blocks, giving you one 32 x 20 simple dual-port SRAM block per MLAB.

Embedded Memory Capacity in Intel Arria 10 Devices

Table 18. Embedded Memory Capacity and Distribution in Intel Arria 10 Devices

Variant	Product Line	M20K		MLAB		Total RAM Bit (Kb)
		Block	RAM Bit (Kb)	Block	RAM Bit (Kb)	
Intel Arria 10 GX	GX 160	440	8,800	1,680	1,050	9,850
	GX 220	587	11,740	2,703	1,690	13,430
	GX 270	750	15,000	3,922	2,452	17,452
	GX 320	891	17,820	4,363	2,727	20,547
	GX 480	1,431	28,620	6,662	4,164	32,784
	GX 570	1,800	36,000	8,153	5,096	41,096
	GX 660	2,131	42,620	9,260	5,788	48,408
	GX 900	2,423	48,460	15,017	9,386	57,846
	GX 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 GT	GT 900	2,423	48,460	15,017	9,386	57,846
	GT 1150	2,713	54,260	20,774	12,984	67,244
Intel Arria 10 SX	SX 160	440	8,800	1,680	1,050	9,850
	SX 220	587	11,740	2,703	1,690	13,430
	SX 270	750	15,000	3,922	2,452	17,452
	SX 320	891	17,820	4,363	2,727	20,547
	SX 480	1,431	28,620	6,662	4,164	32,784
	SX 570	1,800	36,000	8,153	5,096	41,096
	SX 660	2,131	42,620	9,260	5,788	48,408

Embedded Memory Configurations for Single-port Mode

Table 19. Single-port Embedded Memory Configurations for Intel Arria 10 Devices

This table lists the maximum configurations supported for single-port RAM and ROM modes.

Memory Block	Depth (bits)	Programmable Width
MLAB	32	x16, x18, or x20
	64 ⁽¹⁰⁾	x8, x9, x10
M20K	512	x40, x32
	1K	x20, x16
	2K	x10, x8
	4K	x5, x4
	8K	x2
	16K	x1

Clock Networks and PLL Clock Sources

The clock network architecture is based on Intel's global, regional, and peripheral clock structure. This clock structure is supported by dedicated clock input pins, fractional clock synthesis PLLs, and integer I/O PLLs.

Clock Networks

The Intel Arria 10 core clock networks are capable of up to 800 MHz fabric operation across the full industrial temperature range. For the external memory interface, the clock network supports the hard memory controller with speeds up to 2,400 Mbps in a quarter-rate transfer.

To reduce power consumption, the Intel Quartus Prime software identifies all unused sections of the clock network and powers them down.

Fractional Synthesis and I/O PLLs

Intel Arria 10 devices contain up to 32 fractional synthesis PLLs and up to 16 I/O PLLs that are available for both specific and general purpose uses in the core:

- Fractional synthesis PLLs—located in the column adjacent to the transceiver blocks
- I/O PLLs—located in each bank of the 48 I/Os

Fractional Synthesis PLLs

You can use the fractional synthesis PLLs to:

- Reduce the number of oscillators that are required on your board
- Reduce the number of clock pins that are used in the device by synthesizing multiple clock frequencies from a single reference clock source

⁽¹⁰⁾ Supported through software emulation and consumes additional MLAB blocks.

- Series (R_S) and parallel (R_T) on-chip termination (OCT) for all I/O banks with OCT calibration to limit the termination impedance variation
- On-chip dynamic termination that has the ability to swap between series and parallel termination, depending on whether there is read or write on a common bus for signal integrity
- Easy timing closure support using the hard read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture

External Memory Interface

Intel Arria 10 devices offer massive external memory bandwidth, with up to seven 32-bit DDR4 memory interfaces running at up to 2,400 Mbps. This bandwidth provides additional ease of design, lower power, and resource efficiencies of hardened high-performance memory controllers.

The memory interface within Intel Arria 10 FPGAs and SoCs delivers the highest performance and ease of use. You can configure up to a maximum width of 144 bits when using the hard or soft memory controllers. If required, you can bypass the hard memory controller and use a soft controller implemented in the user logic.

Each I/O contains a hardened DDR read/write path (PHY) capable of performing key memory interface functionality such as read/write leveling, FIFO buffering to lower latency and improve margin, timing calibration, and on-chip termination.

The timing calibration is aided by the inclusion of hard microcontrollers based on Intel's Nios® II technology, specifically tailored to control the calibration of multiple memory interfaces. This calibration allows the Intel Arria 10 device to compensate for any changes in process, voltage, or temperature either within the Intel Arria 10 device itself, or within the external memory device. The advanced calibration algorithms ensure maximum bandwidth and robust timing margin across all operating conditions.

In addition to parallel memory interfaces, Intel Arria 10 devices support serial memory technologies such as the Hybrid Memory Cube (HMC). The HMC is supported by the Intel Arria 10 high-speed serial transceivers which connect up to four HMC links, with each link running at data rates up to 15 Gbps.

Related Information

[External Memory Interface Spec Estimator](#)

Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in IntelFPGAs.

Memory Standards Supported by Intel Arria 10 Devices

The I/Os are designed to provide high performance support for existing and emerging external memory standards.



The scalable hard IP supports multiple independent 10GbE ports while using a single PLL for all the 10GBASE-R PCS instantiations, which saves on core logic resources and clock networks:

- Simplifies multiport 10GbE systems compared to XAUI interfaces that require an external XAUI-to-10G PHY.
- Incorporates Electronic Dispersion Compensation (EDC), which enables direct connection to standard 10 Gbps XFP and SFP+ pluggable optical modules.
- Supports backplane Ethernet applications and includes a hard 10GBASE-KR Forward Error Correction (FEC) circuit that you can use for 10 Gbps and 40 Gbps applications.

The 10 Gbps Ethernet PCS hard IP and 10GBASE-KR FEC are present in every transceiver channel.

Related Information

[PCS Features](#) on page 30

Low Power Serial Transceivers

Intel Arria 10 FPGAs and SoCs include lowest power transceivers that deliver high bandwidth, throughput and low latency.

Intel Arria 10 devices deliver the industry's lowest power consumption per transceiver channel:

- 12.5 Gbps transceivers at as low as 242 mW
- 10 Gbps transceivers at as low as 168 mW
- 6 Gbps transceivers at as low as 117 mW

Intel Arria 10 transceivers support various data rates according to application:

- Chip-to-chip and chip-to-module applications—from 1 Gbps up to 25.8 Gbps
- Long reach and backplane applications—from 1 Gbps up to 12.5 with advanced adaptive equalization
- Critical power sensitive applications—from 1 Gbps up to 11.3 Gbps using lower power modes

The combination of 20 nm process technology and architectural advances provide the following benefits:

- Significant reduction in die area and power consumption
- Increase of up to two times in transceiver I/O density compared to previous generation devices while maintaining optimal signal integrity
- Up to 72 total transceiver channels—you can configure up to 6 of these channels to run as fast as 25.8 Gbps
- All channels feature continuous data rate support up to the maximum rated speed



PCS	Description
Standard PCS	<ul style="list-style-type: none"> Operates at a data rate up to 12 Gbps Supports protocols such as PCI-Express, CPRI 4.2+, GigE, IEEE 1588 in Hard PCS Implements other protocols using Basic/Custom (Standard PCS) transceiver configuration rules.
Enhanced PCS	<ul style="list-style-type: none"> Performs functions common to most serial data industry standards, such as word alignment, encoding/decoding, and framing, before data is sent or received off-chip through the PMA Handles data transfer to and from the FPGA fabric Handles data transfer internally to and from the PMA Provides frequency compensation Performs channel bonding for multi-channel low skew applications
PCIe Gen3 PCS	<ul style="list-style-type: none"> Supports the seamless switching of Data and Clock between the Gen1, Gen2, and Gen3 data rates Provides support for PIPE 3.0 features Supports the PIPE interface with the Hard IP enabled, as well as with the Hard IP bypassed

Related Information

- [PCIe Gen1, Gen2, and Gen3 Hard IP](#) on page 26
- [Interlaken Support](#) on page 26
- [10 Gbps Ethernet Support](#) on page 26

PCS Protocol Support

This table lists some of the protocols supported by the Intel Arria 10 transceiver PCS. For more information about the blocks in the transmitter and receiver data paths, refer to the related information.

Protocol	Data Rate (Gbps)	Transceiver IP	PCS Support
PCIe Gen3 x1, x2, x4, x8	8.0	Native PHY (PIPE)	Standard PCS and PCIe Gen3 PCS
PCIe Gen2 x1, x2, x4, x8	5.0	Native PHY (PIPE)	Standard PCS
PCIe Gen1 x1, x2, x4, x8	2.5	Native PHY (PIPE)	Standard PCS
1000BASE-X Gigabit Ethernet	1.25	Native PHY	Standard PCS
1000BASE-X Gigabit Ethernet with IEEE 1588v2	1.25	Native PHY	Standard PCS
10GBASE-R	10.3125	Native PHY	Enhanced PCS
10GBASE-R with IEEE 1588v2	10.3125	Native PHY	Enhanced PCS
10GBASE-R with KR FEC	10.3125	Native PHY	Enhanced PCS
10GBASE-KR and 1000BASE-X	10.3125	1G/10GbE and 10GBASE-KR PHY	Standard PCS and Enhanced PCS
Interlaken (CEI-6G/11G)	3.125 to 17.4	Native PHY	Enhanced PCS
SFI-S/SFI-5.2	11.2	Native PHY	Enhanced PCS
10G SDI	10.692	Native PHY	Enhanced PCS
continued...			



Table 24. Improvements in 20 nm HPS

This table lists the key improvements of the 20 nm HPS compared to the 28 nm HPS.

Advantages/ Improvements	Description
Increased performance and overdrive capability	While the nominal processor frequency is 1.2 GHz, the 20 nm HPS offers an “overdrive” feature which enables a higher processor operating frequency. This requires a higher supply voltage value that is unique to the HPS and may require a separate regulator.
Increased processor memory bandwidth and DDR4 support	Up to 64-bit DDR4 memory at 2,400 Mbps support is available for the processor. The hard memory controller for the HPS comprises a multi-port front end that manages connections to a single port memory controller. The multi-port front end allows logic core and the HPS to share ports and thereby the available bandwidth of the memory controller.
Flexible I/O sharing	An advanced I/O pin muxing scheme allows improved sharing of I/O between the HPS and the core logic. The following types of I/O are available for SoC: <ul style="list-style-type: none">• 17 dedicated I/Os—physically located inside the HPS block and are not accessible to logic within the core. The 17 dedicated I/Os are used for HPS clock, resets, and interfacing with boot devices, QSPI, and SD/MMC.• 48 direct shared I/O—located closest to the HPS block and are ideal for high speed HPS peripherals such as EMAC, USB, and others. There is one bank of 48 I/Os that supports direct sharing where the 48 I/Os can be shared 12 I/Os at a time.• Standard (shared) I/O—all standard I/Os can be shared by the HPS peripherals and any logic within the core. For designs where more than 48 I/Os are required to fully use all the peripherals in the HPS, these I/Os can be connected through the core logic.
EMAC core	Three EMAC cores are available in the HPS. The EMAC cores enable an application to support two redundant Ethernet connections; for example, backplane, or two EMAC cores for managing IEEE 1588 time stamp information while allowing a third EMAC core for debug and configuration. All three EMACs can potentially share the same time stamps, simplifying the 1588 time stamping implementation. A new serial time stamp interface allows core logic to access and read the time stamp values. The integrated EMAC controllers can be connected to external Ethernet PHY through the provided MDIO or I ² C interface.
On-chip memory	The on-chip memory is updated to 256 KB support and can support larger data sets and real time algorithms.
ECC enhancements	Improvements in L2 Cache ECC management allow identification of errors down to the address level. ECC enhancements also enable improved error injection and status reporting via the introduction of new memory mapped access to syndrome and data signals.
HPS to FPGA Interconnect Backbone	Although the HPS and the Logic Core can operate independently, they are tightly coupled via a high-bandwidth system interconnect built from high-performance ARM AMBA AXI bus bridges. IP bus masters in the FPGA fabric have access to HPS bus slaves via the FPGA-to-HPS interconnect. Similarly, HPS bus masters have access to bus slaves in the core fabric via the HPS-to-FPGA bridge. Both bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters within the core fabric can share the HPS SDRAM controller with the processor. Additionally, the processor can be used to configure the core fabric under program control via a dedicated 32-bit configuration port.
FPGA configuration and HPS booting	The FPGA fabric and HPS in the SoCs are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power. You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility.
Security	New security features have been introduced for anti-tamper management, secure boot, encryption (AES), and authentication (SHA).



Features of the HPS

The HPS has the following features:

- 1.2-GHz, dual-core ARM Cortex-A9 MPCore processor with up to 1.5-GHz via overdrive
 - ARMv7-A architecture that runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java byte codes in Jazelle style
 - Superscalar, variable length, out-of-order pipeline with dynamic branch prediction
 - Instruction Efficiency 2.5 MIPS/MHz, which provides total performance of 7500 MIPS at 1.5 GHz
- Each processor core includes:
 - 32 KB of L1 instruction cache, 32 KB of L1 data cache
 - Single- and double-precision floating-point unit and NEON media engine
 - CoreSight debug and trace technology
 - Snoop Control Unit (SCU) and Acceleration Coherency Port (ACP)
- 512 KB of shared L2 cache
- 256 KB of scratch RAM
- Hard memory controller with support for DDR3, DDR4 and optional error correction code (ECC) support
- Multiport Front End (MPFE) Scheduler interface to the hard memory controller
- 8-channel direct memory access (DMA) controller
- QSPI flash controller with SIO, DIO, QIO SPI Flash support
- NAND flash controller (ONFI 1.0 or later) with DMA and ECC support, updated to support 8 and 16-bit Flash devices and new command DMA to offload CPU for fast power down recovery
- Updated SD/SDIO/MMC controller to eMMC 4.5 with DMA with CE-ATA digital command support
- 3 10/100/1000 Ethernet media access control (MAC) with DMA
- 2 USB On-the-Go (OTG) controllers with DMA
- 5 I²C controllers (3 can be used by EMAC for MIO to external PHY)
- 2 UART 16550 Compatible controllers
- 4 serial peripheral interfaces (SPI) (2 Master, 2 Slaves)
- 62 programmable general-purpose I/Os, which includes 48 direct share I/Os that allows the HPS peripherals to connect directly to the FPGA I/Os
- 7 general-purpose timers
- 4 watchdog timers
- Anti-tamper, Secure Boot, Encryption (AES) and Authentication (SHA)

System Peripherals and Debug Access Port

Each Ethernet MAC, USB OTG, NAND flash controller, and SD/MMC controller module has an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels of high-bandwidth data transfers. Peripherals that communicate off-chip are multiplexed with other peripherals at the HPS pin level. This allows you to choose which peripherals interface with other devices on your PCB.

The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS-FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the FPGA fabric to issue transactions to slaves in the HPS.
- HPS-to-FPGA Avalon/AMBA AXI bridge—a high-performance bus supporting 32, 64, and 128 bit data widths that allows the HPS to issue transactions to slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower latency 32 bit width bus that allows the HPS to issue transactions to soft peripherals in the FPGA fabric. This bridge is primarily used for control and status register (CSR) accesses to peripherals in the FPGA fabric.

The HPS-FPGA AXI bridges allow masters in the FPGA fabric to communicate with slaves in the HPS logic, and vice versa. For example, the HPS-to-FPGA AXI bridge allows you to share memories instantiated in the FPGA fabric with one or both microprocessors in the HPS, while the FPGA-to-HPS AXI bridge allows logic in the FPGA fabric to access the memory and peripherals in the HPS.

Each HPS-FPGA bridge also provides asynchronous clock crossing for data transferred between the FPGA fabric and the HPS.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that are shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to six individual ports for access by masters implemented in the FPGA fabric.

The HPS SDRAM controller supports up to 3 masters (command ports), 3x 64-bit read data ports and 3x 64-bit write data ports.

To maximize memory performance, the SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features.



Scheme	Data Width	Max Clock Rate (MHz)	Max Data Rate (Mbps) ⁽¹³⁾	Decompression	Design Security ⁽¹⁴⁾	Partial Reconfiguration ⁽¹⁵⁾	Remote System Update
Fast passive parallel (FPP) through CPLD or external microcontroller	8 bits	100	3200	Yes	Yes	Yes ⁽¹⁷⁾	PFL IP core
	16 bits			Yes	Yes		
	32 bits			Yes	Yes		
Configuration via HPS	16 bits	100	3200	Yes	Yes	Yes ⁽¹⁷⁾	—
	32 bits			Yes	Yes		
Configuration via Protocol [CvP (PCIe*)]	x1, x2, x4, x8 lanes	—	8000	Yes	Yes	Yes ⁽¹⁶⁾	—

You can configure Intel Arria 10 devices through PCIe using Configuration via Protocol (CvP). The Intel Arria 10 CvP implementation conforms to the PCIe 100 ms power-up-to-active time requirement.

SEU Error Detection and Correction

Intel Arria 10 devices offer robust and easy-to-use single-event upset (SEU) error detection and correction circuitry.

The detection and correction circuitry includes protection for Configuration RAM (CRAM) programming bits and user memories. The CRAM is protected by a continuously running CRC error detection circuit with integrated ECC that automatically corrects one or two errors and detects higher order multi-bit errors. When more than two errors occur, correction is available through reloading of the core programming file, providing a complete design refresh while the FPGA continues to operate.

The physical layout of the Intel Arria 10 CRAM array is optimized to make the majority of multi-bit upsets appear as independent single-bit or double-bit errors which are automatically corrected by the integrated CRAM ECC circuitry. In addition to the CRAM protection, the M20K memory blocks also include integrated ECC circuitry and are layout-optimized for error detection and correction. The MLAB does not have ECC.

Power Management

Intel Arria 10 devices leverage the advanced 20 nm process technology, a low 0.9 V core power supply, an enhanced core architecture, and several optional power reduction techniques to reduce total power consumption by as much as 40% compared to Arria V devices and as much as 60% compared to Stratix V devices.

⁽¹³⁾ Enabling either compression or design security features affects the maximum data rate. Refer to the Intel Arria 10 Device Datasheet for more information.

⁽¹⁴⁾ Encryption and compression cannot be used simultaneously.

⁽¹⁵⁾ Partial reconfiguration is an advanced feature of the device family. If you are interested in using partial reconfiguration, contact Intel for support.

⁽¹⁷⁾ Supported at a maximum clock rate of 100 MHz.



Date	Version	Changes
		<ul style="list-style-type: none"> Removed package code 40, low static power, SmartVID, industrial, and military operating temperature support from <i>Sample Ordering Core and Available Options for Intel Arria 10 GT Devices</i> figure. Updated short reach transceiver rate for Intel Arria 10 GT devices to 25.8 Gbps. Removed On-Die Instrumentation — EyeQ and Jitter Margin Tool support from <i>PMA Features of the Transceivers in Intel Arria 10 Devices</i> table.
September 2017	2017.09.20	Updated the maximum speed of the DDR4 external memory interface from 1,333 MHz/2,666 Mbps to 1,200 MHz/2,400 Mbps.
July 2017	2017.07.13	Corrected the automotive temperature range in the figure showing the available options for the Intel Arria 10 GX devices from "-40°C to 100°C" to "-40°C to 125°C".
July 2017	2017.07.06	Added automotive temperature option to Intel Arria 10 GX device family.
May 2017	2017.05.08	<ul style="list-style-type: none"> Corrected protocol names with "1588" to "IEEE 1588v2". Updated the vertical migration table to remove vertical migration between Intel Arria 10 GX and Intel Arria 10 SX device variants. Removed all "Preliminary" marks.
March 2017	2017.03.15	<ul style="list-style-type: none"> Removed the topic about migration from Intel Arria 10 to Intel Stratix 10 devices. Rebranded as Intel.
October 2016	2016.10.31	<ul style="list-style-type: none"> Removed package F36 from Intel Arria 10 GX devices. Updated Intel Arria 10 GT sample ordering code and maximum GX transceiver count. Intel Arria 10 GT devices are available only in the SF45 package option with a maximum of 72 transceivers.
May 2016	2016.05.02	<ul style="list-style-type: none"> Updated the FPGA Configuration and HPS Booting topic. Remove V_{CC} PowerManager from the Summary of Features, Power Management and Arria 10 Device Variants and packages topics. This feature is no longer supported in Arria 10 devices. Removed LPDDR3 from the Memory Standards Supported by the HPS Hard Memory Controller table in the Memory Standards Supported by Intel Arria 10 Devices topic. This standard is only supported by the FPGA. Removed transceiver speed grade 5 from the Device Variants and Packages topic for Arria 10 GX and SX devices.
February 2016	2016.02.11	<ul style="list-style-type: none"> Changed the maximum Arria 10 GT datarate to 25.8 Gbps and the minimum datarate to 1 Gbps globally. Revised the state for Core clock networks in the Summary of Features topic. Changed the transceiver parameters in the "Summary of Features for Arria 10 Devices" table. Changed the transceiver parameters in the "Maximum Resource Counts for Arria 10 GT Devices" table. Changed the package availability for GT devices in the "Package Plan for Arria 10 GT Devices" table. Changed the package configurations for GT devices in the "Migration Capability Across Arria 10 Product Lines" figure. Changed transceiver parameters in the "Low Power Serial Transceivers" section. Changed the transceiver descriptions in the "Device Variants for the Arria 10 Device Family" table. Changed the "Sample Ordering Code and Available Options for Arria 10 GT Devices" figure. Changed the datarates for GT devices in the "PMA Features" section. Changed the datarates for GT devices in the "PCS Features" section.
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