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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 56800E |
| Core Size | 16-Bit |
| Speed | 40MHz |
| Connectivity | EBI/EMI, SCI, SPI |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 62 |
| Program Memory Size | 512KB (256K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 16 |
| Voltage - Supply (Vcc/Vdd) | 2.25V ~ 3.6V |
| Data Converters | A/D 16x12b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-LQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8166vfve |

## Document Revision History

| Version History | Description of Change |
|---|---|
| Rev 0 | Pre-release, Alpha customers only |
| Rev 1.0 | Initial Public Release |
| Rev 2.0 | Added output voltage maximum value and note to clarify in **Table 10-1**; also removed overall life expectancy note, since life expectancy is dependent on customer usage and must be determined by reliability engineering. Clarified value and unit measure for Maximum allowed $P_D$ in **Table 10-3**. Corrected note about average value for Flash Data Retention in **Table 10-4**. Added new RoHS-compliant orderable part numbers in **Table 13-1**. |
| Rev 3.0 | Deleted formula for Max Ambient Operating Temperature (Automotive) and Max Ambient Operating Temperature (Industrial) and corrected Flash Endurance to 10,000 in **Table 10-4**. Added RoHS-compliance and “pb-free” language to back cover |
| Rev 4.0 | Added information/corrected state during reset in **Table 2-2**. Clarified external reference crystal frequency for PLL in **Table 10-14** by increasing maximum value to 8.4MHz. |
| Rev 5.0 | Replaced “Tri-stated” with an explanation in State During Reset column in **Table 2-2**. |
| Rev. 6 | • Added the following note to the description of the TMS signal in **Table 2-2**:<br>**Note:** Always tie the TMS pin to $V_{DD}$ through a 2.2K resistor.<br>• Added the following note to the description of the $\overline{\text{TRST}}$ signal in **Table 2-2**:<br>**Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to $V_{SS}$. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to $V_{SS}$ through a 1K resistor. |
| Rev. 7 | • Remove pullup comment from PWM pins in **Table 2-2**.<br>• Add **Figure 10-1** showing current voltage characteristics.<br>• In **Table 10-24**, correct interpretation of Calibration Factors to be viewed as worst case factors. |

**Please see http://www.freescale.com for the most current data sheet revision.**

## 1.5 Product Documentation

The documents in **Table 1-3** are required for a complete description and proper design with the 56F8366/56F8166 devices. Documentation is available from local Freescale distributors, Freescale semiconductor sales offices, Freescale Literature Distribution Centers, or online at **http://www.freescale.com.**

**Table 1-3 Chip Documentation**

| Topic | Description | Order Number |
|---|---|---|
| DSP56800E Reference Manual | Detailed description of the 56800E family architecture, and 16-bit controller core processor and the instruction set | DSP56800ERM |
| 56F8300 Peripheral User Manual | Detailed description of peripherals of the 56F8300 devices | MC56F8300UM |
| 56F8300 SCI/CAN Bootloader User Manual | Detailed description of the SCI/CAN Bootloaders 56F8300 family of devices | MC56F83xxBLUM |
| 56F8366/56F8166 Technical Data Sheet | Electrical and timing specifications, pin descriptions, and package descriptions (this document) | MC56F8366 |
| 56F8366 Errata | Details any chip issues that might be present | MC56F8366E<br>MC56F8166E |

## 1.6 Data Sheet Conventions

This data sheet uses the following conventions:

| | |
|---|---|
| $\overline{\text{OVERBAR}}$ | This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low. |
| “asserted” | A high true (active high) signal is high or a low true (active low) signal is low. |
| “deasserted” | A high true (active high) signal is low or a low true (active low) signal is high. |

| Examples: | Signal/Symbol | Logic State | Signal State | Voltage[1] |
|---|---|---|---|---|
| | $\overline{\text{PIN}}$ | True | Asserted | $V_{IL}/V_{OL}$ |
| | $\overline{\text{PIN}}$ | False | Deasserted | $V_{IH}/V_{OH}$ |
| | PIN | True | Asserted | $V_{IH}/V_{OH}$ |
| | PIN | False | Deasserted | $V_{IL}/V_{OL}$ |

1. Values for VIL, VOL, VIH, and VOH are defined by individual product specifications.

## 2.2 Signal Pins

After reset, each pin is configured for its primary function (listed first). Any alternate functionality must be programmed.

**Note:** *Signals in italics are NOT available in the 56F8166 device.*

If the "State During Reset" lists more than one state for a pin, the first state is the actual reset state. Other states show the reset condition of the alternate function, which you get if the alternate pin function is selected without changing the configuration of the alternate peripheral. For example, the A8/GPIOA0 pin shows that it is tri-stated during reset. If the GPIOA_PER is changed to select the GPIO function of the pin, it will become an input if no other registers are changed.

**Table 2-2 Signal and Package Information for the 144-Pin LQFP**

| Signal Name | Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| $V_{DD\_IO}$ | 1 | Supply | | **I/O Power** — This pin supplies 3.3V power to the chip I/O interface and also the Processor core throught the on-chip voltage regulator, if it is enabled. |
| $V_{DD\_IO}$ | 16 | | | |
| $V_{DD\_IO}$ | 31 | | | |
| $V_{DD\_IO}$ | 38 | | | |
| $V_{DD\_IO}$ | 66 | | | |
| $V_{DD\_IO}$ | 84 | | | |
| $V_{DD\_IO}$ | 119 | | | |
| $V_{DDA\_ADC}$ | 102 | Supply | | **ADC Power** — This pin supplies 3.3V power to the ADC modules. It must be connected to a clean analog power supply. |
| $V_{DDA\_OSC\_PLL}$ | 80 | Supply | | **Oscillator** and **PLL Power** — This pin supplies 3.3V power to the OSC and to the internal regulator that in turn supplies the Phase Locked Loop. It must be connected to a clean analog power supply. |
| $V_{SS}$ | 27 | Supply | | $V_{SS}$ — These pins provide ground for chip logic and I/O drivers. |
| $V_{SS}$ | 37 | | | |
| $V_{SS}$ | 63 | | | |
| $V_{SS}$ | 69 | | | |
| $V_{SS}$ | 144 | | | |

## Table 2-2 Signal and Package Information for the 144-Pin LQFP

| Signal Name | Pin No. | Type | State During Reset | Signal Description |
|---|---|---|---|---|
| ***PHASEA1*** | 6 | Schmitt Input | Input, pull-up enabled | **Phase A1** — Quadrature Decoder 1, PHASEA input for decoder 1. |
| ***(TB0)*** | | Schmitt Input/ Output | | **TB0** — Timer B, Channel 0 |
| **(SCLK1)** | | Schmitt Input/ Output | | **SPI 1 Serial Clock** — In the master mode, this pin serves as an output, clocking slaved listeners. In slave mode, this pin serves as the data clock input. To activate the SPI function, set the PHSA_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**. |
| **(GPIOC0)** | | Schmitt Input/ Output | | **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>In the 56F8366, the default state after reset is PHASEA1.<br><br>In the 56F8166, the default state is not one of the functions offered and must be reconfigured.<br><br>To deactivate the internal pull-up resistor, clear bit 0 in the GPIOC_PUR register. |
| ***PHASEB1*** | 7 | Schmitt Input | Input, pull-up enabled | **Phase B1** — Quadrature Decoder 1, PHASEB input for decoder 1. |
| ***(TB1)*** | | Schmitt Input/ Output | | **TB1** — Timer B, Channel 1 |
| **(MOSI1)** | | Schmitt Input/ Output | | **SPI 1 Master Out/Slave In** — This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI line a half-cycle before the clock edge the slave device uses to latch the data. To activate the SPI function, set the PHSB_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**. |
| **(GPIOC1)** | | Schmitt Input/ Output | | **Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin.<br><br>In the 56F8366, the default state after reset is PHASEB1.<br><br>In the 56F8166, the default state is not one of the functions offered and must be reconfigured.<br><br>To deactivate the internal pull-up resistor, clear bit 1 in the GPIOC_PUR register. |

# Part 3 On-Chip Clock Synthesis (OCCS)

## 3.1 Introduction

Refer to the OCCS chapter of the **56F8300 Peripheral User Manual** for a full description of the OCCS. The material contained here identifies the specific features of the OCCS design. **Figure 3-1** shows the specific OCCS block diagram to reference in the OCCS chapter in the **56F8300 Peripheral User Manual**.

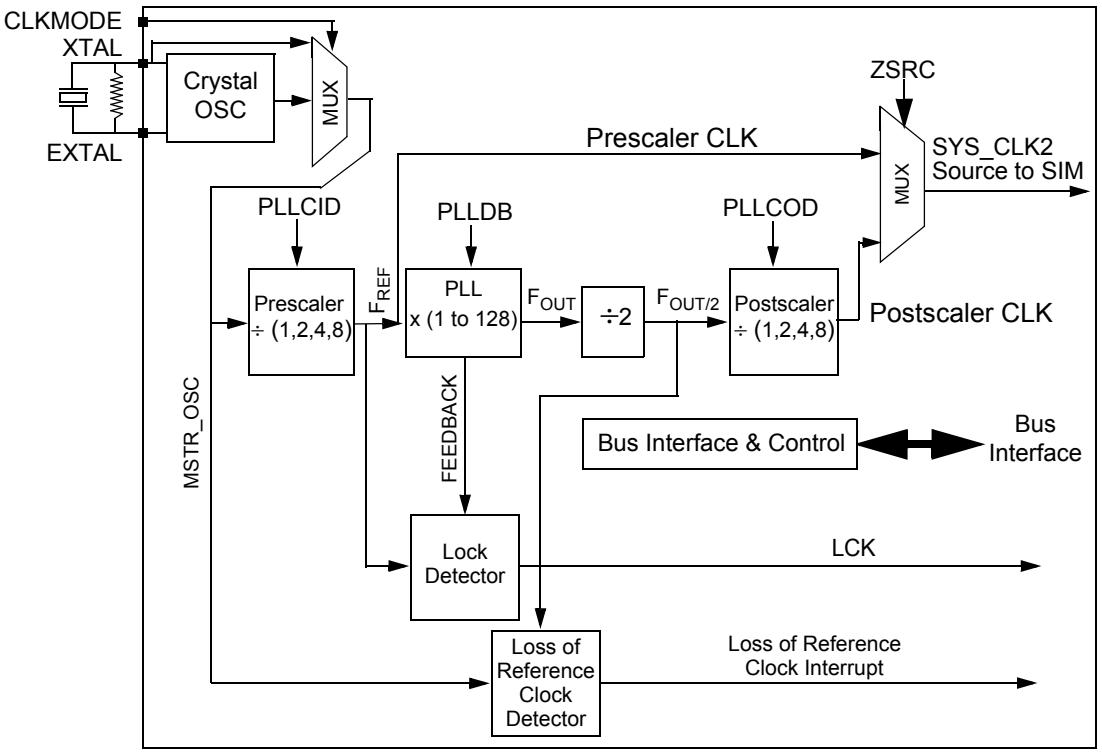


**Figure 3-1 OCCS Block Diagram**

## 3.2 External Clock Operation

The system clock can be derived from an external crystal, ceramic resonator, or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal or ceramic resonator must be connected between the EXTAL and XTAL pins.

### 3.2.1 Crystal Oscillator

The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 10-15**. A recommended crystal oscillator circuit is shown in **Figure 3-2**. Follow the crystal supplier's recommendations when selecting a crystal, since crystal parameters determine the component values required to provide maximum stability and reliable start-up.

## 4.6 EOnCE Memory Map

**Table 4-8 EOnCE Memory Map**

| Address | Register Acronym | Register Name |
|---|---|---|
| | | Reserved |
| X:$FF FF8A | OESCR | External Signal Control Register |
| | | Reserved |
| X:$FF FF8E | OBCNTR | Breakpoint Unit [0] Counter |
| | | Reserved |
| X:$FF FF90 | OBMSK (32 bits) | Breakpoint 1 Unit [0] Mask Register |
| X:$FF FF91 | — | Breakpoint 1 Unit [0] Mask Register |
| X:$FF FF92 | OBAR2 (32 bits) | Breakpoint 2 Unit [0] Address Register |
| X:$FF FF93 | — | Breakpoint 2 Unit [0] Address Register |
| X:$FF FF94 | OBAR1 (24 bits) | Breakpoint 1 Unit [0] Address Register |
| X:$FF FF95 | — | Breakpoint 1 Unit [0] Address Register |
| X:$FF FF96 | OBCR (24 bits) | Breakpoint Unit [0] Control Register |
| X:$FF FF97 | — | Breakpoint Unit [0] Control Register |
| X:$FF FF98 | OTB (21-24 bits/stage) | Trace Buffer Register Stages |
| X:$FF FF99 | — | Trace Buffer Register Stages |
| X:$FF FF9A | OTBPR (8 bits) | Trace Buffer Pointer Register |
| X:$FF FF9B | OTBCR | Trace Buffer Control Register |
| X:$FF FF9C | OBASE (8 bits) | Peripheral Base Address Register |
| X:$FF FF9D | OSR | Status Register |
| X:$FF FF9E | OSCNTR (24 bits) | Instruction Step Counter |
| X:$FF FF9F | — | Instruction Step Counter |
| X:$FF FFA0 | OCR (bits) | Control Register |
| | | Reserved |
| X:$FF FFFC | OCLSR (8 bits) | Core Lock / Unlock Status Register |
| X:$FF FFFD | OTXRXSR (8 bits) | Transmit and Receive Status and Control Register |
| X:$FF FFFE | OTX / ORX (32 bits) | Transmit Register / Receive Register |
| X:$FF FFFF | OTX1 / ORX1 | Transmit Register Upper Word<br>Receive Register Upper Word |

## Table 4-11 Quad Timer A Registers Address Map (Continued) (TMRA_BASE = $00 F040)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| TMRA3_CNTR | $35 | Counter Register |
| TMRA3_CTRL | $36 | Control Register |
| TMRA3_SCR | $37 | Status and Control Register |
| TMRA3_CMPLD1 | $38 | Comparator Load Register 1 |
| TMRA3_CMPLD2 | $39 | Comparator Load Register 2 |
| TMRA3_COMSC | $3A | Comparator Status and Control Register |

## Table 4-12 Quad Timer B Registers Address Map (TMRB_BASE = $00 F080)

***Quad Timer B is NOT available in the 56F8166 device***

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| TMRB0_CMP1 | $0 | Compare Register 1 |
| TMRB0_CMP2 | $1 | Compare Register 2 |
| TMRB0_CAP | $2 | Capture Register |
| TMRB0_LOAD | $3 | Load Register |
| TMRB0_HOLD | $4 | Hold Register |
| TMRB0_CNTR | $5 | Counter Register |
| TMRB0_CTRL | $6 | Control Register |
| TMRB0_SCR | $7 | Status and Control Register |
| TMRB0_CMPLD1 | $8 | Comparator Load Register 1 |
| TMRB0_CMPLD2 | $9 | Comparator Load Register 2 |
| TMRB0_COMSCR | $A | Comparator Status and Control Register |
| | | Reserved |
| TMRB1_CMP1 | $10 | Compare Register 1 |
| TMRB1_CMP2 | $11 | Compare Register 2 |
| TMRB1_CAP | $12 | Capture Register |
| TMRB1_LOAD | $13 | Load Register |
| TMRB1_HOLD | $14 | Hold Register |
| TMRB1_CNTR | $15 | Counter Register |
| TMRB1_CTRL | $16 | Control Register |
| TMRB1_SCR | $17 | Status and Control Register |
| TMRB1_CMPLD1 | $18 | Comparator Load Register 1 |

## Table 4-19 Interrupt Control Registers Address Map (ITCN_BASE = $00 F1A0)

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| IPR 0 | $0 | Interrupt Priority Register 0 |
| IPR 1 | $1 | Interrupt Priority Register 1 |
| IPR 2 | $2 | Interrupt Priority Register 2 |
| IPR 3 | $3 | Interrupt Priority Register 3 |
| IPR 4 | $4 | Interrupt Priority Register 4 |
| IPR 5 | $5 | Interrupt Priority Register 5 |
| IPR 6 | $6 | Interrupt Priority Register 6 |
| IPR 7 | $7 | Interrupt Priority Register 7 |
| IPR 8 | $8 | Interrupt Priority Register 8 |
| IPR 9 | $9 | Interrupt Priority Register 9 |
| VBA | $A | Vector Base Address Register |
| FIM0 | $B | Fast Interrupt Match Register 0 |
| FIVAL0 | $C | Fast Interrupt Vector Address Low 0 Register |
| FIVAH0 | $D | Fast Interrupt Vector Address High 0 Register |
| FIM1 | $E | Fast Interrupt Match Register 1 |
| FIVAL1 | $F | Fast Interrupt Vector Address Low 1 Register |
| FIVAH1 | $10 | Fast Interrupt Vector Address High 1 Register |
| IRQP 0 | $11 | IRQ Pending Register 0 |
| IRQP 1 | $12 | IRQ Pending Register 1 |
| IRQP 2 | $13 | IRQ Pending Register 2 |
| IRQP 3 | $14 | IRQ Pending Register 3 |
| IRQP 4 | $15 | IRQ Pending Register 4 |
| IRQP 5 | $16 | IRQ Pending Register 5 |
| Reserved | | |
| ICTL | $1D | Interrupt Control Register |
| Reserved | | |
| IPR10 | $1F | Interrupt Priority Register 10 |

## Table 4-33 GPIOE Registers Address Map (GPIOE_BASE = $00 F330)

| Register Acronym | Address Offset | Register Description | Reset Value |
|---|---|---|---|
| GPIOE_PUR | $0 | Pull-up Enable Register | 0 x 3FFF |
| GPIOE_DR | $1 | Data Register | 0 x 0000 |
| GPIOE_DDR | $2 | Data Direction Register | 0 x 0000 |
| GPIOE_PER | $3 | Peripheral Enable Register | 0 x 3FFF |
| GPIOE_IAR | $4 | Interrupt Assert Register | 0 x 0000 |
| GPIOE_IENR | $5 | Interrupt Enable Register | 0 x 0000 |
| GPIOE_IPOLR | $6 | Interrupt Polarity Register | 0 x 0000 |
| GPIOE_IPR | $7 | Interrupt Pending Register | 0 x 0000 |
| GPIOE_IESR | $8 | Interrupt Edge-Sensitive Register | 0 x 0000 |
| GPIOE_PPMODE | $9 | Push-Pull Mode Register | 0 x 3FFF |
| GPIOE_RAWDATA | $A | Raw Data Input Register | — |

## Table 4-34 GPIOF Registers Address Map (GPIOF_BASE = $00 F340)

| Register Acronym | Address Offset | Register Description | Reset Value |
|---|---|---|---|
| GPIOF_PUR | $0 | Pull-up Enable Register | 0 x FFFF |
| GPIOF_DR | $1 | Data Register | 0 x 0000 |
| GPIOF_DDR | $2 | Data Direction Register | 0 x 0000 |
| GPIOF_PER | $3 | Peripheral Enable Register | 0 x FFFF |
| GPIOF_IAR | $4 | Interrupt Assert Register | 0 x 0000 |
| GPIOF_IENR | $5 | Interrupt Enable Register | 0 x 0000 |
| GPIOF_IPOLR | $6 | Interrupt Polarity Register | 0 x 0000 |
| GPIOF_IPR | $7 | Interrupt Pending Register | 0 x 0000 |
| GPIOF_IESR | $8 | Interrupt Edge-Sensitive Register | 0 x 0000 |
| GPIOF_PPMODE | $9 | Push-Pull Mode Register | 0 x FFFF |
| GPIOF_RAWDATA | $A | Raw Data Input Register | — |

## Table 4-39 FlexCAN2 Registers Address Map (Continued) (FC2_BASE = $00 FA00)

***FlexCAN2 is NOT available in the 56F8166 device***

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| | | Reserved |
| FC2MB6_CONTROL | $70 | Message Buffer 6 Control / Status Register |
| FC2MB6_ID_HIGH | $71 | Message Buffer 6 ID High Register |
| FC2MB6_ID_LOW | $72 | Message Buffer 6 ID Low Register |
| FC2MB6_DATA | $73 | Message Buffer 6 Data Register |
| FC2MB6_DATA | $74 | Message Buffer 6 Data Register |
| FC2MB6_DATA | $75 | Message Buffer 6 Data Register |
| FC2MB6_DATA | $76 | Message Buffer 6 Data Register |
| | | Reserved |
| FC2MB7_CONTROL | $78 | Message Buffer 7 Control / Status Register |
| FC2MB7_ID_HIGH | $79 | Message Buffer 7 ID High Register |
| FC2MB7_ID_LOW | $7A | Message Buffer 7 ID Low Register |
| FC2MB7_DATA | $7B | Message Buffer 7 Data Register |
| FC2MB7_DATA | $7C | Message Buffer 7 Data Register |
| FC2MB7_DATA | $7D | Message Buffer 7 Data Register |
| FC2MB7_DATA | $7E | Message Buffer 7 Data Register |
| | | Reserved |
| FC2MB8_CONTROL | $80 | Message Buffer 8 Contro l /Status Register |
| FC2MB8_ID_HIGH | $81 | Message Buffer 8 ID High Register |
| FC2MB8_ID_LOW | $82 | Message Buffer 8 ID Low Register |
| FC2MB8_DATA | $83 | Message Buffer 8 Data Register |
| FC2MB8_DATA | $84 | Message Buffer 8 Data Register |
| FC2MB8_DATA | $85 | Message Buffer 8 Data Register |
| FC2MB8_DATA | $86 | Message Buffer 8 Data Register |
| | | Reserved |
| FC2MB9_CONTROL | $88 | Message Buffer 9 Control / Status Register |
| FC2MB9_ID_HIGH | $89 | Message Buffer 9 ID High Register |
| FC2MB9_ID_LOW | $8A | Message Buffer 9 ID Low Register |
| FC2MB9_DATA | $8B | Message Buffer 9 Data Register |
| FC2MB9_DATA | $8C | Message Buffer 9 Data Register |
| FC2MB9_DATA | $8D | Message Buffer 9 Data Register |

**Table 4-39 FlexCAN2 Registers Address Map (Continued)**
**(FC2_BASE = $00 FA00)**
***FlexCAN2 is NOT available in the 56F8166 device***

| Register Acronym | Address Offset | Register Description |
|---|---|---|
| FC2MB13_DATA | $AC | Message Buffer 13 Data Register |
| FC2MB13_DATA | $AD | Message Buffer 13 Data Register |
| FC2MB13_DATA | $AE | Message Buffer 13 Data Register |
| | | Reserved |
| FC2MB14_CONTROL | $B0 | Message Buffer 14 Control / Status Register |
| FC2MB14_ID_HIGH | $B1 | Message Buffer 14 ID High Register |
| FC2MB14_ID_LOW | $B2 | Message Buffer 14 ID Low Register |
| FC2MB14_DATA | $B3 | Message Buffer 14 Data Register |
| FC2MB14_DATA | $B4 | Message Buffer 14 Data Register |
| FC2MB14_DATA | $B5 | Message Buffer 14 Data Register |
| FC2MB14_DATA | $B6 | Message Buffer 14 Data Register |
| | | Reserved |
| FC2MB15_CONTROL | $B8 | Message Buffer 15 Control / Status Register |
| FC2MB15_ID_HIGH | $B9 | Message Buffer 15 ID High Register |
| FC2MB15_ID_LOW | $BA | Message Buffer 15 ID Low Register |
| FC2MB15_DATA | $BB | Message Buffer 15 Data Register |
| FC2MB15_DATA | $BC | Message Buffer 15 Data Register |
| FC2MB15_DATA | $BD | Message Buffer 15 Data Register |
| FC2MB15_DATA | $BE | Message Buffer 15 Data Register |
| | | Reserved |

## 4.8 Factory Programmed Memory

The Boot Flash memory block is programmed during manufacturing with a default Serial Bootloader program. The Serial Bootloader application can be used to load a user application into the Program and *Data Flash* (*NOT available in the 56F8166 device*) memories of the device. The **56F83xx SCI/CAN Bootloader User Manual (MC56F83xxBLUM)** provides detailed information on this firmware. An application note, **Production Flash Programming (AN1973),** details how the Serial Bootloader program can be used to perform production flash programming of the on board flash memories as well as other potential methods.

Like all the flash memory blocks the Boot Flash can be erased and programmed by the user. The Serial Bootloader application is programmed as an aid to the end user, but is not required to be used or maintained in the Boot Flash memory.

# Part 5 Interrupt Controller (ITCN)

## 5.1 Introduction

The Interrupt Controller (ITCN) module is used to arbitrate between various interrupt requests (IRQs), to signal to the 56800E core when an interrupt of sufficient priority exists, and to what address to jump in order to service this interrupt.

## 5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

For further information, see **Table 4-5**, Interrupt Vector Table Contents.

## 5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers allowing each of the 86 interrupt sources to be set to one of four priority levels, excluding certain interrupts of fixed priority. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, zero is the highest priority, while number 85 is the lowest.

### 5.3.1 Normal Interrupt Handling

Once the ITCN has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the VBA and the vector number to determine the vector address. In this way, an offset is generated into the vector table for each interrupt.

### 5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following tables define the nesting requirements for each priority level.

**Table 5-1 Interrupt Mask Bit Definition**

| SR[9][1] | SR[8][1] | Permitted Exceptions | Masked Exceptions |
|---|---|---|---|
| 0 | 0 | Priorities 0, 1, 2, 3 | None |
| 0 | 1 | Priorities 1, 2, 3 | Priority 0 |
| 1 | 0 | Priorities 2, 3 | Priorities 0, 1 |
| 1 | 1 | Priority 3 | Priorities 0, 1, 2 |

1. Core status register bits indicating current interrupt mask within the core.

#### 5.6.3.1 Flash Memory Command, Data, Address Buffers Empty Interrupt Priority Level (FMCBE IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.3.2 Flash Memory Command Complete Priority Level (FMCC IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.3.3 Flash Memory Error Interrupt Priority Level (FMERR IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.3.4 PLL Loss of Lock Interrupt Priority Level (LOCK IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.7.2 Timer D, Channel 3 Interrupt Priority Level (TMRD3 IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.7.3 Timer D, Channel 2 Interrupt Priority Level (TMRD2 IPL)—Bits 11–10

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.7.4 Timer D, Channel 1 Interrupt Priority Level (TMRD1 IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.7.5 Timer D, Channel 0 Interrupt Priority Level (TMRD0 IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

#### 5.6.7.6 Reserved—Bits 5–4

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

## 6.8 Stop and Wait Mode Disable Function

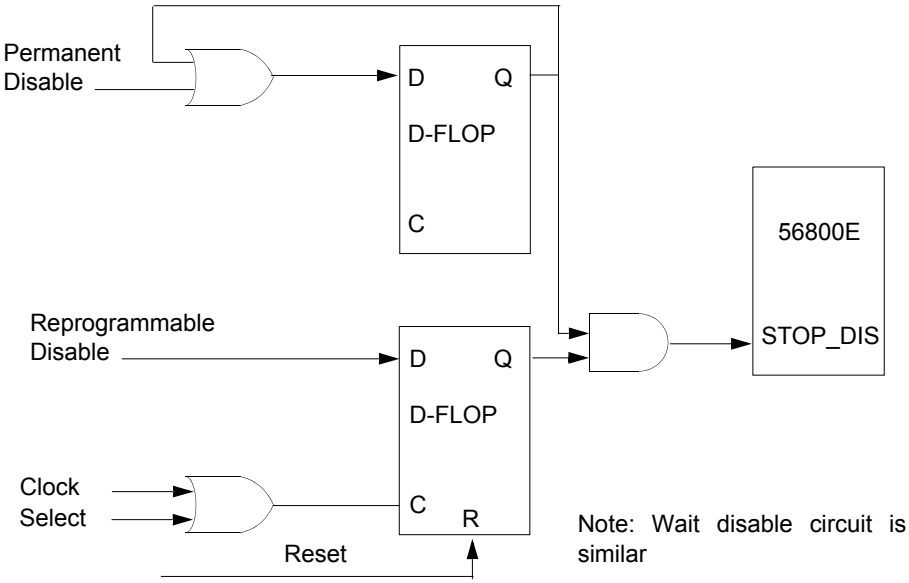


**Figure 6-17 Internal Stop Disable Circuit**

The 56800E core contains both STOP and WAIT instructions. Both put the CPU to sleep. For lowest power consumption in Stop mode, the PLL can be shut down. This must be done explicitly before entering Stop mode, since there is no automatic mechanism for this. When the PLL is shut down, the 56800E system clock must be set equal to the prescaler output.

Some applications require the 56800E STOP and WAIT instructions be disabled. To disable those instructions, write to the SIM control register (SIM_CONTROL) described in **Part 6.5.1**. This procedure can be on either a permanent or temporary basis. Permanently assigned applications last only until their next reset.

## 6.9 Resets

The SIM supports four sources of reset. The two asynchronous sources are the external $\overline{\text{RESET}}$ pin and the Power-On Reset (POR). The two synchronous sources are the software reset, which is generated within the SIM itself by writing to the SIM_CONTROL register, and the COP reset.

Reset begins with the assertion of any of the reset sources. Release of reset to various blocks is sequenced to permit proper operation of the device. A POR reset is first extended for $2^{21}$ clock cycles to permit stabilization of the clock source, followed by a 32 clock window in which SIM clocking is initiated. It is then followed by a 32 clock window in which peripherals are released to implement Flash security, and, finally, followed by a 32 clock window in which the core is initialized. After completion of the described reset sequence, application code will begin execution.

Resets may be asserted asynchronously, but they are always released internally on a rising edge of the system clock.

# Part 7 Security Features

The 56F8366/56F8166 offer security features intended to prevent unauthorized users from reading the contents of the Flash Memory (FM) array. The Flash security consists of several hardware interlocks that block the means by which an unauthorized user could gain access to the Flash array.

However, part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program, as this code would defeat the purpose of security. At the same time, the user may also wish to put a "backdoor" in his program. As an example, the user downloads a security key through the SCI, allowing access to a programming routine that updates parameters stored in another section of the Flash.

## 7.1 Operation with Security Enabled

Once the user has programmed the Flash with his application code, the device can be secured by programming the security bytes located in the FM configuration field, which occupies a portion of the FM array. These non-volatile bytes will keep the part secured through reset and through power-down of the device. Only two bytes within this field are used to enable or disable security. Refer to the Flash Memory section in the **56F8300 Peripheral User Manual** for the state of the security bytes and the resulting state of security. When Flash security mode is enabled in accordance with the method described in the Flash Memory module specification, the device will disable external P-space accesses restricting code execution to internal memory, disable EXTBOOT = 1 mode, and disable the core EOnCE debug capabilities. Normal program execution is otherwise unaffected.

## 7.2 Flash Access Blocking Mechanisms

The 56F8366/56F8166 have several operating functional and test modes. Effective Flash security must address operating mode selection and anticipate modes in which the on-chip Flash can be compromised and read without explicit user permission. Methods to block these are outlined in the next subsections.

### 7.2.1 Forced Operating Mode Selection

At boot time, the SIM determines in which functional modes the device will operate. These are:

- Internal Boot Mode
- External Boot Mode
- Secure Mode

When Flash security is enabled as described in the Flash Memory module specification, the device will boot in internal boot mode, disable all access to external P-space, and start executing code from the Boot Flash at address 0x02_0000.

This security affords protection only to applications in which the device operates in internal Flash security mode. Therefore, the security feature cannot be used unless all executing code resides on-chip.

When security is enabled, any attempt to override the default internal operating mode by asserting the EXTBOOT pin in conjunction with reset will be ignored.

### 7.2.2 Disabling EOnCE Access

On-chip Flash can be read by issuing commands across the EOnCE port, which is the debug interface for the 56800E core. The TRST, TCLK, TMS, TDO, and TDI pins comprise a JTAG interface onto which the EOnCE port functionality is mapped. When the device boots, the chip-level JTAG TAP (Test Access Port) is active and provides the chip's boundary scan capability and access to the ID register.

Proper implementation of Flash security requires that no access to the EOnCE port is provided when security is enabled. The 56800E core has an input which disables reading of internal memory via the JTAG/EOnCE. The FM sets this input at reset to a value determined by the contents of the FM security bytes.

### 7.2.3 Flash Lockout Recovery

If a user inadvertently enables Flash security on the device, a built-in lockout recovery mechanism can be used to reenable access to the device. This mechanism completely reases all on-chip Flash, thus disabling Flash security. Access to this recovery mechanism is built into CodeWarrior via an instruction in memory configuration (*.cfg*) files. Add, or uncomment the following configuration command:

**unlock_flash_on_connect 1**

For more information, please see **CodeWarrior MC56F83xx/DSP5685x Family Targeting Manual**.

The LOCKOUT_RECOVERY instruction has an associated 7-bit Data Register (DR) that is used to control the clock divider circuit within the FM module. This divider, FM_CLKDIV[6:0], is used to control the period of the clock used for timed events in the FM erase algorithm. This register must be set with appropriate values before the lockout sequence can begin. Refer to the JTAG section of the **56F8300 Peripheral User Manual** for more details on setting this register value.

The value of the JTAG FM_CLKDIV[6:0] will replace the value of the FM register FMCLKD that divides down the system clock for timed events, as illustrated in **Figure 7-1**. FM_CLKDIV[6] will map to the PRDIV8 bit, and FM_CLKDIV[5:0] will map to the DIV[5:0] bits. The combination of PRDIV8 and DIV must divide the FM input clock down to a frequency of 150kHz-200kHz. The **"Writing the FMCLKD Register**" section in the Flash Memory chapter of the **56F8300 Peripheral User Manual** gives specific equations for calculating the correct values.

## Table 8-2 56F8166 GPIO Ports Configuration (Continued)

| GPIO Port | Port Width | Available Pins in 56F8166 | Peripheral Function | Reset Function |
|---|---|---|---|---|
| E | 14 | 11 | 2 pins - SCI0<br>2 pins - EMI Address pins<br>4 pins - SPI0<br>1 pin - TMRC<br>1 pin - TMRC - Not available in this package<br>2 pins - Dedicated GPIO<br>2 pins - TMRD - Not available in this package | SCI0<br>EMI Address<br>SPI0<br>TMRC<br>N/A<br>GPIO<br>N/A |
| F | 16 | 16 | 16 pins - EMI Data | EMI Data |

## Table 8-3 GPIO External Signals Map

**Pins in shaded rows are not available in 56F8366/56F8166**

***Pins in italics are NOT available in the 56F8166 device***

| GPIO Port | GPIO Bit | Reset Function | Functional Signal | Package PIn |
|---|---|---|---|---|
| GPIOA | 0 | Peripheral | A8 | 19 |
| | 1 | Peripheral | A9 | 20 |
| | 2 | Peripheral | A10 | 21 |
| | 3 | Peripheral | A11 | 22 |
| | 4 | Peripheral | A12 | 23 |
| | 5 | Peripheral | A13 | 24 |
| | 6 | Peripheral | A14 | 25 |
| | 7 | Peripheral | A15 | 26 |
| | 8 | Peripheral | A0 | 138 |
| | 9 | Peripheral | A1 | 10 |
| | 10 | Peripheral | A2 | 11 |
| | 11 | Peripheral | A3 | 12 |
| | 12 | Peripheral | A4 | 13 |
| | 13 | Peripheral | A5 | 14 |

## Table 10-7 Current Consumption per Power Supply Pin (Typical)
### On-Chip Regulator Enabled (OCR_DIS = Low)

| Mode | $I_{DD\_IO}$[1] | $I_{DD\_ADC}$ | $I_{DD\_OSC\_PLL}$ | Test Conditions |
|---|---|---|---|---|
| Stop1 | 6mA | 0μA | 165μA | • 8MHz Device Clock<br>• All peripheral clocks are off<br>• ADC powered off<br>• PLL powered off |
| Stop2 | 5.1mA | 0μA | 155μA | • External Clock is off<br>• All peripheral clocks are off<br>• ADC powered off<br>• PLL powered off |

1. No Output Switching
2. Includes Processor Core current supplied by internal voltage regulator

## Table 10-8 Current Consumption per Power Supply Pin (Typical)
### On-Chip Regulator Disabled (OCR_DIS = High)

| Mode | $I_{DD\_Core}$ | $I_{DD\_IO}$[1] | $I_{DD\_ADC}$ | $I_{DD\_OSC\_PLL}$ | Test Conditions |
|---|---|---|---|---|---|
| RUN1_MAC | 150mA | 13μA | 50mA | 2.5mA | • 60MHz Device Clock<br>• All peripheral clocks are enabled<br>• All peripherals running<br>• Continuous MAC instructions with fetches from Data RAM<br>• ADC powered on and clocked |
| Wait3 | 86mA | 13μA | 70μA | 2.5mA | • 60MHz Device Clock<br>• All peripheral clocks are enabled<br>• ADC powered off |
| Stop1 | 950μA | 13μA | 0μA | 165μA | • 8MHz Device Clock<br>• All peripheral clocks are off<br>• ADC powered off<br>• PLL powered off |
| Stop2 | 100μA | 13μA | 0μA | 155μA | • External Clock is off<br>• All peripheral clocks are off<br>• ADC powered off<br>• PLL powered off |

1. No Output Switching

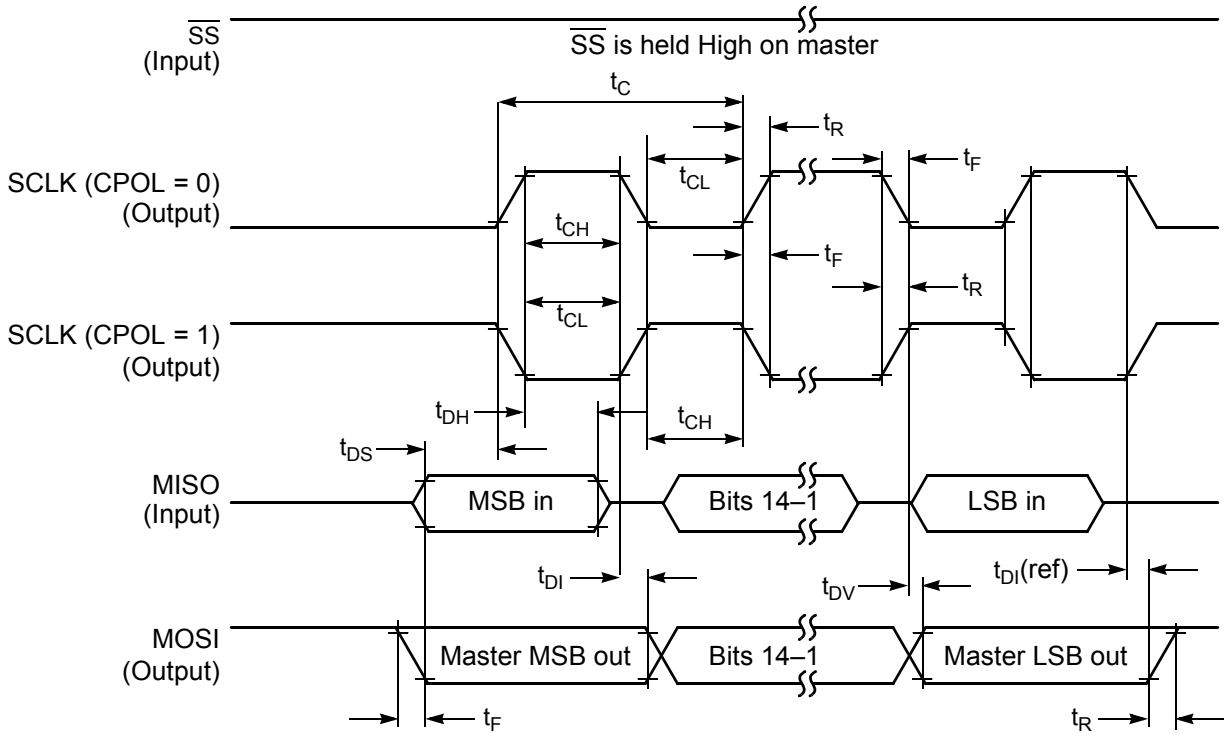


**Figure 10-11 SPI Master Timing (CPHA = 0)**

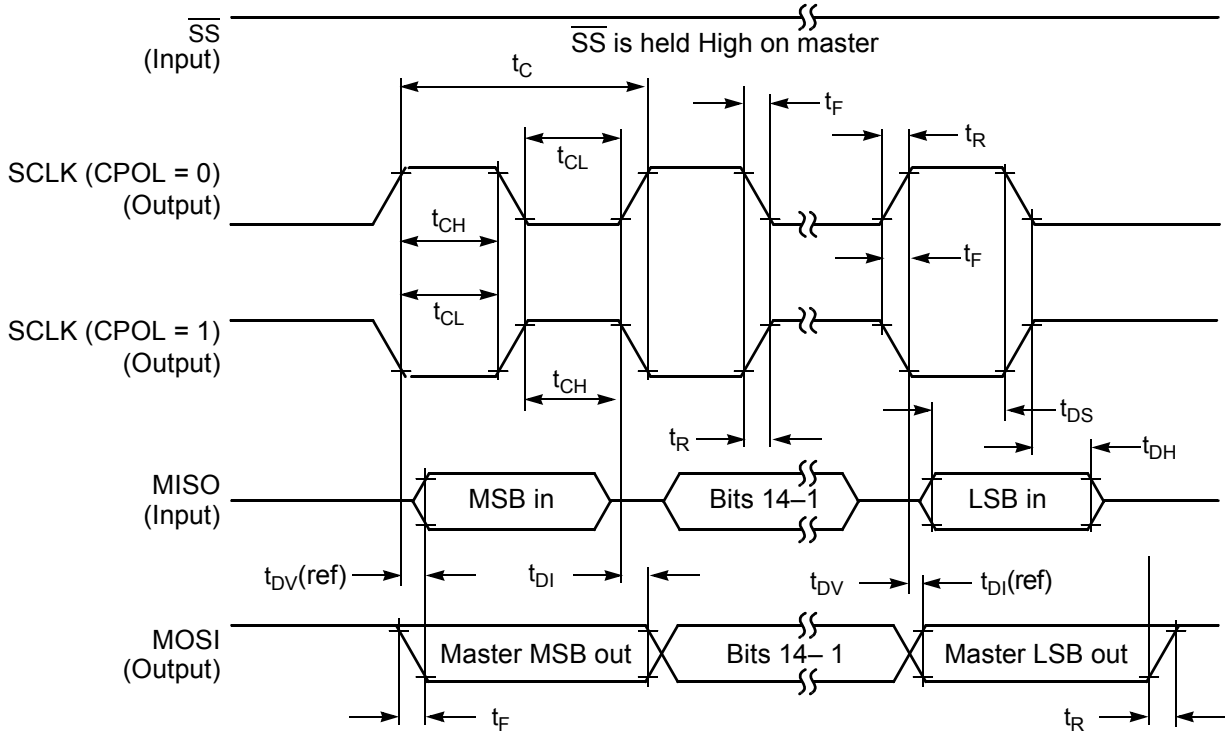


**Figure 10-12 SPI Master Timing (CPHA = 1)**