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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	62
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc56f8366mfve

bulk erased or erased in pages. Program Flash page erase size is 1KB. Boot Flash page erase size is 512 bytes and the Boot Flash memory can also be either bulk or page erased.

A key application-specific feature of the 56F8166 is the inclusion of one Pulse Width Modulator (PWM) module. This module incorporates three complementary, individually programmable PWM signal output pairs and can also support six independent PWM functions to enhance motor control functionality. Complementary operation permits programmable dead time insertion, distortion correction via current sensing by software, and separate top and bottom output polarity control. The up-counter value is programmable to support a continuously variable PWM frequency. Edge-aligned and center-aligned synchronous pulse width control (0% to 100% modulation) is supported. The device is capable of controlling most motor types: ACIM (AC Induction Motors); both BDC and BLDC (Brush and Brushless DC motors); SRM and VRM (Switched and Variable Reluctance Motors); and stepper motors. The PWM incorporates fault protection and cycle-by-cycle current limiting with sufficient output drive capability to directly drive standard optoisolators. A “smoke-inhibit”, write-once protection feature for key parameters is also included. A patented PWM waveform distortion correction circuit is also provided. Each PWM is double-buffered and includes interrupt controls to permit integral reload rates to be programmable from 1 to 16. The PWM module provides reference outputs to synchronize the Analog-to-Digital Converters through two channels of Quad Timer C.

The 56F8166 incorporates a Quadrature Decoder capable of capturing all four transitions on the two-phase inputs, permitting generation of a number proportional to actual position. Speed computation capabilities accommodate both fast- and slow-moving shafts. An integrated watchdog timer in the Quadrature Decoder can be programmed with a time-out value to alert when no shaft motion is detected. Each input is filtered to ensure only true transitions are recorded.

This controller also provides a full set of standard programmable peripherals that include two Serial Communications Interfaces (SCIs); two Serial Peripheral Interfaces (SPIs); and two Quad Timers. Any of these interfaces can be used as General Purpose Input/Outputs (GPIOs) if that function is not required. An internal interrupt controller is also a part of the 56F8166.

1.3 Award-Winning Development Environment

Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.

The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

1.4 Architecture Block Diagram

Note: *Features in italics are NOT available in the 56F8166 device and are shaded in the following figures.*

The 56F8366/56F8166 architecture is shown in **Figure 1-1** and **Figure 1-2**. **Figure 1-1** illustrates how the 56800E system buses communicate with internal memories, the external memory interface and the IPBus Bridge. **Table 1-2** lists the internal buses in the 56800E architecture and provides a brief description of their function. **Figure 1-2** shows the peripherals and control blocks connected to the IPBus Bridge. The figures do not show the on-board regulator and power and ground signals. They also do not show the multiplexing between peripherals or the dedicated GPIOs. Please see **Part 2, Signal/Connection Descriptions,** to see which signals are multiplexed with those of other peripherals.

Also shown in **Figure 1-2** are connections between the PWM, Timer C and ADC blocks. These connections allow the PWM and/or Timer C to control the timing of the start of ADC conversions. The Timer C channel indicated can generate periodic start (SYNC) signals to the ADC to start its conversions. In another operating mode, the PWM load interrupt (SYNC output) signal is routed internally to the Timer C input channel as indicated. The timer can then be used to introduce a controllable delay before generating its output signal. The timer output then triggers the ADC. To fully understand this interaction, please see the **56F8300 Peripheral User Manual** for clarification on the operation of all three of these peripherals.

Table 2-2 Signal and Package Information for the 144-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
D7 **(GPIOF0)**	28	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D14 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D14 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These eight GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Data Bus functionality. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register.
D8 (GPIOF1)	29			
D9 (GPIOF2)	30			
D10 (GPIOF3)	32			
D11 (GPIOF4)	133			
D12 (GPIOF5)	134			
D13 (GPIOF6)	135			
D14 (GPIOF7)	136			
D15 **(GPIOF8)**	137	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D15 specifies part of the data for external program or data memory accesses. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — This GPIO pin can be individually programmed as an input or output pin. At reset, this pin defaults to the data bus function. To deactivate the internal pull-up resistor, set bit 8 in the GPIOF_PUR register.

Table 2-2 Signal and Package Information for the 144-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
TXD1 **(GPIOD6)**	42	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Transmit Data** — SCI1 transmit data output **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI output. To deactivate the internal pull-up resistor, clear bit 6 in the GPIOD_PUR register.
RXD1 **(GPIOD7)**	43	Input Input/ Output	Input, pull-up enabled	**Receive Data** — SCI1 receive data input **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is SCI input. To deactivate the internal pull-up resistor, clear bit 7 in the GPIOD_PUR register.
TCK	121	Schmitt Input	Input, pulled low internally	**Test Clock Input** — This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/EOnCE port. The pin is connected internally to a pull-down resistor.
TMS	122	Schmitt Input	Input, pulled high internally	**Test Mode Select Input** — This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
TDI	123	Schmitt Input	Input, pulled high internally	**Test Data Input** — This input pin provides a serial input data stream to the JTAG/EOnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. To deactivate the internal pull-up resistor, set the JTAG bit in the SIM_PUDR register.
TDO	124	Output	In reset, output is disabled, pull-up is enabled	**Test Data Output** — This tri-stateable output pin provides a serial output data stream from the JTAG/EOnCE port. It is driven in the shift-IR and shift-DR controller states, and changes on the falling edge of TCK.

Table 2-2 Signal and Package Information for the 144-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
INDEX1	8	Schmitt Input	Input, pull-up enabled	**Index1** — Quadrature Decoder 1, INDEX input
(TB2)		Schmitt Input/ Output		**TB2** — Timer B, Channel 2
(MISO1)		Schmitt Input/ Output		**SPI 1 Master In/Slave Out** — This serial data pin is an input to a master device and an output from a slave device. The MISO line of a slave device is placed in the high-impedance state if the slave device is not selected. The slave device places data on the MISO line a half-cycle before the clock edge the master device uses to latch the data. To activate the SPI function, set the INDEX_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC2)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as an input or output pin. After reset, the default state is INDEX1. To deactivate the internal pull-up resistor, clear bit 2 in the GPIOC_PUR register.
HOME1	9	Schmitt Input	Input, pull-up enabled	**Home** — Quadrature Decoder 1, HOME input
(TB3)		Schmitt Input/ Output		**TB3** — Timer B, Channel 3
($\overline{\text{SS1}}$)		Schmitt Input		**SPI 1 Slave Select** — In the master mode, this pin is used to arbitrate multiple masters. In slave mode, this pin is used to select the slave. To activate the SPI function, set the HOME_ALT bit in the SIM_GPS register. For details, see **Part 6.5.8**.
(GPIOC3)		Schmitt Input/ Output		**Port C GPIO** — This GPIO pin can be individually programmed as input or an output pin. In the 56F8366, the default state after reset is HOME1. In the 56F8166, the default state is not one of the functions offered and must be reconfigured. To deactivate the internal pull-up resistor, clear bit 3 in the GPIOC_PUR register.

The crystal and associated components should be mounted as near as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

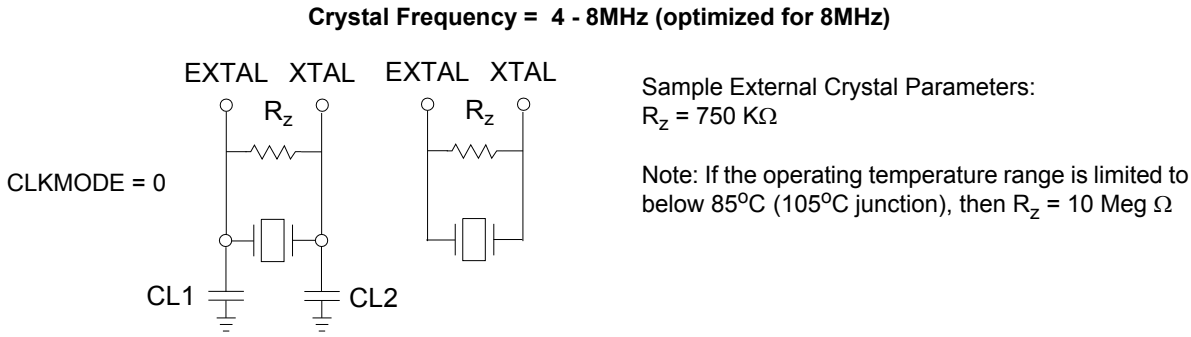

Figure 3-2 Connecting to a Crystal Oscillator

Note: The OCCS_COHL bit must be set to 1 when a crystal oscillator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

3.2.2 Ceramic Resonator (Default)

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. A typical ceramic resonator circuit is shown in **Figure 3-3**. Refer to the supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as near as possible to the EXTAL and XTAL pins.

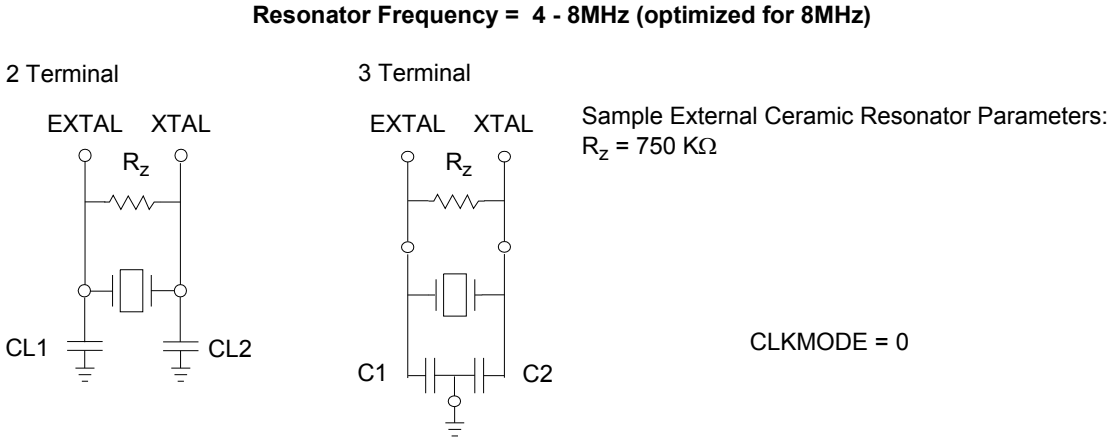

Figure 3-3 Connecting a Ceramic Resonator

Note: The OCCS_COHL bit must be set to 0 when a ceramic resonator is used. The reset condition on the OCCS_COHL bit is 0. Please see the COHL bit in the Oscillator Control (OSCTL) register, discussed in the **56F8300 Peripheral User Manual**.

Note: *Program RAM is NOT available on the 56F8166 device.*

Table 4-4 Program Memory Map at Reset

<table>
<tr><th rowspan="3">Begin/End Address</th><th>Mode 0 (MA = 0)</th><th colspan="2">Mode 1[1] (MA = 1)</th></tr>
<tr><th>Internal Boot</th><th colspan="2">External Boot</th></tr>
<tr><th>Internal Boot
16-Bit External Address Bus</th><th>EMI_MODE = 0[2,3]
16-Bit External Address Bus</th><th>EMI_MODE = 1[4]
20-Bit External Address Bus</th></tr>
<tr><td>P:$1F FFFF
P:$10 0000</td><td rowspan="2">External Program Memory[5]</td><td rowspan="2">External Program Memory[5]</td><td>External Program Memory[6]</td></tr>
<tr><td>P:$0F FFFF
P:$05 0000</td><td rowspan="8">External Program Memory
COP Reset Address = 04 0002[7]
Boot Location = 04 0000[7]</td></tr>
<tr><td>P:$04 FFFF
P:$04 F800</td><td colspan="2">On-Chip Program RAM
4KB</td></tr>
<tr><td>P:$04 F7FF
P:$04 4000</td><td colspan="2">Reserved
92KB</td></tr>
<tr><td>P:$04 3FFF
P:$04 0000</td><td>Boot Flash
32KB
COP Reset Address = 04 0002
Boot Location = 04 0000</td><td>Boot Flash
32KB
(Not Used for Boot in this Mode)</td></tr>
<tr><td>P:$03 FFFF
P:$02 0000</td><td>Internal Program Flash[8]
256KB</td><td>Internal Program Flash
256KB</td></tr>
<tr><td>P:$01 FFFF
P:$01 0000</td><td rowspan="2">Internal Program Flash[8]
256KB</td><td>Internal Program Flash
128KB</td></tr>
<tr><td>P:$00 FFFF
P:$00 0000</td><td>External Program Memory
COP Reset Address = 00 0002
Boot Location = 00 0000</td></tr>
</table>

1. If Flash Security Mode is enabled, EXTBOOT Mode 1 cannot be used. See **Security Features, Part 7**.
2. This mode provides maximum compatibility with 56F80x parts while operating externally.
3. “EMI_MODE =0” when EMI_MODE pin is tied to ground at boot up.
4. “EMI_MODE =1” when EMI_MODE pin is tied to V_{DD} at boot up.
5. Not accessible in reset configuration, since the address is above P:$00 FFFF. The higher bit address/GPIO (and/or chip selects) pins must be reconfigured before this external memory is accessible.
6. Not accessible in reset configuration, since the address is above P:$0F FFFF. The higher bit address/GPIO (and/or chip selects) pins must be reconfigured before this external memory is accessible.
7. Booting from this external address allows prototyping of the internal Boot Flash.
8. Two independent program flash blocks allow one to be programmed/erased while executing from another. Each block must have its own mass erase.

Table 4-5 Interrupt Vector Table Contents[1] (Continued)

Peripheral	Vector Number	Priority Level	Vector Base Address +	Interrupt Function
TMRC	56	0-2	P:$70	Timer C, Channel 0
TMRC	57	0-2	P:$72	Timer C, Channel 1
TMRC	58	0-2	P:$74	Timer C, Channel 2
TMRC	59	0-2	P:$76	Timer C, Channel 3
TMRB	60	0-2	P:$78	Timer B, Channel 0
TMRB	61	0-2	P:$7A	Timer B, Channel 1
TMRB	62	0-2	P:$7C	Timer B, Channel 2
TMRB	63	0-2	P:$7E	Timer B, Channel 3
TMRA	64	0-2	P:$80	Timer A, Channel 0
TMRA	65	0-2	P:$82	Timer A, Channel 1
TMRA	66	0-2	P:$84	Timer A, Channel 2
TMRA	67	0-2	P:$86	Timer A, Channel 3
SCI0	68	0-2	P:$88	SCI 0 Transmitter Empty
SCI0	69	0-2	P:$8A	SCI 0 Transmitter Idle
				Reserved
SCI0	71	0-2	P:$8E	SCI 0 Receiver Error
SCI0	72	0-2	P:$90	SCI 0 Receiver Full
ADCB	73	0-2	P:$92	ADC B Conversion Compete / End of Scan
ADCA	74	0-2	P:$94	ADC A Conversion Complete / End of Scan
ADCB	75	0-2	P:$96	ADC B Zero Crossing or Limit Error
ADCA	76	0-2	P:$98	ADC A Zero Crossing or Limit Error
PWMB	77	0-2	P:$9A	Reload PWM B
PWMA	78	0-2	P:$9C	Reload PWM A
PWMB	79	0-2	P:$9E	PWM B Fault
PWMA	80	0-2	P:$A0	PWM A Fault
core	81	- 1	P:$A2	SW Interrupt LP
FLEXCAN2	82	0-2	P:$A4	FlexCAN Bus Off
FLEXCAN2	83	0-2	P:$A6	FlexCAN Error
FLEXCAN2	84	0-2	P:$A8	FlexCAN Wake Up
FLEXCAN2	85	0-2	P:$AA	FlexCAN Message Buffer Interrupt

1. Two words are allocated for each entry in the vector table. This does not allow the full address range to be referenced from the vector table, providing only 19 bits of address.

2. If the VBA is set to $0200 (or VBA = 0000 for Mode 1, EMI_MODE = 0), the first two locations of the vector table are the chip reset addresses; therefore, these locations are not interrupt vectors.

Table 4-13 Quad Timer C Registers Address Map (Continued)
(TMRC_BASE = $00 F0C0)

Register Acronym	Address Offset	Register Description
TMRC2_SCR	$27	Status and Control Register
TMRC2_CMPLD1	$28	Comparator Load Register 1
TMRC2_CMPLD2	$29	Comparator Load Register 2
TMRC2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRC3_CMP1	$30	Compare Register 1
TMRC3_CMP2	$31	Compare Register 2
TMRC3_CAP	$32	Capture Register
TMRC3_LOAD	$33	Load Register
TMRC3_HOLD	$34	Hold Register
TMRC3_CNTR	$35	Counter Register
TMRC3_CTRL	$36	Control Register
TMRC3_SCR	$37	Status and Control Register
TMRC3_CMPLD1	$38	Comparator Load Register 1
TMRC3_CMPLD2	$39	Comparator Load Register 2
TMRC3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map
(TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
TMRD0_CMP1	$0	Compare Register 1
TMRD0_CMP2	$1	Compare Register 2
TMRD0_CAP	$2	Capture Register
TMRD0_LOAD	$3	Load Register
TMRD0_HOLD	$4	Hold Register
TMRD0_CNTR	$5	Counter Register
TMRD0_CTRL	$6	Control Register
TMRD0_SCR	$7	Status and Control Register
TMRD0_CMPLD1	$8	Comparator Load Register 1
TMRD0_CMPLD2	$9	Comparator Load Register 2
TMRD0_COMSCR	$A	Comparator Status and Control Register

Table 4-21 Analog-to-Digital Converter Registers Address Map (ADCB_BASE = $00 F240) (Continued)

Register Acronym	Address Offset	Register Description
ADCB_RSLT 7	$10	Result Register 7
ADCB_LLMT 0	$11	Low Limit Register 0
ADCB_LLMT 1	$12	Low Limit Register 1
ADCB_LLMT 2	$13	Low Limit Register 2
ADCB_LLMT 3	$14	Low Limit Register 3
ADCB_LLMT 4	$15	Low Limit Register 4
ADCB_LLMT 5	$16	Low Limit Register 5
ADCB_LLMT 6	$17	Low Limit Register 6
ADCB_LLMT 7	$18	Low Limit Register 7
ADCB_HLMT 0	$19	High Limit Register 0
ADCB_HLMT 1	$1A	High Limit Register 1
ADCB_HLMT 2	$1B	High Limit Register 2
ADCB_HLMT 3	$1C	High Limit Register 3
ADCB_HLMT 4	$1D	High Limit Register 4
ADCB_HLMT 5	$1E	High Limit Register 5
ADCB_HLMT 6	$1F	High Limit Register 6
ADCB_HLMT 7	$20	High Limit Register 7
ADCB_OFS 0	$21	Offset Register 0
ADCB_OFS 1	$22	Offset Register 1
ADCB_OFS 2	$23	Offset Register 2
ADCB_OFS 3	$24	Offset Register 3
ADCB_OFS 4	$25	Offset Register 4
ADCB_OFS 5	$26	Offset Register 5
ADCB_OFS 6	$27	Offset Register 6
ADCB_OFS 7	$28	Offset Register 7
ADCB_POWER	$29	Power Control Register
ADCB_CAL	$2A	ADC Calibration Register

Table 4-35 System Integration Module Registers Address Map (SIM_BASE = $00 F350)

Register Acronym	Address Offset	Register Description
SIM_CONTROL	$0	Control Register
SIM_RSTSTS	$1	Reset Status Register
SIM_SCR0	$2	Software Control Register 0
SIM_SCR1	$3	Software Control Register 1
SIM_SCR2	$4	Software Control Register 2
SIM_SCR3	$5	Software Control Register 3
SIM_MSH_ID	$6	Most Significant Half JTAG ID
SIM_LSH_ID	$7	Least Significant Half JTAG ID
SIM_PUDR	$8	Pull-up Disable Register
		Reserved
SIM_CLKOSR	$A	Clock Out Select Register
SIM_GPS	$B	Quad Decoder 1 / Timer B / SPI 1 Select Register
SIM_PCE	$C	Peripheral Clock Enable Register
SIM_ISALH	$D	I/O Short Address Location High Register
SIM_ISALL	$E	I/O Short Address Location Low Register
SIM_PCE2	$F	Peripheral Clock Enable Register 2

Table 4-36 Power Supervisor Registers Address Map (LVI_BASE = $00 F360)

Register Acronym	Address Offset	Register Description
LVI_CONTROL	$0	Control Register
LVI_STATUS	$1	Status Register

Table 4-39 FlexCAN2 Registers Address Map (Continued)
(FC2_BASE = $00 FA00)
FlexCAN2 is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
FC2MB9_DATA	$8E	Message Buffer 9 Data Register
		Reserved
FC2MB10_CONTROL	$90	Message Buffer 10 Control / Status Register
FC2MB10_ID_HIGH	$91	Message Buffer 10 ID High Register
FC2MB10_ID_LOW	$92	Message Buffer 10 ID Low Register
FC2MB10_DATA	$93	Message Buffer 10 Data Register
FC2MB10_DATA	$94	Message Buffer 10 Data Register
FC2MB10_DATA	$95	Message Buffer 10 Data Register
FC2MB10_DATA	$96	Message Buffer 10 Data Register
		Reserved
FC2MB11_CONTROL	$98	Message Buffer 11 Control / Status Register
FC2MB11_ID_HIGH	$99	Message Buffer 11 ID High Register
FC2MB11_ID_LOW	$9A	Message Buffer 11 ID Low Register
FC2MB11_DATA	$9B	Message Buffer 11 Data Register
FC2MB11_DATA	$9C	Message Buffer 11 Data Register
FC2MB11_DATA	$9D	Message Buffer 11 Data Register
FC2MB11_DATA	$9E	Message Buffer 11 Data Register
		Reserved
FC2MB12_CONTROL	$A0	Message Buffer 12 Control / Status Register
FC2MB12_ID_HIGH	$A1	Message Buffer 12 ID High Register
FC2MB12_ID_LOW	$A2	Message Buffer 12 ID Low Register
FC2MB12_DATA	$A3	Message Buffer 12 Data Register
FC2MB12_DATA	$A4	Message Buffer 12 Data Register
FC2MB12_DATA	$A5	Message Buffer 12 Data Register
FC2MB12_DATA	$A6	Message Buffer 12 Data Register
		Reserved
FC2MB13_CONTROL	$A8	Message Buffer 13 Control / Status Register
FC2MB13_ID_HIGH	$A9	Message Buffer 13 ID High Register
FC2MB13_ID_LOW	$AA	Message Buffer 13 ID Low Register
FC2MB13_DATA	$AB	Message Buffer 13 Data Register

5.6.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.2.2 EOnCE Receive Register Full Interrupt Priority Level (RX_REG IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.3 EOnCE Transmit Register Empty Interrupt Priority Level (TX_REG IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.2.4 EOnCE Trace Buffer Interrupt Priority Level (TRBUF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 1 through 3. It is disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 1
- 10 = IRQ is priority level 2
- 11 = IRQ is priority level 3

5.6.3 Interrupt Priority Register 2 (IPR2)

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-5 Interrupt Priority Register 2 (IPR2)

5.6.22 IRQ Pending 4 Register (IRQP4)

Base + $15	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [80:65]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-24 IRQ Pending 4 Register (IRQP4)

5.6.22.1 IRQ Pending (PENDING)—Bits 80–65

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.23 IRQ Pending 5 Register (IRQP5)

Base + $16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	1	1	1	1	1	1	1	1	1	1	PENDING[81:85]			
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-25 IRQ Pending Register 5 (IRQP5)

5.6.23.1 Reserved—Bits 96–86

This bit field is reserved or not implemented. The bits are read as 1 and cannot be modified by writing.

5.6.23.2 IRQ Pending (PENDING)—Bits 81–85

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 85.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.24 Reserved—Base + 17

5.6.25 Reserved—Base + 18

5.6.26 Reserved—Base + 19

5.6.27 Reserved—Base + 1A

5.6.32.2 FlexCAN2 Message Buffer Interrupt Priority Level (FlexCAN2_MSGBUF IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.3 FlexCAN2 Wake Up Interrupt Priority Level (FlexCAN2_WKUP IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.4 FlexCAN2 Error Interrupt Priority Level (FlexCAN2_ERR IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.5 FlexCAN2 Bus-Off Interrupt Priority Level (FlexCAN2_BOFF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

6.5.3.1 Software Control Data 1 (FIELD)—Bits 15–0

This register is reset only by the Power-On Reset (POR). It has no part-specific functionality and is intended for use by a software developer to contain data that will be unaffected by the other reset sources (RESET pin, software reset, and COP reset).

6.5.4 Most Significant Half of JTAG ID (SIM_MSH_ID)

This read-only register displays the most significant half of the JTAG ID for the chip. This register reads $01D6.

Base + $6	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0
Write																
RESET	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0

Figure 6-6 Most Significant Half of JTAG ID (SIM_MSH_ID)

6.5.5 Least Significant Half of JTAG ID (SIM_LSH_ID)

This read-only register displays the least significant half of the JTAG ID for the chip. This register reads $D01D.

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1
Write																
RESET	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1

Figure 6-7 Least Significant Half of JTAG ID (SIM_LSH_ID)

6.5.6 SIM Pull-up Disable Register (SIM_PUDR)

Most of the pins on the chip have on-chip pull-up resistors. Pins which can operate as GPIO can have these resistors disabled via the GPIO function. Non-GPIO pins can have their pull-ups disabled by setting the appropriate bit in this register. Disabling pull-ups is done on a peripheral-by-peripheral basis (for pins not muxed with GPIO). Each bit in the register (see **Figure 6-8**) corresponds to a functional group of pins. See **Table 2-2** to identify which pins can deactivate the internal pull-up resistor.

Base + $8	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	PWMA1	CAN	EMI_ MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA0	0	CTRL	0	JTAG	0	0	0
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-8 SIM Pull-up Disable Register (SIM_PUDR)

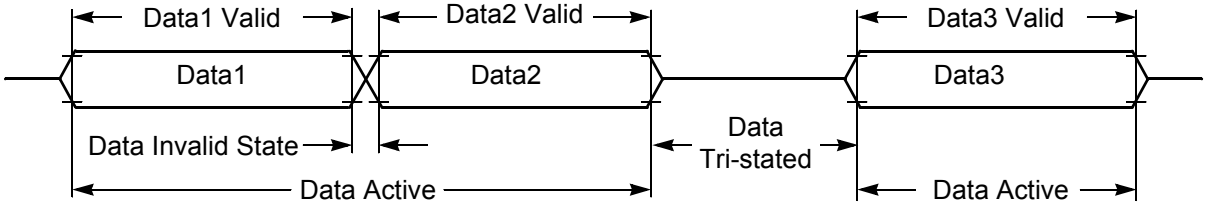

Figure 10-3 Signal States

10.4 Flash Memory Characteristics

Table 10-12 Flash Timing Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Program time[1]	Tprog	20	—	—	μs
Erase time[2]	Terase	20	—	—	ms
Mass erase time	Tme	100	—	—	ms

1. There is additional overhead which is part of the programming sequence. See the **56F8300 Peripheral User Manual** for details. Program time is per 16-bit word in Flash memory. Two words at a time can be programmed within the Program Flash module, as it contains two interleaved memories.
2. Specifies page erase time. There are 512 bytes per page in the Data and Boot Flash memories. The Program Flash module uses two interleaved Flash memories, increasing the effective page size to 1024 bytes.

10.5 External Clock Operation Timing

Table 10-13 External Clock Operation Timing Requirements[1]

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[2]	f_{osc}	0	—	120	MHz
Clock Pulse Width[3]	t_{PW}	3.0	—	—	ns
External clock input rise time[4]	t_{rise}	—	—	10	ns
External clock input fall time[5]	t_{fall}	—	—	10	ns

1. Parameters listed are guaranteed by design.
2. See **Figure 10-4** for details on using the recommended connection of an external clock driver.
3. The high or low pulse width must be no smaller than 8.0ns or the chip will not function.
4. External clock input rise time is measured from 10% to 90%.
5. External clock input fall time is measured from 90% to 10%.

Figure 10-22 TRST Timing Diagram

10.16 Analog-to-Digital Converter (ADC) Parameters

Table 10-24 ADC Parameters

Characteristic	Symbol	Min	Typ	Max	Unit
Input voltages	V_{ADIN}	V_{REFL}	—	V_{REFH}	V
Resolution	R_{ES}	12	—	12	Bits
Integral Non-Linearity[1]	INL	—	+/- 2.4	+/- 3.2	LSB[2]
Differential Non-Linearity	DNL	—	+/- 0.7	< +1	LSB[2]
Monotonicity	GUARANTEED				
ADC internal clock	f_{ADIC}	0.5	—	5	MHz
Conversion range	R_{AD}	V_{REFL}	—	V_{REFH}	V
ADC channel power-up time	t_{ADPU}	5	6	16	t_{AIC} cycles[3]
ADC reference circuit power-up time[4]	t_{VREF}	—	—	25	ms
Conversion time	t_{ADC}	—	6	—	t_{AIC} cycles[3]
Sample time	t_{ADS}	—	1	—	t_{AIC} cycles[3]
Input capacitance	C_{ADI}	—	5	—	pF
Input injection current[5], per pin	I_{ADI}	—	—	3	mA
Input injection current, total	I_{ADIT}	—	—	20	mA
V_{REFH} current	I_{VREFH}	—	1.2	3	mA
ADC A current	I_{ADCA}	—	25	—	mA
ADC B current	I_{ADCB}	—	25	—	mA
Quiescent current	I_{ADCQ}	—	0	10	µA
Uncalibrated Gain Error (ideal = 1)	E_{GAIN}	—	+/- .004	+/- .01	—
Uncalibrated Offset Voltage	V_{OFFSET}	—	+/- 27	+/- 40	mV
Calibrated Absolute Error[6]	AE_{CAL}	—	See **Figure 10-23**	—	LSBs

Table 11-1 56F8366 144-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
13	A4	49	GPIOD1	85	$\overline{\text{RSTO}}$	121	TCK
14	A5	50	ISB0	86	$\overline{\text{RESET}}$	122	TMS
15	$V_{CAP}4$	51	$V_{CAP}1$	87	CLKMODE	123	TDI
16	V_{DD_IO}	52	ISB1	88	ANA0	124	TDO
17	A6	53	ISB2	89	ANA1	125	$V_{PP}1$
18	A7	54	$\overline{\text{IRQA}}$	90	ANA2	126	CAN_TX
19	A8	55	$\overline{\text{IRQB}}$	91	ANA3	127	CAN_RX
20	A9	56	FAULTB0	92	ANA4	128	$V_{CAP}2$
21	A10	57	FAULTB1	93	ANA5	129	$\overline{\text{SS0}}$
22	A11	58	FAULTB2	94	ANA6	130	SCLK0
23	A12	59	D0	95	ANA7	131	MISO0
24	A13	60	D1	96	TEMP_SENSE	132	MOSI0
25	A14	61	FAULTB3	97	V_{REFLO}	133	D11
26	A15	62	PWMA0	98	V_{REFN}	134	D12
27	V_{SS}	63	V_{SS}	99	V_{REFMID}	135	D13
28	D7	64	PWMA1	100	V_{REFP}	136	D14
29	D8	65	PWMA2	101	V_{REFH}	137	D15
30	D9	66	V_{DD_IO}	102	V_{DDA_ADC}	138	A0
31	V_{DD_IO}	67	PWMA3	103	V_{SSA_ADC}	139	PHASEA0
32	D10	68	PWMA4	104	ANB0	140	PHASEB0
33	GPIOB0	69	V_{SS}	105	ANB1	141	INDEX0
34	PWMB0	70	PWMA5	106	ANB2	142	HOME0
35	PWMB1	71	FAULTA0	107	ANB3	143	EMI_MODE
36	PWMB2	72	D2	108	ANB4	144	V_{SS}

Table 11-2 56F8166 144-Pin LQFP Package Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	V_{DD_IO}	37	V_{SS}	73	NC	109	ANB5
2	$V_{PP}2$	38	V_{DD_IO}	74	NC	110	ANB6
3	CLKO	39	PWMB3	75	D3	111	ANB7
4	TXD0	40	PWMB4	76	D4	112	EXTBOOT
5	RXD0	41	PWMB5	77	D5	113	GPIOC8
6	SCLK1	42	TXD1	78	D6	114	GPIOC9
7	MOSI1	43	RXD1	79	OCR_DIS	115	GPIOC10
8	MISO1	44	$\overline{WR}$	80	$V_{DDA\_OSC\_PLL}$	116	GPIOE10
9	$\overline{SS1}$	45	$\overline{RD}$	81	XTAL	117	GPIOE11
10	A1	46	$\overline{PS}$	82	EXTAL	118	TC0
11	A2	47	$\overline{DS}$	83	$V_{CAP}3$	119	V_{DD_IO}
12	A3	48	GPIOD0	84	V_{DD_IO}	120	$\overline{TRST}$
13	A4	49	GPIOD1	85	$\overline{RSTO}$	121	TCK
14	A5	50	ISB0	86	$\overline{RESET}$	122	TMS
15	$V_{CAP}4$	51	$V_{CAP}1$	87	CLKMODE	123	TDI
16	V_{DD_IO}	52	ISB1	88	ANA0	124	TDO
17	A6	53	ISB2	89	ANA1	125	$V_{PP}1$
18	A7	54	$\overline{IRQA}$	90	ANA2	126	NC
19	A8	55	$\overline{IRQB}$	91	ANA3	127	NC
20	A9	56	FAULTB0	92	ANA4	128	$V_{CAP}2$
21	A10	57	FAULTB1	93	ANA5	129	$\overline{SS0}$
22	A11	58	FAULTB2	94	ANA6	130	SCLK0
23	A12	59	D0	95	ANA7	131	MISO0
24	A13	60	D1	96	NC	132	MOSI0
25	A14	61	FAULTB3	97	V_{REFLO}	133	D11