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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	56800E
Core Size	16-Bit
Speed	60MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	62
Program Memory Size	512KB (256K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	18K x 16
Voltage - Supply (Vcc/Vdd)	2.25V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc56f8366vfve

Table 2-2 Signal and Package Information for the 144-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
D7 **(GPIOF0)**	28	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D7 - D14 specify part of the data for external program or data memory accesses. Depending upon the state of the DRV bit in the EMI bus control register (BCR), D7 - D14 are tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — These eight GPIO pins can be individually programmed as input or output pins. At reset, these pins default to Data Bus functionality. To deactivate the internal pull-up resistor, clear the appropriate GPIO bit in the GPIOF_PUR register. Example: GPIOF0, clear bit 0 in the GPIOF_PUR register.
D8 (GPIOF1)	29			
D9 (GPIOF2)	30			
D10 (GPIOF3)	32			
D11 (GPIOF4)	133			
D12 (GPIOF5)	134			
D13 (GPIOF6)	135			
D14 (GPIOF7)	136			
D15 **(GPIOF8)**	137	Input/ Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Data Bus** — D15 specifies part of the data for external program or data memory accesses. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. **Port F GPIO** — This GPIO pin can be individually programmed as an input or output pin. At reset, this pin defaults to the data bus function. To deactivate the internal pull-up resistor, set bit 8 in the GPIOF_PUR register.

Table 2-2 Signal and Package Information for the 144-Pin LQFP

Signal Name	Pin No.	Type	State During Reset	Signal Description
$\overline{\text{RD}}$	45	Output	In reset, output is disabled, pull-up is enabled	**Read Enable** — $\overline{\text{RD}}$ is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low, pins D0 - D15 become inputs and an external device is enabled onto the data bus. When $\overline{\text{RD}}$ is deasserted high, the external data is latched inside the device. When $\overline{\text{RD}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{CSn}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a static RAM or ROM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{RD}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{\text{WR}}$	44	Output	In reset, output is disabled, pull-up is enabled	**Write Enable** — $\overline{\text{WR}}$ is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low, pins D0 - D15 become outputs and the device puts data on the bus. When $\overline{\text{WR}}$ is deasserted high, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0 - A16, $\overline{\text{PS}}$, $\overline{\text{DS}}$, and $\overline{\text{CSn}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a static RAM. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{WR}}$ is tri-stated when the external bus is inactive. Most designs will want to change the DRV state to DRV = 1 instead of using the default setting. To deactivate the internal pull-up resistor, set the CTRL bit in the SIM_PUDR register.
$\overline{\text{PS}}$ **($\overline{\text{CS0}}$)** **(GPIOD8)**	46	Output Input/ Output	In reset, output is disabled, pull-up is enabled	**Program Memory Select** — This signal is actually $\overline{\text{CS0}}$ in the EMI, which is programmed at reset for compatibility with the 56F80x $\overline{\text{PS}}$ signal. $\overline{\text{PS}}$ is asserted low for external program memory access. Depending upon the state of the DRV bit in the EMI bus control register (BCR), $\overline{\text{PS}}$ is tri-stated when the external bus is inactive. $\overline{\text{CS0}}$ resets to provide the $\overline{\text{PS}}$ function as defined on the 56F80x devices. **Port D GPIO** — This GPIO pin can be individually programmed as an input or output pin. To deactivate the Internal pull-up resistor, clear bit 8 in the GPIOD_PUR register.

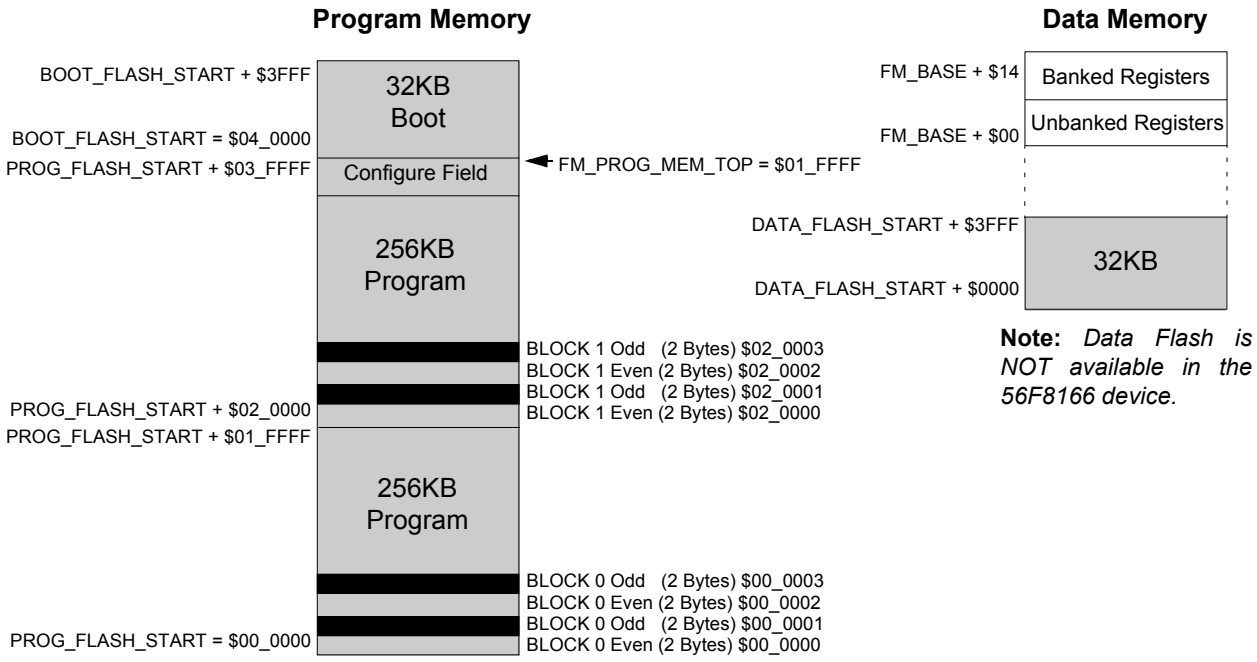


Figure 4-1 Flash Array Memory Maps

Table 4-7 shows the page and sector sizes used within each Flash memory block on the chip.

Note: *Data Flash is NOT available on the 56F8166 device.*

Table 4-7. Flash Memory Partitions

	Flash Size	Sectors	Sector Size	Page Size
Program Flash	512KB	16	16K x 16 bits	1024 x 16 bits
Data Flash	32KB	16	1024 x 16 bits	256 x 16 bits
Boot Flash	32KB	4	4K x 16 bits	512 x 16 bits

Please see **56F8300 Peripheral User Manual** for additional Flash information.

Table 4-9 Data Memory Peripheral Base Address Map Summary (Continued)

Peripheral	Prefix	Base Address	Table Number
SIM	SIM	X:$00 F350	4-35
Power Supervisor	LVI	X:$00 F360	4-36
FM	FM	X:$00 F400	4-37
FlexCAN	FC	X:$00 F800	4-38
FlexCAN2	FC	X:$00 FA00	4-39

Table 4-10 External Memory Integration Registers Address Map (EMI_BASE = $00 F020)

Register Acronym	Address Offset	Register Description	Reset Value
CSBAR 0	$0	Chip Select Base Address Register 0	0x0004 = 64K when EXTBOOT = 0 or EMI_MODE = 0 0x0008 = 1M when EMI_Mode = 1 (Selects entire program space for CS0) Note that A17-A19 are not available in this package
CSBAR 1	$1	Chip Select Base Address Register 1	0x0004 = 64K when EMI_MODE = 0 0x0008 = 1M when EMI_MODE = 1 (Selects A0 - A19 addressable data space for CS1) Note that A17-A19 are not available in this package
CSBAR 2	$2	Chip Select Base Address Register 2	
CSBAR 3	$3	Chip Select Base Address Register 3	
CSBAR 4	$4	Chip Select Base Address Register 4	
CSBAR 5	$5	Chip Select Base Address Register 5	
CSBAR 6	$6	Chip Select Base Address Register 6	
CSBAR 7	$7	Chip Select Base Address Register 7	
CSOR 0	$8	Chip Select Option Register 0	0x5FCB programmed for chip select for program space, word wide, read and write, 11 waits

Table 4-12 Quad Timer B Registers Address Map (Continued)
(TMRB_BASE = $00 F080)
Quad Timer B is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
TMRB1_CMPLD2	$19	Comparator Load Register 2
TMRB1_COMSCR	$1A	Comparator Status and Control Register
		Reserved
TMRB2_CMP1	$20	Compare Register 1
TMRB2_CMP2	$21	Compare Register 2
TMRB2_CAP	$22	Capture Register
TMRB2_LOAD	$23	Load Register
TMRB2_HOLD	$24	Hold Register
TMRB2_CNTR	$25	Counter Register
TMRB2_CTRL	$26	Control Register
TMRB2_SCR	$27	Status and Control Register
TMRB2_CMPLD1	$28	Comparator Load Register 1
TMRB2_CMPLD2	$29	Comparator Load Register 2
TMRB2_COMSCR	$2A	Comparator Status and Control Register
		Reserved
TMRB3_CMP1	$30	Compare Register 1
TMRB3_CMP2	$31	Compare Register 2
TMRB3_CAP	$32	Capture Register
TMRB3_LOAD	$33	Load Register
TMRB3_HOLD	$34	Hold Register
TMRB3_CNTR	$35	Counter Register
TMRB3_CTRL	$36	Control Register
TMRB3_SCR	$37	Status and Control Register
TMRB3_CMPLD1	$38	Comparator Load Register 1
TMRB3_CMPLD2	$39	Comparator Load Register 2
TMRB3_COMSCR	$3A	Comparator Status and Control Register

Table 4-14 Quad Timer D Registers Address Map (Continued)
(TMRD_BASE = $00 F100)
Quad Timer D is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
TMRD3_CTRL	$36	Control Register
TMRD3_SCR	$37	Status and Control Register
TMRD3_CMPLD1	$38	Comparator Load Register 1
TMRD3_CMPLD2	$39	Comparator Load Register 2
TMRD3_COMSCR	$3A	Comparator Status and Control Register

Table 4-15 Pulse Width Modulator A Registers Address Map
(PWMA_BASE = $00 F140)
PWMA is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
PWMA_PMCTL	$0	Control Register
PWMA_PMFCTL	$1	Fault Control Register
PWMA_PMFSA	$2	Fault Status Acknowledge Register
PWMA_PMOUT	$3	Output Control Register
PWMA_PMCNT	$4	Counter Register
PWMA_PWMCM	$5	Counter Modulo Register
PWMA_PWMVAL0	$6	Value Register 0
PWMA_PWMVAL1	$7	Value Register 1
PWMA_PWMVAL2	$8	Value Register 2
PWMA_PWMVAL3	$9	Value Register 3
PWMA_PWMVAL4	$A	Value Register 4
PWMA_PWMVAL5	$B	Value Register 5
PWMA_PMDEADTM	$C	Dead Time Register
PWMA_PMDISMAP1	$D	Disable Mapping Register 1
PWMA_PMDISMAP2	$E	Disable Mapping Register 2
PWMA_PMCFG	$F	Configure Register
PWMA_PMCCR	$10	Channel Control Register
PWMA_PMPORT	$11	Port Register
PWMA_PMICCR	$12	PWM Internal Correction Control Register

Table 4-39 FlexCAN2 Registers Address Map (Continued)
(FC2_BASE = $00 FA00)
FlexCAN2 is NOT available in the 56F8166 device

Register Acronym	Address Offset	Register Description
FC2MB13_DATA	$AC	Message Buffer 13 Data Register
FC2MB13_DATA	$AD	Message Buffer 13 Data Register
FC2MB13_DATA	$AE	Message Buffer 13 Data Register
		Reserved
FC2MB14_CONTROL	$B0	Message Buffer 14 Control / Status Register
FC2MB14_ID_HIGH	$B1	Message Buffer 14 ID High Register
FC2MB14_ID_LOW	$B2	Message Buffer 14 ID Low Register
FC2MB14_DATA	$B3	Message Buffer 14 Data Register
FC2MB14_DATA	$B4	Message Buffer 14 Data Register
FC2MB14_DATA	$B5	Message Buffer 14 Data Register
FC2MB14_DATA	$B6	Message Buffer 14 Data Register
		Reserved
FC2MB15_CONTROL	$B8	Message Buffer 15 Control / Status Register
FC2MB15_ID_HIGH	$B9	Message Buffer 15 ID High Register
FC2MB15_ID_LOW	$BA	Message Buffer 15 ID Low Register
FC2MB15_DATA	$BB	Message Buffer 15 Data Register
FC2MB15_DATA	$BC	Message Buffer 15 Data Register
FC2MB15_DATA	$BD	Message Buffer 15 Data Register
FC2MB15_DATA	$BE	Message Buffer 15 Data Register
		Reserved

4.8 Factory Programmed Memory

The Boot Flash memory block is programmed during manufacturing with a default Serial Bootloader program. The Serial Bootloader application can be used to load a user application into the Program and *Data Flash* (*NOT available in the 56F8166 device*) memories of the device. The **56F83xx SCI/CAN Bootloader User Manual (MC56F83xxBLUM)** provides detailed information on this firmware. An application note, **Production Flash Programming (AN1973),** details how the Serial Bootloader program can be used to perform production flash programming of the on board flash memories as well as other potential methods.

Like all the flash memory blocks the Boot Flash can be erased and programmed by the user. The Serial Bootloader application is programmed as an aid to the end user, but is not required to be used or maintained in the Boot Flash memory.

Part 5 Interrupt Controller (ITCN)

5.1 Introduction

The Interrupt Controller (ITCN) module is used to arbitrate between various interrupt requests (IRQs), to signal to the 56800E core when an interrupt of sufficient priority exists, and to what address to jump in order to service this interrupt.

5.2 Features

The ITCN module design includes these distinctive features:

- Programmable priority levels for each IRQ
- Two programmable Fast Interrupts
- Notification to SIM module to restart clocks out of Wait and Stop modes
- Drives initial address on the address bus after reset

For further information, see **Table 4-5**, Interrupt Vector Table Contents.

5.3 Functional Description

The Interrupt Controller is a slave on the IPBus. It contains registers allowing each of the 86 interrupt sources to be set to one of four priority levels, excluding certain interrupts of fixed priority. Next, all of the interrupt requests of a given level are priority encoded to determine the lowest numerical value of the active interrupt requests for that level. Within a given priority level, zero is the highest priority, while number 85 is the lowest.

5.3.1 Normal Interrupt Handling

Once the ITCN has determined that an interrupt is to be serviced and which interrupt has the highest priority, an interrupt vector address is generated. Normal interrupt handling concatenates the VBA and the vector number to determine the vector address. In this way, an offset is generated into the vector table for each interrupt.

5.3.2 Interrupt Nesting

Interrupt exceptions may be nested to allow an IRQ of higher priority than the current exception to be serviced. The following tables define the nesting requirements for each priority level.

Table 5-1 Interrupt Mask Bit Definition

SR[9][1]	SR[8][1]	Permitted Exceptions	Masked Exceptions
0	0	Priorities 0, 1, 2, 3	None
0	1	Priorities 1, 2, 3	Priority 0
1	0	Priorities 2, 3	Priorities 0, 1
1	1	Priority 3	Priorities 0, 1, 2

1. Core status register bits indicating current interrupt mask within the core.

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	IPR0	R	0	0	BKPT_U0 IPL		STPCNT IPL		0	0	0	0	0	0	0	0	0	0
		W																
$1	IPR1	R	0	0	0	0	0	0	0	0	0	0	RX_REG IPL		TX_REG IPL		TRBUF IPL	
		W																
$2	IPR2	R	FMCBE IPL		FMCC IPL		FMERR IPL		LOCK IPL		LVI IPL		0	0	IRQB IPL		IRQA IPL	
		W																
$3	IPR3	R	GPIOD IPL		GPIOE IPL		GPIOF IPL		FCMSGBUF IPL		FCWKUP IPL		FCERR IPL		FCBOFF IPL		0	0
		W																
$4	IPR4	R	SPI0_RCV IPL		SPI1_XMIT IPL		SPI1_RCV IPL		0	0	0	0	GPIOA IPL		GPIOB IPL		GPIOC IPL	
		W																
$5	IPR5	R	DEC1_XIRQ IPL		DEC1_HIRQ IPL		SCI1_RCV IPL		SCI1_RERR IPL		0	0	SCI1_TIDL IPL		SCI1_XMIT IPL		SPI0_XMIT IPL	
		W																
$6	IPR6	R	TMRC0 IPL		TMRD3 IPL		TMRD2 IPL		TMRD1 IPL		TMRD0 IPL		0	0	DEC0_XIRQ IPL		DEC0_HIRQ IPL	
		W																
$7	IPR7	R	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
		W																
$8	IPR8	R	SCI0_RCV IPL		SCI0_RERR IPL		0	0	SCI0_TIDL IPL		SCI0_XMIT IPL		TMRA3 IPL		TMRA2 IPL		TMRA1 IPL	
		W																
$9	IPR9	R	PWMA F IPL		PWMB F IPL		PWMA_RL IPL		PWMB_RL IPL		ADCA_ZC IPL		ABCB_ZC IPL		ADCA_CC IPL		ADCB_CC IPL	
		W																
$A	VBA	R	0	0	0	VECTOR BASE ADDRESS												
		W																
$B	FIM0	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0						
		W																
$C	FIVAL0	R	FAST INTERRUPT 0 VECTOR ADDRESS LOW															
		W																
$D	FIVAH0	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 0 VECTOR ADDRESS HIGH				
		W																
$E	FIM1	R	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1						
		W																
$F	FIVAL1	R	FAST INTERRUPT 1 VECTOR ADDRESS LOW															
		W																
$10	FIVAH1	R	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
		W																
$11	IRQP0	R	PENDING [16:2]															1
		W																
$12	IRQP1	R	PENDING [32:17]															
		W																
$13	IRQP2	R	PENDING [48:33]															
		W																
$14	IRQP3	R	PENDING [64:49]															
		W																
$15	IRQP4	R	PENDING [80:65]															
		W																
$16	IRQP5	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	PENDING [81]
		W																
	Reserved																	
$1D	ICTL	R	INT	IPIC		VAB							INT_DIS	1	IRQB STATE	IRQA STATE	$\overline{\text{IRQB}}$ EDG	$\overline{\text{IRQA}}$ EDG
		W																
	Reserved																	
$1F	IPR10	R	0	0	0	0	0	0	0	0	FLEXCAN2 MSGBUF IPL		FLEXCAN2 WKUP IPL		FLEXCAN2 ERR IPL		FLEXCAN2 BOFF IPL	
		W																

= Reserved

Figure 5-2 ITCN Register Map Summary

5.6.7.7 Quadrature Decoder 0, INDEX Pulse Interrupt Priority Level (DEC0_XIRQ IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.7.8 Quadrature Decoder 0, HOME Signal Transition or Watchdog Timer Interrupt Priority Level (DEC0_HIRQ IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.8 Interrupt Priority Register 7 (IPR7)

Base + $7	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Write	TMRA0 IPL		TMRB3 IPL		TMRB2 IPL		TMRB1 IPL		TMRB0 IPL		TMRC3 IPL		TMRC2 IPL		TMRC1 IPL	
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-10 Interrupt Priority Register (IPR7)

5.6.8.1 Timer A, Channel 0 Interrupt Priority Level (TMRA0 IPL)—Bits 15–14

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.2 SCI0 Receiver Error Interrupt Priority Level (SCI0_RERR IPL)—Bits 13–12

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.3 Reserved—Bits 11–10

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.9.4 SCI0 Transmitter Idle Interrupt Priority Level (SCI0_TIDL IPL)—Bits 9–8

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.5 SCI0 Transmitter Empty Interrupt Priority Level (SCI0_XMIT IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.9.6 Timer A, Channel 3 Interrupt Priority Level (TMRA3 IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.17 Fast Interrupt 1 Vector Address High Register (FIVAH1)

Base + $10	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	0	0	FAST INTERRUPT 1 VECTOR ADDRESS HIGH				
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-19 Fast Interrupt 1 Vector Address High Register (FIVAH1)

5.6.17.1 Reserved—Bits 15–5

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

5.6.17.2 Fast Interrupt 1 Vector Address High (FIVAH1)—Bits 4–0

The upper five bits of the vector address are used for Fast Interrupt 1. This register is combined with FIVAL1 to form the 21-bit vector address for Fast Interrupt 1 defined in the FIM1 register.

5.6.18 IRQ Pending 0 Register (IRQP0)

Base + $11	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [16:2]															1
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-20 IRQ Pending 0 Register (IRQP0)

5.6.18.1 IRQ Pending (PENDING)—Bits 16–2

This register combines with the other five to represent the pending IRQs for interrupt vector numbers 2 through 81.

- 0 = IRQ pending for this vector number
- 1 = No IRQ pending for this vector number

5.6.18.2 Reserved—Bit 0

This bit is reserved or not implemented. It is read as 1 and cannot be modified by writing.

5.6.19 IRQ Pending 1 Register (IRQP1)

$Base + $12	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	PENDING [32:17]															
Write																
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 5-21 IRQ Pending 1 Register (IRQP1)

5.6.32.2 FlexCAN2 Message Buffer Interrupt Priority Level (FlexCAN2_MSGBUF IPL)—Bits 7–6

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.3 FlexCAN2 Wake Up Interrupt Priority Level (FlexCAN2_WKUP IPL)—Bits 5–4

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.4 FlexCAN2 Error Interrupt Priority Level (FlexCAN2_ERR IPL)—Bits 3–2

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

5.6.32.5 FlexCAN2 Bus-Off Interrupt Priority Level (FlexCAN2_BOFF IPL)—Bits 1–0

This field is used to set the interrupt priority level for IRQs. This IRQ is limited to priorities 0 through 2. They are disabled by default.

- 00 = IRQ disabled (default)
- 01 = IRQ is priority level 0
- 10 = IRQ is priority level 1
- 11 = IRQ is priority level 2

Add. Offset	Register Name		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$0	SIM_CONTROL	R	0	0	0	0	0	0	0	0	0	EMI_MODE	ONCE EBL	SW RST	STOP_DISABLE		WAIT_DISABLE	
		W																
$1	SIM_RSTSTS	R	0	0	0	0	0	0	0	0	0	0	SWR	COPR	EXTR	POR	0	0
		W																
$2	SIM_SCR0	R	FIELD															
		W																
$3	SIM_SCR1	R	FIELD															
		W																
$4	SIM_SCR2	R	FIELD															
		W																
$5	SIM_SCR3	R	FIELD															
		W																
$6	SIM_MSH_ID	R	0	0	0	0	0	0	0	1	1	1	0	1	0	1	1	0
		W																
$7	SIM_LSH_ID	R	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1
		W																
$8	SIM_PUDR	R	0	PWMA 1	CAN	EMI_MODE	$\overline{\text{RESET}}$	IRQ	XBOOT	PWMB	PWMA 0	0	CTRL	0	JTAG	0	0	0
		W																
	Reserved																	
$A	SIM_CLKOSR	R	0	0	0	0	0	0	$\overline{\text{A23}}$	$\overline{\text{A22}}$	$\overline{\text{A21}}$	$\overline{\text{A20}}$	CLKDIS	CLKOSEL				
		W																
$B	SIM_GPS	R	0	0	0	0	0	0	0	0	0	0	D1	D0	C3	C2	C1	C0
		W																
$C	SIM_PCE	R	EMI	ADCB	ADCA	CAN	DEC1	DEC0	TMRD	TMRC	TMRB	TMRA	SCI1	SCI0	SPI1	SPI0	PWMB	PWMA
		W																
$D	SIM_ISALH	R	1	1	1	1	1	1	1	1	1	1	1	1	1	1	ISAL[23:22]	
		W																
$E	SIM_ISALL	R	ISAL[21:6]															
		W																
$F	SIM_PCE2	R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CAN2
		W																

= Reserved

Figure 6-2 SIM Register Map Summary

6.5.1 SIM Control Register (SIM_CONTROL)

Base + $0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	0	0	0	0	0	0	0	0	0	EMI_MODE	ONCE EBL	SW RST	STOP_DISABLE		WAIT_DISABLE	
Write																
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-3 SIM Control Register (SIM_CONTROL)

6.5.1.1 Reserved—Bits 15–7

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.1 Reserved—Bits 15–6

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

6.5.2.2 Software Reset (SWR)—Bit 5

When 1, this bit indicates that the previous reset occurred as a result of a software reset (write to SW RST bit in the SIM_CONTROL register). This bit will be cleared by any hardware reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.3 COP Reset (COPR)—Bit 4

When 1, the COPR bit indicates the Computer Operating Properly (COP) timer-generated reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit will clear it.

6.5.2.4 External Reset (EXTR)—Bit 3

If 1, the EXTR bit indicates an external system reset has occurred. This bit will be cleared by a Power-On Reset or by software. Writing a 0 to this bit position will set the bit, while writing a 1 to the bit position will clear it. Basically, when the EXTR bit is 1, the previous system reset was caused by the external RESET pin being asserted low.

6.5.2.5 Power-On Reset (POR)—Bit 2

When 1, the POR bit indicates a Power-On Reset occurred some time in the past. This bit can be cleared only by software or by another type of reset. Writing a 0 to this bit will set the bit, while writing a 1 to the bit position will clear the bit. In summary, if the bit is 1, the previous system reset was due to a Power-On Reset.

6.5.2.6 Reserved—Bits 1–0

This bit field is reserved or not implemented. It is read as 0 and cannot be modified by writing.

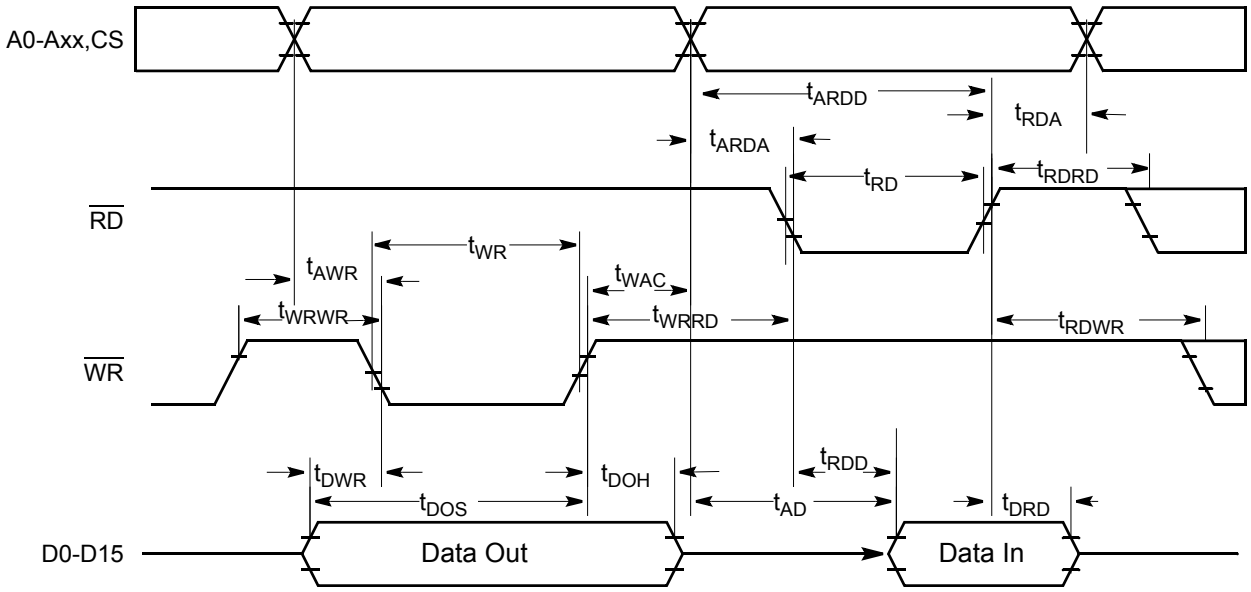
6.5.3 SIM Software Control Registers (SIM_SCR0, SIM_SCR1, SIM_SCR2, and SIM_SCR3)

Only SIM_SCR0 is shown below. SIM_SCR1, SIM_SCR2, and SIM_SCR3 are identical in functionality.

Base + $2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read	FIELD															
Write																
POR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 6-5 SIM Software Control Register 0 (SIM_SCR0)

The timing of write cycles is different when WWS = 0 than when WWS > 0. Therefore, some parameters contain two sets of numbers to account for this difference. Use the “Wait States Configuration” column of **Table 10-16** to make the appropriate selection.



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 10-5 External Memory Interface Timing

Note: When multiple lines are given for the same wait state configuration, calculate each and then select the smallest or most negative.

Table 10-16 External Memory Interface Timing

Characteristic	Symbol	Wait States Configuration	D	M	Wait States Controls	Unit
Address Valid to $\overline{WR}$ Asserted	t_{AWR}	WWS=0	-2.076	0.50	WWSS	ns
		WWS>0	-1.795	0.75 + DCAOE		
$\overline{WR}$ Width Asserted to $\overline{WR}$ Deasserted	t_{WR}	WWS=0	-0.094	0.25 + DCAOE	WWS	ns
		WWS>0	-0.012	0		
Data Out Valid to $\overline{WR}$ Asserted	t_{DWR}	WWS=0	-9.321	0.25 + DCAEO	WWSS	ns
		WWS=0	-1.160	0.00		
		WWS>0	-8.631	0.50		
		WWS>0	-0.879	0.25 + DCAOE		
Valid Data Out Hold Time after $\overline{WR}$ Deasserted	t_{DOH}		-2.086	0.25 + DCAEO	WWSH	ns

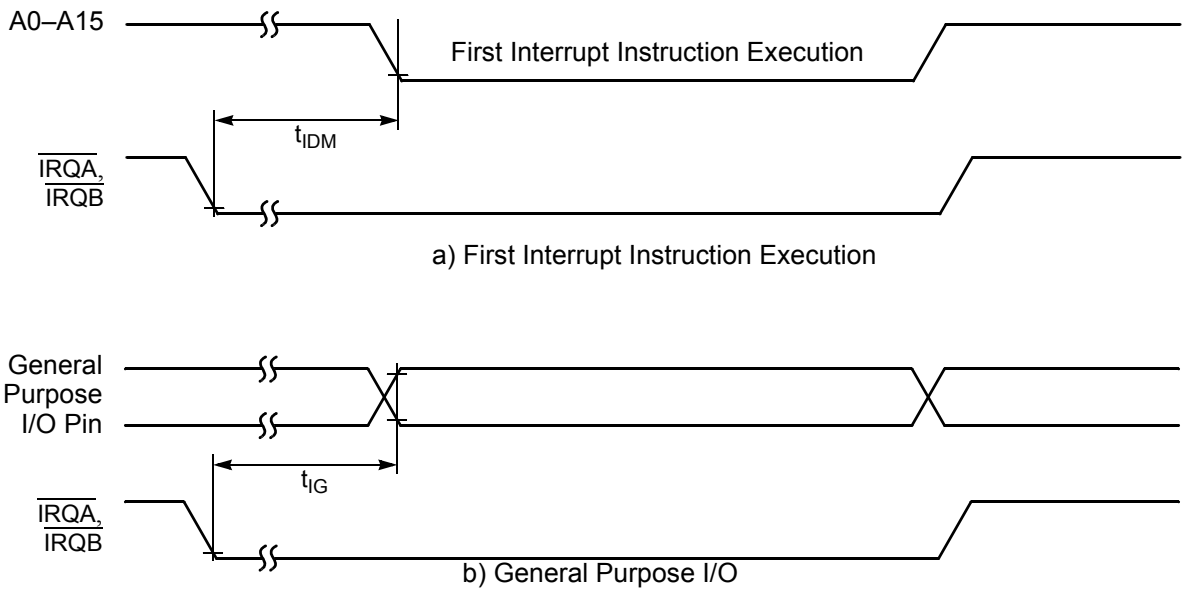


Figure 10-8 External Level-Sensitive Interrupt Timing

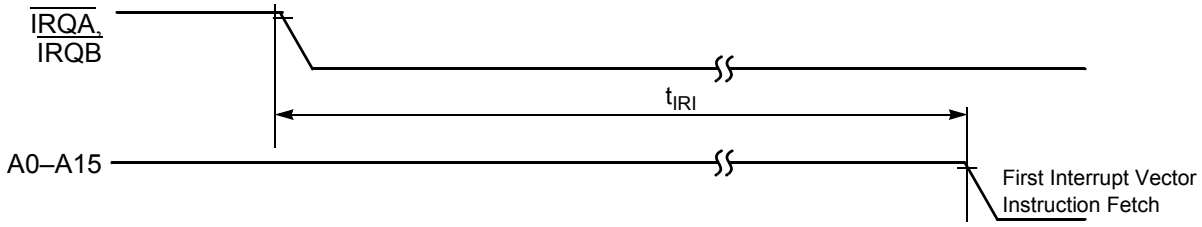


Figure 10-9 Interrupt from Wait State Timing

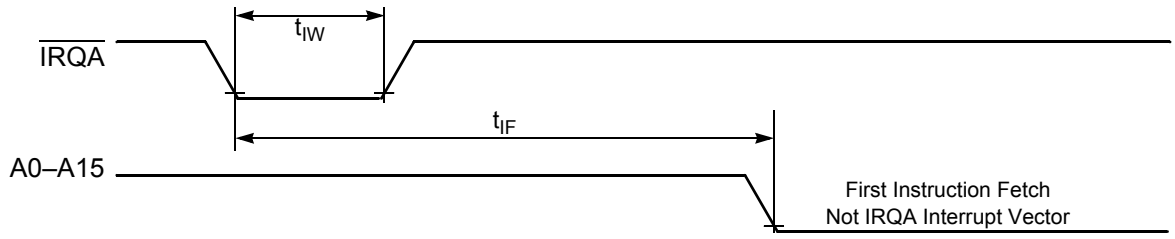


Figure 10-10 Recovery from Stop State Using Asynchronous Interrupt Timing

10.10 Serial Peripheral Interface (SPI) Timing

Table 10-18 SPI Timing[1]

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 50	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	10-14
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	10-14
Clock (SCK) high time Master Slave	t_{CH}	 17.6 25	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Clock (SCK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	10-14
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	10-11, 10-12, 10-13, 10-14
Access time (time to data active from high-impedance state) Slave	t_A	4.8	15	ns	10-14
Disable time (hold time to high-impedance state) Slave	t_D	3.7	15.2	ns	10-14
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	10-11, 10-12, 10-13, 10-14
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	10-11, 10-12, 10-13
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	10-11, 10-12, 10-13, 10-14
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	10-11, 10-12, 10-13, 10-14

1. Parameters listed are guaranteed by design.

Table 10-24 ADC Parameters (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Calibration Factor 1[7]	CF1	—	—	0.002289	—
Calibration Factor 2	CF2	—	—	–25.6	—
Crosstalk between channels	—	—	-60	—	dB
Common Mode Voltage	V_{common}	—	$(V_{REFH} - V_{REFLO}) / 2$	—	V
Signal-to-noise ratio	SNR	—	64.6	—	db
Signal-to-noise plus distortion ratio	SINAD	—	59.1	—	db
Total Harmonic Distortion	THD	—	60.6	—	db
Spurious Free Dynamic Range	SFDR	—	61.1	—	db
Effective Number Of Bits[8]	ENOB	—	9.6	—	Bits

1. INL measured from $V_{in} = .1V_{REFH}$ to $V_{in} = .9V_{REFH}$ 10% to 90% Input Signal Range
2. LSB = Least Significant Bit
3. ADC clock cycles
4. Assumes each voltage reference pin is bypassed with 0.1μF ceramic capacitors to ground
5. The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC. This allows the ADC to operate in noisy industrial environments where inductive flyback is possible.
6. Absolute error includes the effects of both gain error and offset error.
7. Please see the **56F8300Peripheral User's Manual** for additional information on ADC calibration.
8. ENOB = (SINAD - 1.76)/6.02

Table 11-2 56F8166 144-Pin LQFP Package Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
26	A15	62	NC	98	V_{REFN}	134	D12
27	V_{SS}	63	V_{SS}	99	V_{REFMID}	135	D13
28	D7	64	NC	100	V_{REFP}	136	D14
29	D8	65	NC	101	V_{REFH}	137	D15
30	D9	66	V_{DD_IO}	102	V_{DDA_ADC}	138	A0
31	V_{DD_IO}	67	NC	103	V_{SSA_ADC}	139	PHASEA0
32	D10	68	NC	104	ANB0	140	PHASEB0
33	GPIOB0	69	V_{SS}	105	ANB1	141	INDEX0
34	PWMB0	70	NC	106	ANB2	142	HOME0
35	PWMB1	71	NC	107	ANB3	143	EMI_MODE
36	PWMB2	72	D2	108	ANB4	144	V_{SS}