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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, Serial Port
Clock Rate	66MHz
Non-Volatile Memory	External
On-Chip RAM	192kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-2189mbstz-266

ADSP-2189M* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- EZ-KIT Lite Evaluation Kit for ADSP-218x Processor

DOCUMENTATION

Application Notes

- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-227: Digital Control System Design with the ADSP-2100 Family
- AN-334: Digital Signal Processing Techniques
- AN-524: ADV601/ADV611 Bin Width Calculation in ADSP-21xx DSP
- EE-06: ADSP-21xx Serial Port Startup Issues
- EE-100: ADSP-218x External Overlay Memory
- EE-102: Mode D and ADSP-218x Pin Compatibility - the FAQs
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-11: ADSP-2181 Priority Chain & IDMA Holdoffs
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-115: ADSP-2189 IDMA Interface to Motorola MC68300 Family of Microprocessors
- EE-12: Interrupts and Programmable Flags on the ADSP-2185/2186
- EE-121: Porting Code from ADSP-21xx to ADSP-219x
- EE-122: Coding for Performance on the ADSP-219x
- EE-123: An Overview of the ADSP-219x Pipeline
- EE-124: Booting up the ADSP-2192
- EE-125: ADSP-218x Embedded System Software Management and In-System-Programming (ISP)
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-129: ADSP-2192 Interprocessor Communication
- EE-130: Making Fast Transition from ADSP-21xx to ADSP-219x
- EE-131: Booting the ADSP-2191/95/96 DSPs
- EE-133: Converting From Legacy Architecture Files To Linker Description Files for the ADSP-218x
- EE-139: Interfacing the ADSP-2191 to an AD7476 via the SPI Port
- EE-142: Autobuffering, C and FFTs on the ADSP-218x
- EE-144: Creating a Master-Slave SPI Interface Between Two ADSP-2191 DSPs
- EE-145: SPI Booting of the ADSP-2191 using the Atmel AD25020N on an EZ-KIT Lite Evaluation Board

Fabricated in a high speed, low power, CMOS process, the ADSP-2189M operates with a 13.3 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2189M's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle, the ADSP-2189M can:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computational operation

This takes place while the processor continues to:

- Receive and transmit data through the two serial ports
- Receive and/or transmit data through the internal DMA port
- Receive and/or transmit data through the byte DMA port
- Decrement timer

DEVELOPMENT SYSTEM

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2189M. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment.

A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-2189M assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

The EZ-KIT Lite is a hardware/software kit offering a complete development environment for the entire ADSP-21xx family: an ADSP-218x-based evaluation board with PC monitor software plus Assembler, Linker, Simulator and PROM Splitter software. The ADSP-218x EZ-KIT Lite is a low cost, easy to use hardware platform on which you can quickly get started with your DSP software design. The EZ-KIT Lite includes the following features:

- 33 MHz ADSP-218x
- Full 16-bit Stereo Audio I/O with AD1847 SoundPort® Codec
- RS-232 Interface to PC with Windows 3.1 Control Software
- EZ-ICE Connector for Emulator Control
- DSP Demo Programs

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-2189M system. The emulator consists of hardware, host computer resident software and the target board connector. The ADSP-2189M integrates on-chip emulation support with a 14-pin ICE-Port interface. This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 Family EZ-ICEs. The ADSP-2189M device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 20 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

See "Designing An EZ-ICE-Compatible Target System" in the *ADSP-2100 Family EZ-Tools Manual* (ADSP-2181 sections) as well as the Designing an EZ-ICE compatible System section of this data sheet for the exact specifications of the EZ-ICE target board connector.

Additional Information

This data sheet provides a general overview of ADSP-2189M functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual*, Third Edition. For more information about the development tools, refer to the ADSP-2100 Family Development Tools Data Sheet.

ARCHITECTURE OVERVIEW

The ADSP-2189M instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2189M assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

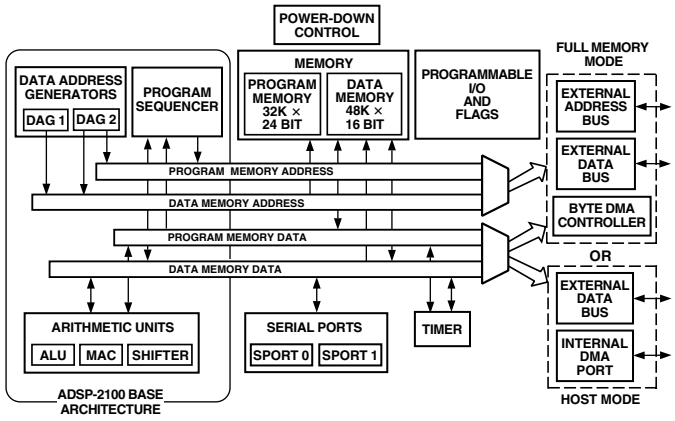


Figure 1. Functional Block Diagram

Figure 1 is an overall block diagram of the ADSP-2189M. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization and derive exponent operations.

The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

EZ-ICE and SoundPort are registered trademarks of Analog Devices, Inc.

Table II. ADSP-2189M Modes of Operation

MODE D	MODE C	MODE B	MODE A	Booting Method
X	0	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Full Memory Mode.[1]
X	0	1	0	No automatic boot operations occur. Program execution starts at external memory location 0. Chip is configured in Full Memory Mode. BDMA can still be used but the processor does not automatically use or wait for these operations.
0	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down. (**REQUIRES ADDITIONAL HARDWARE**).
0	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. $\overline{\text{IACK}}$ has active pull-down.[1]
1	1	0	0	BDMA feature is used to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded. Chip is configured in Host Mode; $\overline{\text{IACK}}$ requires external pull-down. (**REQUIRES ADDITIONAL HARDWARE**).
1	1	0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to. Chip is configured in Host Mode. $\overline{\text{IACK}}$ requires external pull-down.[1]

NOTE
[1]Considered as standard operating settings. Using these configurations allows for easier design and better memory management.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting, the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Power Supplies

The ADSP-2189M has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply can be connected to either a 2.5 V or 3.3 V supply. All external supply pins must be connected to the same supply. All input and I/O pins can tolerate input voltages up to 3.6 V regardless of the external supply voltage. This feature provides maximum flexibility in mixing 2.5 V and 3.3 V components.

MODES OF OPERATION

Setting Memory Mode

Memory Mode selection for the ADSP-2189M is made during chip reset through the use of the Mode C pin. This pin is multiplexed with the DSP's PF2 pin, so care must be taken in how the mode selection is made. The two methods for selecting the value of Mode C are active and passive.

Passive Configuration involves the use a pull-up or pull-down resistor connected to the Mode C pin. To minimize power consumption, or if the PF2 pin is to be used as an output in the DSP application, a weak pull-up or pull-down, on the order of 10 kΩ, can be used. This value should be sufficient to pull the pin to the desired level and still allow the pin to operate as a programmable flag output without undue strain on the processor's output driver. For minimum power consumption during power-down, reconfigure PF2 to be an input, as the pull-up or pull-down will hold the pin in a known state and will not switch.

Active Configuration involves the use of a three-statable external driver connected to the Mode C pin. A driver's output enable should be connected to the DSP's $\overline{\text{RESET}}$ signal such that it only drives the PF2 pin when $\overline{\text{RESET}}$ is active (low). When $\overline{\text{RESET}}$ is deasserted, the driver should three-state, thus allowing full use of the PF2 pin as either an input or output. To minimize power consumption during power-down, configure the programmable flag as an output when connected to a three-stated buffer. This ensures that the pin will be held at a constant level and will not oscillate should the three-state driver's level hover around the logic switching point.

$\overline{\text{IACK}}$ Configuration

Mode D = 0 and in host mode: $\overline{\text{IACK}}$ is an active, driven signal and cannot be wire OR-ed.

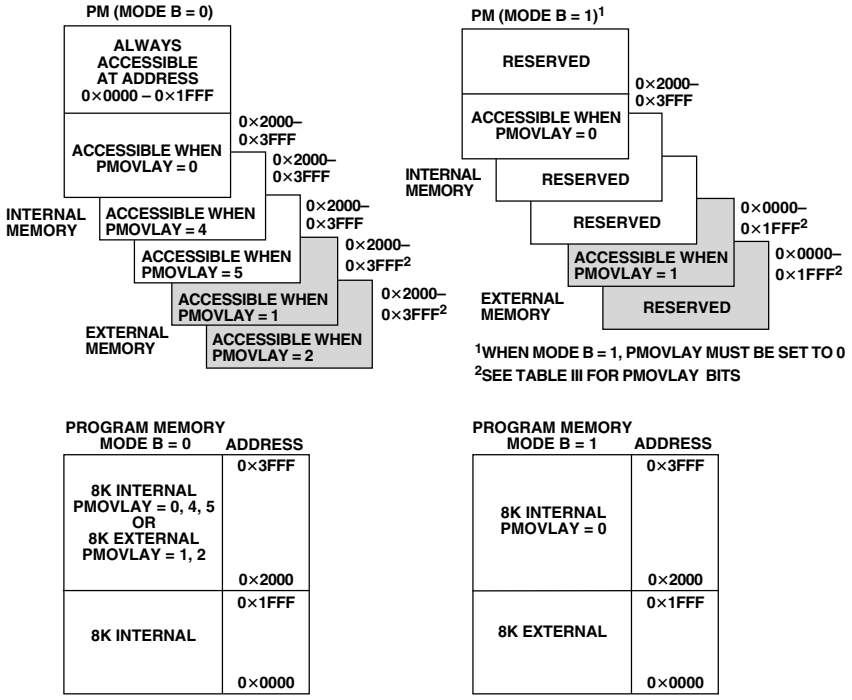


Figure 4. Program Memory

Mode D = 1 and in host mode: $\overline{\text{IACK}}$ is an open source and requires an external pull-down, but multiple $\overline{\text{IACK}}$ pins can be wire OR-ed together.

MEMORY ARCHITECTURE

The ADSP-2189M provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory and I/O. Refer to the following figures and tables for PM and DM memory allocations in the ADSP-2189M.

Program Memory

Program Memory, *Full Memory Mode* is a 24-bit-wide space for storing both instruction op codes and data. The ADSP-2189M has 32K words of Program Memory RAM on chip and the capability of accessing up to two 8K external memory overlay spaces using the external data bus.

Program Memory, *Host Mode* allows access to all internal memory. External overlay access is limited by a single external address line (A0). External program execution is not available in host mode due to a restricted data bus that is 16-bits wide only.

Table III. PMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0, 4, 5	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Data Memory

Data Memory, *Full Memory Mode* is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2189M has 48K words on Data Memory RAM on-chip. Part of this space is used by 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus. All internal accesses complete in one cycle. Accesses to external memory are timed using the wait-states specified by the DWAIT register and the wait-state mode bit.

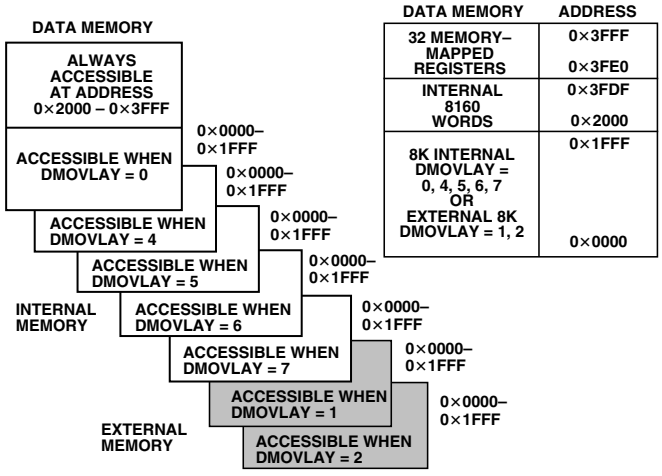


Figure 5. Data Memory Map

Data Memory, *Host Mode* allows access to all internal memory. External overlay access is limited by a single external address line (A0).

Table IV. DMOVLAY Bits

PMOVLAY	Memory	A13	A12:0
0, 4, 5, 6, 7	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

Memory Mapped Registers (New to the ADSP-2189M)
The ADSP-2189M has three memory mapped registers that differ from other ADSP-21xx Family DSPs. The slight modifications to these registers (Wait-State Control, Programmable Flag and Composite Select Control and System Control) provide the ADSP-2189M's wait-state and $\overline{\text{BMS}}$ control features.

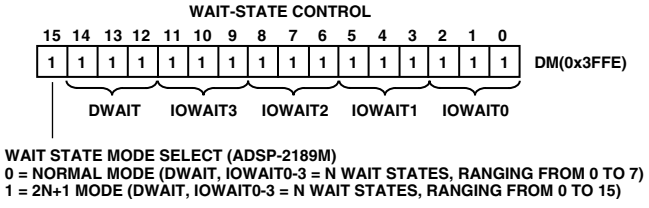


Figure 6. Wait-State Control Register (ADSP-2189M)

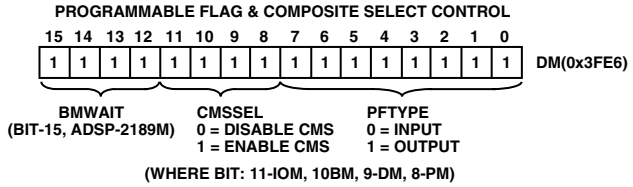


Figure 7. Programmable Flag and Composite Select Control Register

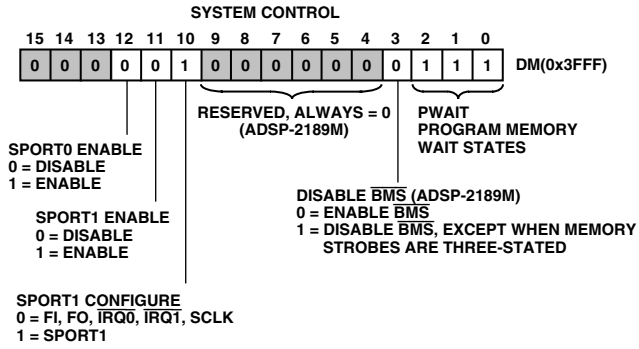


Figure 8. System Control Register

I/O Space (Full Memory Mode)
The ADSP-2189M supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals (such as data converters and external registers) or to bus interface ASIC data registers. I/O space supports 2048 locations of 16-bit-wide data. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait-state registers, IOWAIT0–3, which, in combination with the wait-state mode bit, specify up to 15 wait-states to be automatically generated for each of four regions. The wait-states act on address ranges as shown in Table V.

Table V. Wait-States

Address Range	Wait-State Register
0x000–0x1FF	IOWAIT0 and Wait-State Mode Select Bit
0x200–0x3FF	IOWAIT1 and Wait-State Mode Select Bit
0x400–0x5FF	IOWAIT2 and Wait-State Mode Select Bit
0x600–0x7FF	IOWAIT3 and Wait-State Mode Select Bit

Composite Memory Select ($\overline{\text{CMS}}$)
The ADSP-2189M has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

When set, each bit in the CMSSEL register causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals, with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All enable bits default to 1 at reset, except the $\overline{\text{BMS}}$ bit.

Byte Memory Select ($\overline{\text{BMS}}$)
The ADSP-2189M's $\overline{\text{BMS}}$ disable feature combined with the $\overline{\text{CMS}}$ pin lets you use multiple memories in the byte memory space. For example, an EPROM could be attached to the $\overline{\text{BMS}}$ select, and an SRAM could be connected to $\overline{\text{CMS}}$. Because $\overline{\text{BMS}}$ is enabled at reset, the EPROM would be used for booting. After booting, software could disable $\overline{\text{BMS}}$ and set the $\overline{\text{CMS}}$ signal to respond to $\overline{\text{BMS}}$, enabling the SRAM.

Bus Request and Bus Grant
The ADSP-2189M can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2189M is not performing an external memory access, it responds to the active $\overline{BR}$ input in the following processor cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal, and
- Halting program execution.

If Go Mode is enabled, the ADSP-2189M will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2189M is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point at which it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2189M requires the external bus for a memory or BDMA access, but is stopped. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2189M deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

Flag I/O Pins
The ADSP-2189M has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2189M's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2189M has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1 and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

Note: Pins PF0, PF1, PF2 and PF3 are also used for device configuration during reset.

INSTRUCTION SET DESCRIPTION

The ADSP-2189M assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source-and-object-code-compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2189M's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

DESIGNING AN EZ-ICE-COMPATIBLE SYSTEM

The ADSP-2189M has on-chip emulation support and an ICE-Port, a special set of pins that interface to the EZ-ICE. These features allow in-circuit emulation without replacing the target system processor by using only a 14-pin connection from the target system to the EZ-ICE. Target systems must have a 14-pin connector to accept the EZ-ICE's in-circuit probe, a 14-pin plug.

Issuing the chip reset command during emulation causes the DSP to perform a full chip reset, including a reset of its memory mode. Therefore, it is vital that the mode pins are set correctly PRIOR to issuing a chip reset command from the emulator user interface. If you are using a passive method of maintaining mode information (as discussed in Setting Memory Modes), then it does not matter that the mode information is latched by an emulator reset. However, if using the $\overline{RESET}$ pin as a method of setting the value of the mode pins, the effects of an emulator reset must be taken into consideration.

One method of ensuring that the values located on the mode pins are those desired is to construct a circuit like the one shown in Figure 12. This circuit forces the value located on the Mode A pin to logic high; regardless if it latched via the $\overline{RESET}$ or $\overline{ERESET}$ pin.

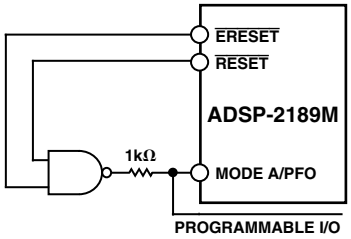


Figure 12. Mode A Pin/EZ-ICE Circuit

See the ADSP-2100 Family EZ-Tools data sheet for complete information on ICE products.

The ICE-Port interface consists of the following ADSP-2189M pins: $\overline{EBR}$, $\overline{EINT}$, EE, $\overline{EBG}$, ECLK, $\overline{ERESET}$, ELIN, $\overline{EMS}$, and ELOUT.

These ADSP-2189M pins must be connected only to the EZ-ICE connector in the target system. These pins have no function except during emulation, and do not require pull-up or pull-down resistors. The traces for these signals between the ADSP-2189M and the connector must be kept as short as possible, no longer than three inches.

The following pins are also used by the EZ-ICE: $\overline{BR}$, $\overline{BG}$, $\overline{RESET}$, and GND.

The EZ-ICE uses the EE (emulator enable) signal to take control of the ADSP-2189M in the target system. This causes the processor to use its $\overline{ERESET}$, $\overline{EBR}$, and $\overline{EBG}$ pins instead of the $\overline{RESET}$, $\overline{BR}$, and $\overline{BG}$ pins. The $\overline{BG}$ output is three-stated. These signals do not need to be jumper-isolated in your system.

The EZ-ICE connects to your target system via a ribbon cable and a 14-pin female plug. The female plug is plugged onto the 14-pin connector (a pin strip header) on the target board.

Target Board Connector for EZ-ICE Probe
The EZ-ICE connector (a standard pin strip header) is shown in Figure 13. You must add this connector to your target board design if you intend to use the EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

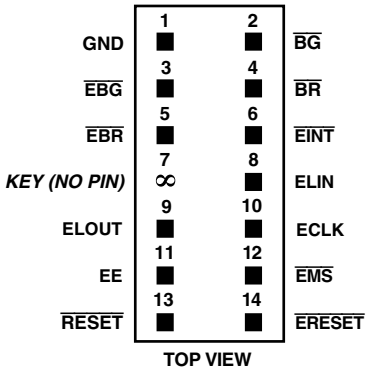


Figure 13. Target Board Connector for EZ-ICE

The 14-pin, 2-row pin strip header is keyed at the Pin 7 location—you must remove Pin 7 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The pin strip header must have at least 0.15 inch clearance on all sides to accept the EZ-ICE probe plug.

Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

Target Memory Interface
For your target system to be compatible with the EZ-ICE emulator, it must comply with the memory interface guidelines listed below.

PM, DM, BM, IOM, and CM

Design your Program Memory (PM), Data Memory (DM), Byte Memory (BM), I/O Memory (IOM), and Composite Memory (CM) external interfaces to comply with worst case device timing requirements and switching characteristics as specified in this data sheet. The performance of the EZ-ICE may approach published worst case specification for some memory access timing requirements and switching characteristics.

Note: If your target does not meet the worst case chip specification for memory access parameters, you may not be able to emulate your circuitry at the desired CLKIN frequency. Depending on the severity of the specification violation, you may have trouble manufacturing your system as DSP components statistically vary in switching characteristic and timing requirements within published limits.

Restriction: All memory strobe signals on the ADSP-2189M ($\overline{RD}$, $\overline{WR}$, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, and $\overline{IOMS}$) used in your target system must have 10 kΩ pull-up resistors connected when the EZ-ICE is being used. The pull-up resistors are necessary because there are no internal pull-ups to guarantee their state during prolonged three-state conditions resulting from typical EZ-ICE debugging sessions. These resistors may be removed at your option when the EZ-ICE is not being used.

Target System Interface Signals
When the EZ-ICE board is installed, the performance on some system signals change. Design your system to be compatible with the following system interface signal changes introduced by the EZ-ICE board:

- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{RESET}$ signal.
- EZ-ICE emulation introduces an 8 ns propagation delay between your target circuitry and the DSP on the $\overline{BR}$ signal.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when single-stepping.
- EZ-ICE emulation ignores $\overline{RESET}$ and $\overline{BR}$ when in Emulator Space (DSP halted).
- EZ-ICE emulation ignores the state of target $\overline{BR}$ in certain modes. As a result, the target system may take control of the DSP's external memory bus only if bus grant ($\overline{BG}$) is asserted by the EZ-ICE board's DSP.

ADSP-2189M–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter	K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DDINT}	2.37	2.63	2.25	2.75	V
V_{DDEXT}	2.37	3.6	2.25	3.6	V
V_{INPUT}[1]	V_{IL} = –0.3	V_{IH} = 3.6	–0.03	3.6	V
T_{AMB}	0	+70	–40	+85	°C

NOTES

[1]The ADSP-2189M is 3.3 V tolerant (always accepts up to 3.6 Volt max $V_{IH)}$, but voltage compliance (on outputs, V_{OH}) depends on the input V_{DDEXT}; because V_{OH} (max) ≈ V_{DDEXT} (max). This applies to Bidirectional pins (D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7) and Input Only pins (CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$).

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions	K/B Grades Min	K/B Grades Typ	K/B Grades Max	Unit
V_{IH}, Hi-Level Input Voltage[1, 2]	@ V_{DDINT} = max	1.5			V
V_{IH}, Hi-Level CLKIN Voltage	@ V_{DDINT} = max	2.0			V
V_{IL}, Lo-Level Input Voltage[1, 3]	@ V_{DDINT} = min			0.6	V
V_{OH}, Hi-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OH} = –0.5 mA	2.0			V
	@ V_{DDEXT} = 3.0 V, I_{OH} = –0.5 mA	2.4			V
	@ V_{DDEXT} = min, I_{OH} = –100 µA[6]	V_{DDEXT} – 0.3			V
V_{OL}, Lo-Level Output Voltage[1, 4, 5]	@ V_{DDEXT} = min, I_{OL} = 2 mA			0.4	V
I_{IH}, Hi-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 3.6 V			10	µA
I_{IL}, Lo-Level Input Current[3]	@ V_{DDINT} = max, V_{IN} = 0 V			10	µA
I_{OZH}, Three-State Leakage Current[7]	@ V_{DDINT} = max, V_{IN} = 3.6 V[8]			10	µA
I_{OZL}, Three-State Leakage Current[7]	@ V_{DDINT} = max, V_{IN} = 0 V[8]			10	µA
I_{DD}, Supply Current (Idle)[9]	@ V_{DDINT} = 2.5, t_{CK} = 15 ns		9		mA
I_{DD}, Supply Current (Idle)[9]	@ V_{DDINT} = 2.5, t_{CK} = 13.3 ns		10		mA
I_{DD}, Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.5, t_{CK} = 15 ns[11], T_{AMB} = +25°C		32		mA
I_{DD}, Supply Current (Dynamic)[10]	@ V_{DDINT} = 2.5, t_{CK} = 13.3 ns[11], T_{AMB} = +25°C		36		mA
I_{DD}, Supply Current (Power-Down)[12, 15]	Lowest Power Mode		150		µA
C_I, Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C			8	pF
C_O, Output Pin Capacitance[6, 7, 12, 14]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C			8	pF

NOTES

[1]Bidirectional pins: D0–D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, A1–A13, PF0–PF7.

[2]Input Only pins: $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[3]Input Only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{BR}}$, DR0, DR1, $\overline{\text{PWD}}$.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{PWDACK}}$, A0, DT0, DT1, CLKOUT, FL2-0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2189M outputs are CMOS-compatible and will drive to V_{DDEXT} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0–A13, D0-D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$, $\overline{\text{CMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, PF0–PF7.

[8]0 V on $\overline{\text{BR}}$.

[9]Idle refers to ADSP-2189M state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

[10]I_{DD} measurement taken with all instructions executing from internal memory. 50% of the instructions are multifunction (types 1, 4, 5, 12, 13, 14), 30% are type 2 and type 6, and 20% are idle instructions.

[11]V_{IN} = 0 V and 3 V. For typical figures for supply currents, refer to Power Dissipation section.

[12]See Chapter 9 of the *ADSP-2100 Family User's Manual*, Third Edition for details.

[13]Applies to LQFP package type.

[14]Output pin capacitance is the capacitive load for any three-stated output pin.

[15]V_{DDINT} = 2.5 V. T = 25°C.

Specifications subject to change without notice.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

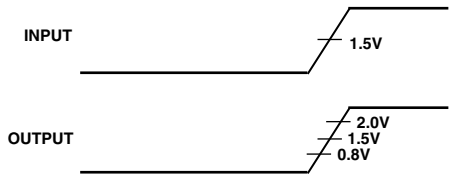


Figure 19. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

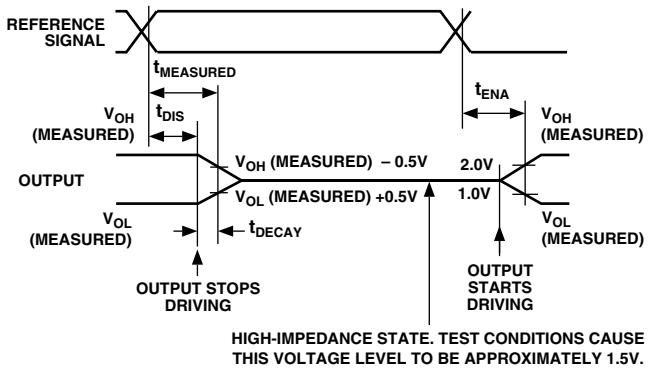


Figure 20. Output Enable/Disable

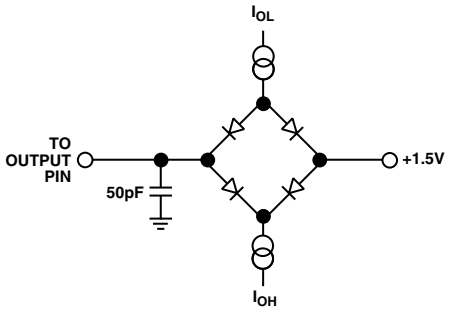


Figure 21. Equivalent Device Loading for AC Measurements (Including All Fixtures)

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals and Reset				
Timing Requirements:				
t_{CKI}	CLKIN Period	26.6	80	ns
t_{CKIL}	CLKIN Width Low	13		ns
t_{CKIH}	CLKIN Width High	13		ns
Switching Characteristics:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 2$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 2$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	13	ns
Control Signals				
Timing Requirements:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[1]		ns
t_{MS}	Mode Setup before $\overline{\text{RESET}}$ High	2		ns
t_{MH}	Mode Hold after $\overline{\text{RESET}}$ High	5		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

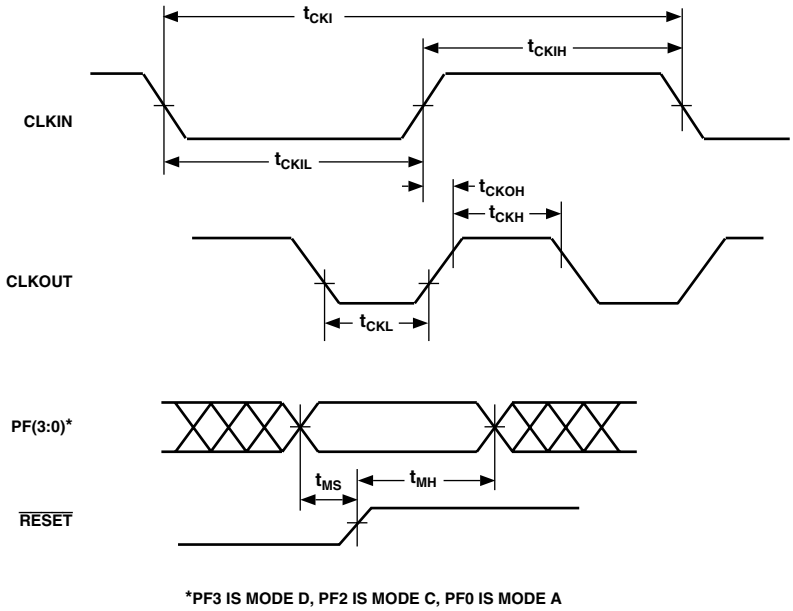


Figure 22. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirements:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low[1, 2, 3, 4]	$0.25t_{CK}$ + 10		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High[1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.5t_{CK}$ – 5		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]		$0.5t_{CK}$ + 4	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to Interrupt Controller Operation in the Program Control chapter of the *ADSP-2100 Family User's Manual*, Third Edition, for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulsewidths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQLE}$.
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7.
[5]Flag Outputs = PFx, FL0, FL1, FL2, Flag_out4.

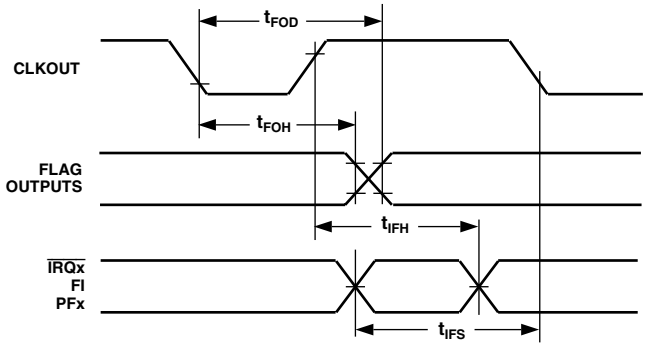


Figure 23. Interrupts and Flags

Parameter		Min	Max	Unit
Memory Read				
Timing Requirements:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 5 + w$	ns
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 6 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristics:				
t_{RP}	$\overline{RD}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{ASR}	A0–A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{RDA}	A0–A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

w = wait-states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

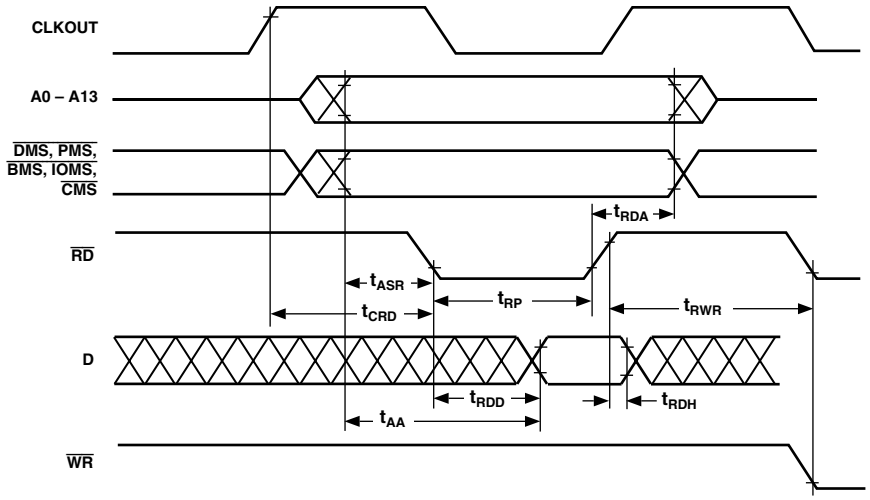


Figure 25. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristics:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 4 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 1$		ns
t_{WP}	$\overline{WR}$ Pulsewidth	$0.5t_{CK} - 3 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 3$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 3$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 2$	$0.25t_{CK} + 4$	ns
t_{AW}	A0–A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 5 + w$		ns
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 1$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 3$		ns

w = wait-states × t_{CK}.
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$.

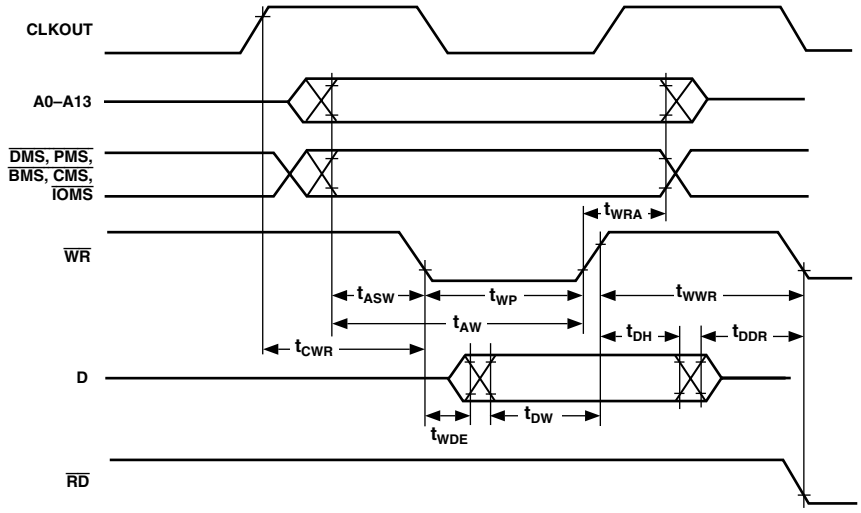


Figure 26. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirements:				
t_{SCK}	SCLK Period	26.67		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	SCLKIN Width	12		ns
Switching Characteristics:				
t_{CC}	CLKOUT High to SCLKOUT	$0.25t_{CK}$	$0.25t_{CK}$ + 6	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		12	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		12	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		12	ns
t_{SCDD}	SCLK High to DT Disable		12	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		12	ns

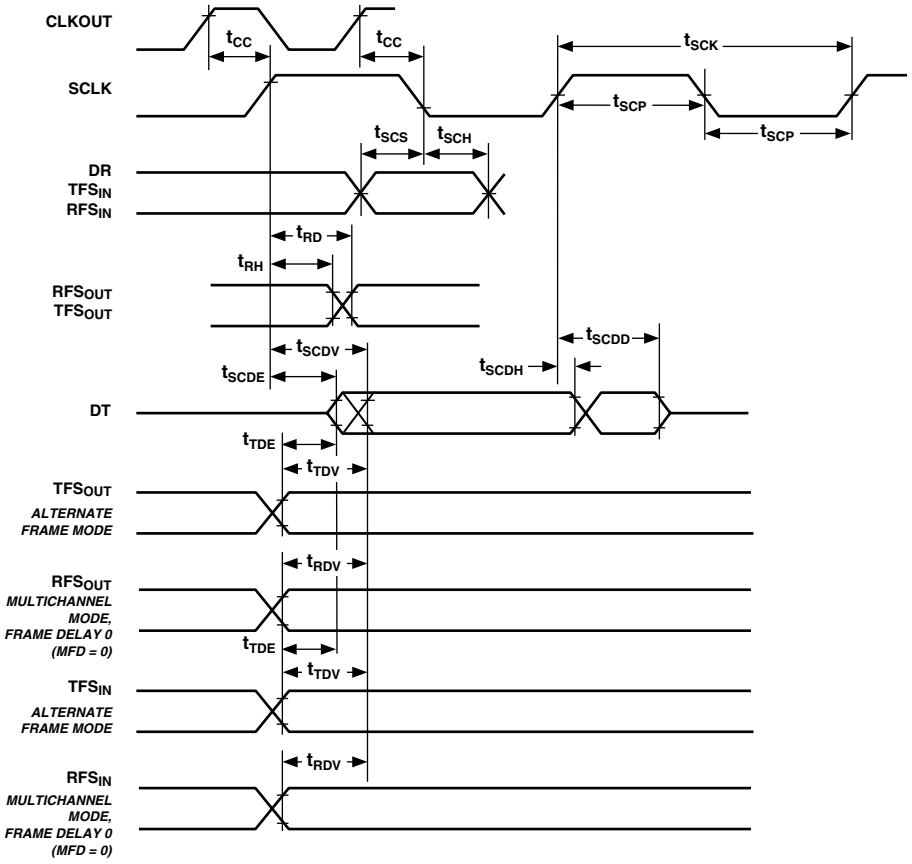


Figure 27. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirements:				
t_{IALP}	Duration of Address Latch[1, 2]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[2]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[2]	3		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[2, 3]	0		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	3		ns
t_{IALD}	Address Latch Start after Address Latch End[1, 2]	2		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and IAL High.
[2]End of Address Latch = $\overline{IS}$ High or IAL Low.
[3]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.

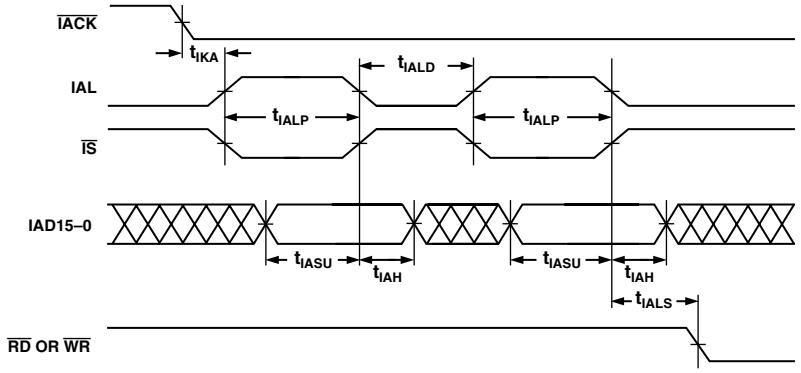


Figure 28. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirements:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	0		ns
t_{IKSU}	IAD15–0 Data Setup before End of Write[2, 3, 4]	$0.5t_{CK}$ + 5		ns
t_{IKH}	IAD15–0 Data Hold after End of Write[2, 3, 4]	0		ns
Switching Characteristics:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		10	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the *ADSP-2100 Family User's Manual*, Third Edition.

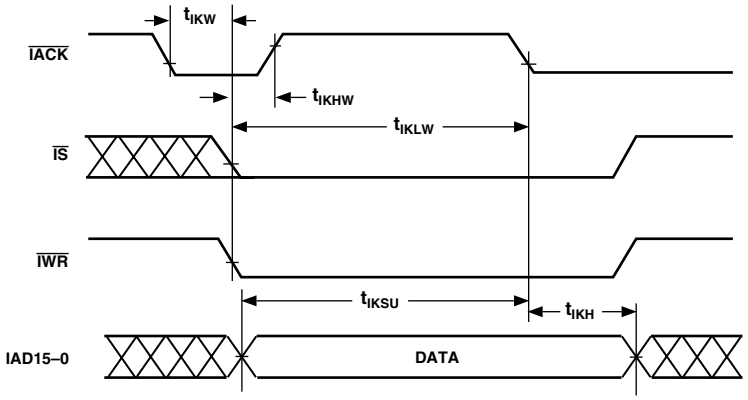


Figure 30. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read, Long Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRK}	End of Read after $\overline{IACK}$ Low[2]	2		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDS}	IAD15–0 Data Setup before $\overline{IACK}$ Low	$0.5t_{CK} - 2$		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		11	ns
t_{IRDH1}	IAD15–0 Previous Data Hold after Start of Read (DM/PM1)[3]	$2t_{CK} - 3$		ns
t_{IRDH2}	IAD15–0 Previous Data Hold after Start of Read (PM2)[4]	$t_{CK} - 5$		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.
[3]DM read or first half of PM read.
[4]Second half of PM read.

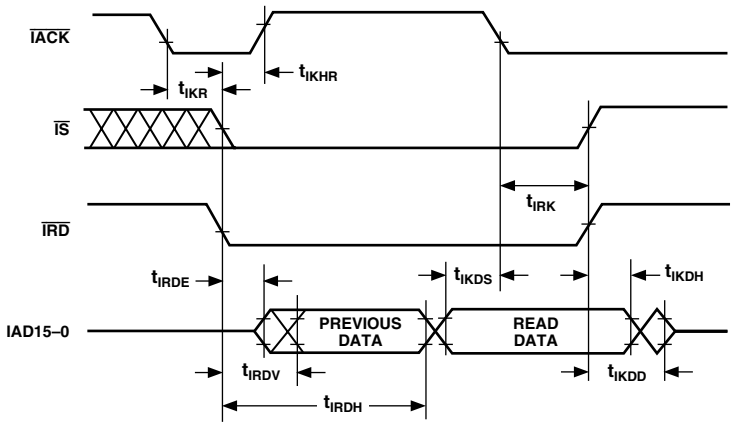


Figure 31. IDMA Read, Long Read Cycle

Parameter		Min	Max	Unit
IDMA Read, Short Read Cycle				
Timing Requirements:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	0		ns
t_{IRP}	Duration of Read	10		ns
Switching Characteristics:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		10	ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	0		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		10	ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

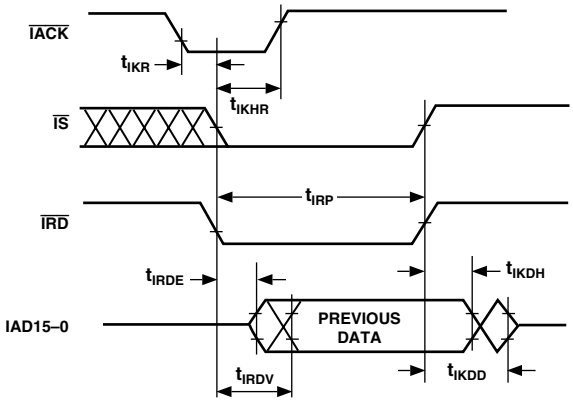
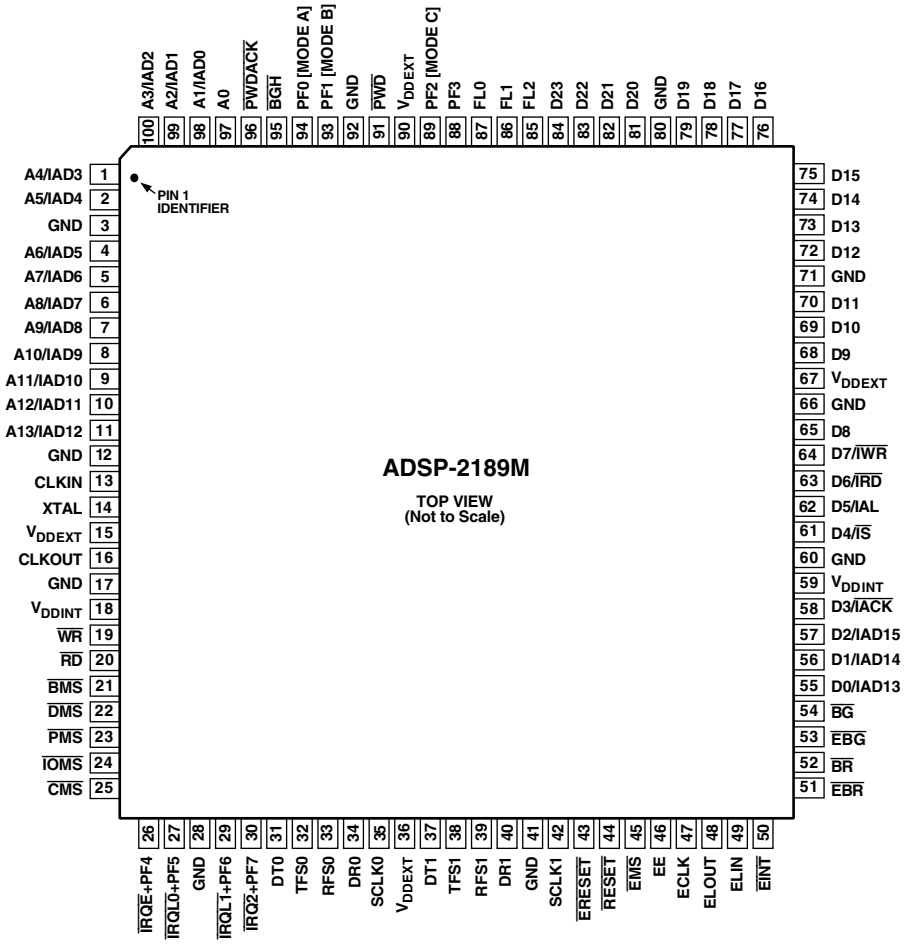


Figure 32. IDMA Read, Short Read Cycle

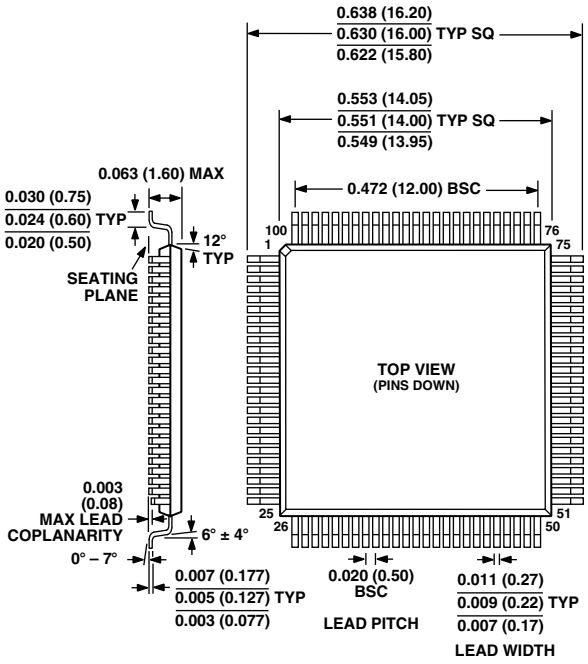
100-Lead LQFP Package Pinout



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

100-Lead Metric Thin Plastic Quad Flatpack (ST-100)



NOTE:
THE ACTUAL POSITION OF EACH LEAD IS WITHIN (0.08) 0.0032 FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate	Package Description*	Package Option
ADSP-2189MKST-300	0°C to +70°C	75 MHz	100-Lead LQFP	ST-100
ADSP-2189MBST-266	–40°C to +85°C	66 MHz	100-Lead LQFP	ST-100

*In 1998, JEDEC reevaluated the specifications for the TQFP package designation, assigning it to packages 1.0 mm thick. Previously labelled TQFP packages (1.6 mm thick) are now designated as LQFP.

C3605a–0–4/00 (rev. A)

PRINTED IN U.S.A.