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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	I²C, IDE, Memory Card, SPI, UART/USART
Peripherals	DMA, I²S, POR, Serial Audio, WDT
Number of I/O	34
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 4x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf5249lcag120

Paragraph Number | Page Number

SECTION 9
SYSTEM INTEGRATION MODULE

LIST OF FIGURES

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the ÷1 and ÷16 clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

1.6.16 IDE AND SMARTMEDIA INTERFACES

The MCF5249 system bus allows connection of an IDE hard disk drive and SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the MCF5249.

1.6.17 ANALOG/DIGITAL CONVERTER (ADC)

The four channel ADC is based on the Sigma-Delta concept with 12-bit resolution. The digital portion of the ADC is provided internally. The analog voltage comparator must be provided externally as well as an external integrator circuit (resistor/capacitor) which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

1.6.18 FLASH MEMORY CARD INTERFACE

The interface is Sony MemoryStick and SecureDigital compatible. However, there is no hardware support for MagicGate™.

1.6.19 I^2C MODULE

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

1.6.20 CHIP-SELECTS

There are four programmable chip selects on the MCF5249:

- Two programmable chip-select outputs (CS0 and CS1) provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions, and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.
- Two dedicated chip selects (CS2 and CS3) are used for the IDE and/or SmartMedia interface

CS0 is active after reset to provide boot-up from external FLASH/ROM.

1.6.21 GPIO INTERFACE

A total of 44 General Purpose inputs and 46 General Purpose outputs are available. These are multiplexed with various other signals. Eight of the GPIO inputs have edge sensitive interrupt capability.

1.6.22 INTERRUPT CONTROLLER

The MCF5249 has a primary and a secondary interrupt controller. These interrupt controllers handle interrupts from all internal interrupt sources. In addition, there are 8 GPIOs where external interrupts can

4.3 AUDIO CLOCK GENERATION

The audio clocks and output DAC clocks are divided directly from the crystal. Clock settings depend on CRSEL, CLSEL, and AUDIOSEL bits, as explained in Table 4-4. As the table shows, the AUDIOCLK is completely derived from the AUDIOSEL bit, and this clock is independent of the other select bits. For the DAC clocks (MCLK2 and MCLK1) the relationship between CRSEL and CLSEL is defined in Table 4-4.

Table 4-4 PLLCR Bit Fields

PLLCR CLSEL (BITS30-28)	PLLCR CRSEL (BIT 23)	PLLCR CONFIG AUDIOSEL (BIT 22)	AUDIOCLK	MCLK2	MCLK1
000	1	1	FXTAL	FXTAL	FXTAL/2
001	1	1	FXTAL	FXTAL	FXTAL
010	1	1	FXTAL	FXTAL/2	FXTAL/2
011	1	1	FXTAL	FXTAL/2	FXTAL
100	1	1	FXTAL	FXTAL	FXTAL/2
101	1	1	FXTAL	FXTAL	FXTAL
110	1	1	FXTAL	FXTAL/2	FXTAL/2
111	1	1	FXTAL	FXTAL/2	FXTAL
000	1	0	FXTAL/2	FXTAL	FXTAL/2
001	1	0	FXTAL/2	FXTAL	FXTAL
010	1	0	FXTAL/2	FXTAL/2	FXTAL/2
011	1	0	FXTAL/2	FXTAL/2	FXTAL
100	1	0	FXTAL/2	FXTAL	FXTAL/2
101	1	0	FXTAL/2	FXTAL	FXTAL
110	1	0	FXTAL/2	FXTAL/2	FXTAL/2
111	1	0	FXTAL/2	FXTAL/2	FXTAL

Note: MCLK1 and MCLK2 will output a clock signal just after reset and before they can be configured as GPIO if so desired. The frequency of the clock will be the same as CRIN prior to initialization of the PLL.

The multiplexer that switches AUDIOCLK between Fxtal and Fxtal/2 is glitch free. No reset is needed after switching audio clock. For the MCLK1 and MCLK2 clocks, the divide by 2 is 50% duty cycle, divide by 3 is 33% duty cycle, and divide by 4 is 25% duty cycle.

Table 7-1 DRAM Controller Registers

MBAR OFFSET	[31:24]	[23:16]	[15:8]	[7:0]
0x100	DRAM control register (DCR) [See Section 7.2.1]		Reserved	
0x104	Reserved			
0x108	DRAM address and control register 0 (DACR0) [See Section 7.3.2.2.]			
0x10C	DRAM mask register block 0 (DMR0) [See Section 7.3.2.3.]			
0x110	DRAM address and control register 1 (DACR1) [See Section 7.3.2.2.]			
0x114	DRAM mask register block 1 (DMR1) [See Section 7.3.2.3.]			

7.3 SYNCHRONOUS OPERATION

By running synchronously with the system clock, SDRAM can (after an initial latency period) be accessed on every clock; 5-1-1-1 is a typical MCF5249 burst rate to SDRAM.

Note: Because the MCF5249 cannot have more than one page open at a time, it does not support interleaving.

Table 7-2 lists common SDRAM commands.

Table 7-2 SDRAM Commands

COMMAND	DEFINITION
ACTV	Activate. Executed before READ or WRITE executes; SDRAM registers and decodes row address.
MRS	Mode register set.
NOP	No-op. Does not affect SDRAM state machine; DRAM controller control signals negated; SDRAM_CS asserted.
PALL	Precharge all. Precharges all internal banks of an SDRAM component; executed before new page is opened.
READ	Read access. SDRAM registers column address and decodes that a read access is occurring.
REF	Refresh. Refreshes internal bank rows of an SDRAM component.
SELF	Self refresh. Refreshes internal bank rows of an SDRAM component when it is in low-power mode.
SELFX	Exit self refresh. This command is sent to the DRAM controller when DCR[IS] is cleared.
WRITE	Write access. SDRAM registers column address and decodes that a write access is occurring.

Commands are issued to memory using specific encoding on address and control pins. Soon after system reset, a command must be sent to the SDRAM mode register to configure SDRAM operating parameters.

Table 7-18 DACR Initialization Values (Continued)

BITS	NAME	SETTING	DESCRIPTION
3	IP	0	Indicates precharge has not been initiated.
2	PM	1	Indicates continuous page mode
1–0	—		Reserved. Don't care.

7.4.4 DMR INITIALIZATION

In this example, again, only the second 512-Kbyte block of each 1-Mbyte space is accessed in each bank. In addition the SDRAM component is mapped only to readable and writable supervisor and user data. The DMRs have the following configuration.

	31														18	17	16
Field	BAM															—	
Setting	0	0	0	0	0	0	0	0	0	1	1	1	0	1		X	X
(hex)	0				0				7				4				

	15						9	8	7	6	5	4	3	2	1	0
Field	—							WP	—	C/I	AM	SC	SD	UC	UD	V
Setting	X	X	X	X	X	X	X	0	X	1	1	1	0	1	0	1
(hex)	0				0				7				5			

Figure 7-16 DMR0 Register

With this configuration, the DMR0 = 0x0074_0075, as described in Table 7-19.

Table 7-19 DMR0 Initialization Values

BITS	NAME	SETTING	DESCRIPTION
31–16	BAM		With bits 17 and 16 as don't cares, BAM = 0x0074, which leaves bank select bits and upper 512K select bits unmasked. Bits 22 and 21 are set because they are used as bank selects; bit 20 is set because it controls the 1-Mbyte boundary address.
15–9	—		Reserved. Don't care.
8	WP	0	Allow reads and writes
7	—		Reserved
6	C/I	1	Disable CPU space access
5	AM	1	Disable alternate master access
4	SC	1	Disable supervisor code accesses
3	SD	0	Enable supervisor data accesses
2	UC	1	Disable user code accesses
1	UD	0	Enable user data accesses
0	V	1	Enable accesses.

Table 8-6 Write Cycle States (Continued)

STATE NAME	DESCRIPTION
STATE 3	During state 3 (S3), the MCF5249 waits for a cycle termination signal ($\overline{TA}$). If $\overline{TA}$ is not asserted before the rising edge of BCLK at the end of the first clock cycle, the MCF5249 inserts wait states (full clock cycles) until $\overline{TA}$ is asserted. $\overline{TA}$ is generated internally by the chip select module. If internal $\overline{TA}$ is requested (auto-acknowledge enabled in the chip select control register, CSCR) then $\overline{TA}$ is generated internally by the chip select module.
STATE 4	During state 4, $\overline{TA}$ should be negated by the external device or if auto-acknowledge is enabled, negated internally by the chip select module.
STATE 5	$\overline{CS}$ is negated on the falling edge of BCLK in state 5 (S5). The MCF5249 stops driving the address lines and R/$\overline{W}$, terminating the write cycle. The data bus returns to high impedance on the rising edge of BCLK. The rising edge of BCLK may be the start of state 0 for the next access cycle.

8.5.4 BACK-TO-BACK BUS CYCLES

The MCF5249 can accommodate back-to-back bus cycles. The processor runs back-to-back bus cycles whenever possible. For example, when a longword read is started on a word-size bus, and burst read enable is disabled into the relevant chip select register, the processor will perform two word reads back to back. Figure 7-9 shows a read, followed by a write that occurs back to back.

A basic read and a write cycle are used to illustrate the back-to-back cycle. There is no restriction as to the type of operation to be placed back to back. The initiation of a back-to-back cycle is not user definable.

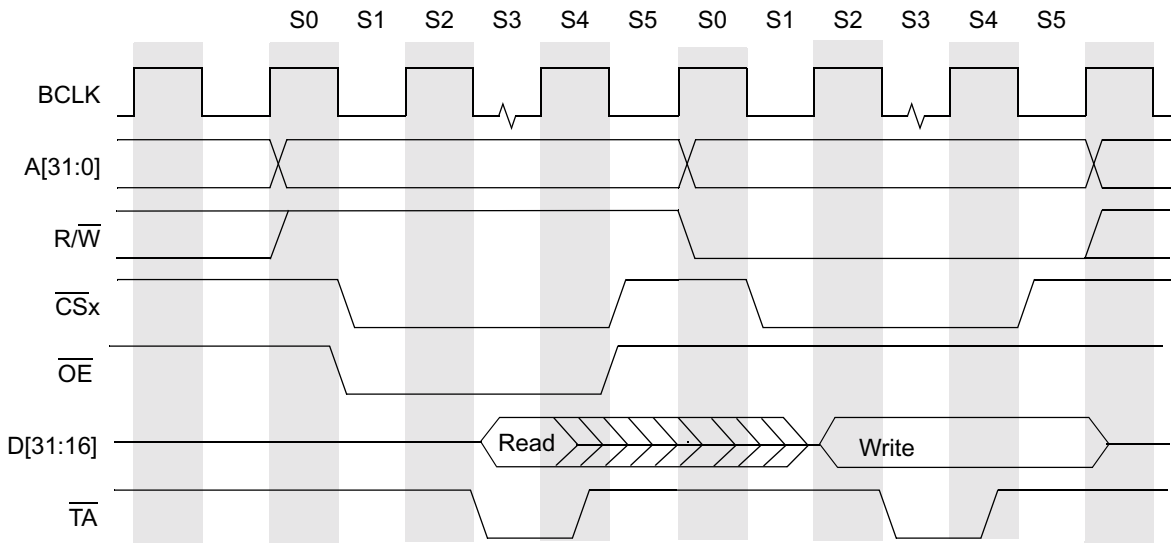

Figure 8-7 Back-to-Back Bus Cycles

Table 9-1 MBAR Register Addresses

ADDRESS	NAME	SIZE (BYTES)	DESCRIPTION
CPU + $C0F	MBAR	4	Module base address register
CPU + $C0E	MBAR2	4	Module base address register 2

Table 9-2 SIM Memory Map

ADDRESS	DESCRIPTION	0	1	2	3
MBAR + $000	SYSTEM CONTROL REG	RSR	SYPCR	SWIVR	SWSR
MBAR + $004		Reserved			
MBAR + $008		Reserved			
MBAR + $00C	BUS MASTER CONTROL REG	MPARK	Reserved		
MBAR + $010	—	Reserved			
MBAR + $014	—				
MBAR + $018	—				
MBAR + $01C	—				
MBAR + $020	—				
MBAR + $024	—				
MBAR + $028	—				
MBAR + $02C	—				
MBAR + $030	—				
MBAR + $034	—				
MBAR + $038	—				
MBAR + $03C	—				
MBAR + $040	Primary interrupt Pending Reg	IPR			
MBAR + $044	Primary Interrupt Mask Reg	IMR			
MBAR + $04C	Primary Interrupt Control Reg	ICR0	ICR1	ICR2	ICR3
MBAR + $050	Primary Interrupt Control Reg	ICR4	ICR5	ICR6	ICR7
MBAR + $054	Primary Interrupt Control Reg	ICR8	ICR9	ICR10	ICR11
MBAR2 + $000	gpio 0-31 input reg	GPIO-READ (READ ONLY)			
MBAR2 + $004	gpio 0-31 output reg	GPIO-OUT			
MBAR2 + $008	gpio 0-31 output enable reg	GPIO-ENABLE			
MBAR2 + $00C	gpio 0-31 function select	GPIO-FUNCTION			
MBAR + $0AC	Device ID Reg				
MBAR2 + $0B0	gpio 32-63 input reg	GPIO1-READ (READ ONLY)			
MBAR2 + $0B4	gpio 32-63 output reg	GPIO1-OUT			

Table 9-4 Module Base Address Bit Descriptions (Continued)

BIT NAME	DESCRIPTION
V	This bit defines when the base address is valid: 0 = MBAR address space not visible by CPU 1 = MBAR address space visible by CPU

The following example shows how to set the MBAR to location $10000000 using the D0 register. A “1” in the least significant bit validates the MBAR location. This example assumes that all accesses are valid:

```
move.1 #$10000001,DO
movec DO,MBAR
```

Table 9-5 Second Module Base Address Register (MBAR2)

BITS	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIELD	BA31	BA30	-	-	-	-	-	-	-	-	-	-	-	-	-	-
RESET	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	R/W	R/W														
BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD									LS7	LS6	LS5	LS4	LS3	LS2	LS1	V
RESET	-	-	-	-	-	-	-	-	0	0	0	0	0	0	0	0
R/W									R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 9-6 Second Module Base Address Bit Descriptions

BIT NAME	DESCRIPTION
BA[31:30]	The Base Address field defines the base address for a 1024-MByte address range. If V-bit in MBAR2 is set, address range Base Address to BaseAddress + $3FFF FFFF are mapped to MBAR2 space, and cannot be used for MBAR, SDRAM or Chip Select.
LS[7:1]	If interrupts both “primary” and the “secondary” interrupt controller have interrupt level 7 pending, bit LS7 determines which interrupt controller gets priority. If this bit is cleared, the primary interrupt controller gets priority. If this bit is set, the secondary interrupt controller gets priority. There are 7 LSn bits, one for each interrupt level.
V	The Valid bit defines if the CPU can access the MBAR2 mapped peripherals 0 = MBAR2 address space not visible by CPU. 1 = MBAR2 address space visible by CPU

9.3.2 DEVICE ID

The DeviceID register is a read only register that allows the software to determine which hardware it is running on. The register contains the part number in the upper 24 bits, the mask revision number in the lower 8 bits, and is read as 0x005448rr, where *rr* is the revision number.

This register allows developers the flexibility to write code to run on more than one device. The revision number allows developers to distinguish between different mask versions that may have minor changes or

Section 14
DMA Controller Module

The direct memory access (DMA) controller module quickly and efficiently moves blocks of data with minimal processor overhead. The DMA module, shown in Figure 14-1, provides four channels that allow byte, word, or longword operand transfers. These transfers should be dual address to on-chip devices; such as the UART, SDRAM controller, and audio module.

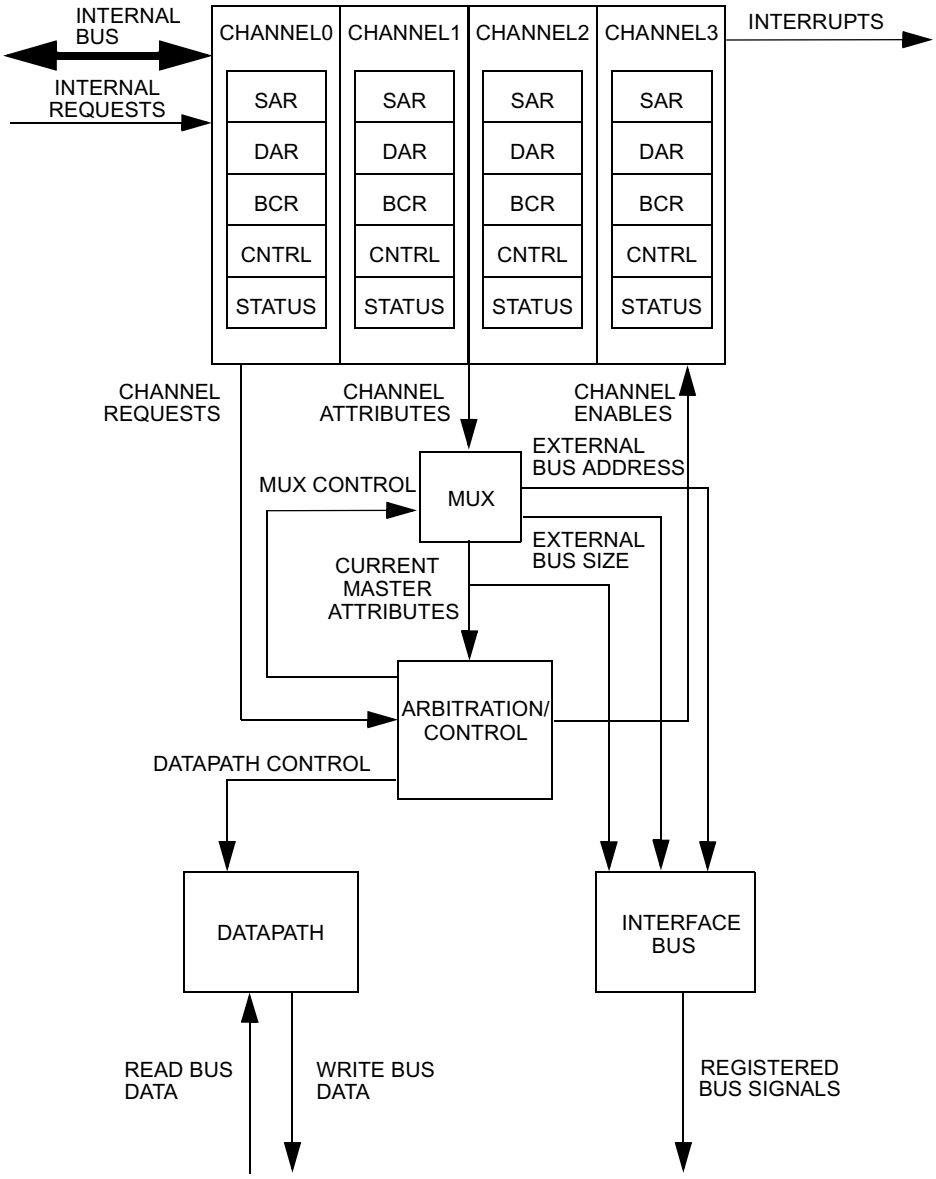

Figure 14-1 DMA Signal Diagram

Table 14-2 Memory Map DMA Channel 0

DMA CHANNEL	ADDRESS	[31:24]	[23:16]	[15:8]	[7:0]
	MBAR2+$188	DMAROUTE - Request source control			
Channel 0	MBAR+$300	Source Address Register 0			
	MBAR+$304	Destination Address Register 0			
	MBAR+$308	DMA Control Register 0			
	MBAR+$30C	Byte Count Register 0		Reserved	
	MBAR+$310	Status Register 0	Reserved		
	MBAR+$314	Interrupt Vector Register 0	Reserved		

Table 14-3 Memory Map DMA Channel 1

DMA CHANNEL	ADDRESS	[31:24]	[23:16]	[15:8]	[7:0]
Channel 1	MBAR+$340	Source Address Register 1			
	MBAR+$344	Destination Address Register 1			
	MBAR+$348	DMA Control Register 1			
	MBAR+$34C	Byte Count Register 1		Reserved	
	MBAR+$350	Status Register 1	Reserved		
	MBAR+$354	Interrupt Vector Register 1	Reserved		

Table 14-4 Memory Map DMA Channel 2

DMA CHANNEL	ADDRESS	[31:24]	[23:16]	[15:8]	[7:0]
Channel 2	MBAR+$380	Source Address Register 2			
	MBAR+$384	Destination Address Register 2			
	MBAR+$388	DMA Control Register 2			
	MBAR+$38C	Byte Count Register 2		Reserved	
	MBAR+$390	Status Register 2	Reserved		
	MBAR+$394	Interrupt Vector Register 2	Reserved		

Table 14-5 Memory Map DMA Channel 3

DMA CHANNEL	ADDRESS	[31:24]	[23:16]	[15:8]	[7:0]
Channel 3	MBAR+$3C0	Source Address Register 3			
	MBAR+$3C4	Destination Address Register 3			
	MBAR+$3C8	DMA Control Register 3			
	MBAR+$3CC	Byte Count Register 3		Reserved	
	MBAR+$3D0	Status Register 3	Reserved		
	MBAR+$3D4	Interrupt Vector Register 3	Reserved		

Note: Table 14-2 is for BCR24BIT = 0. Table 14-6 shows the difference in the memory map when BCR24BIT = 1.

15.3.3.3 Remote Loopback Mode

In this mode, the channel automatically transmits received data on the TxD output on a bit-by-bit basis. The local CPU-to-transmitter link is disabled. This mode is useful for testing remote channel receiver and transmitter operation. While in this mode, the receiver clocks the transmitter.

Note: Because the receiver is not active, the CPU cannot read received data. All status conditions are inactive. Received parity is not checked and is not recalculated for transmission. Stop bits are transmitted as received. A received break is echoed as received until the next valid start bit is detected.

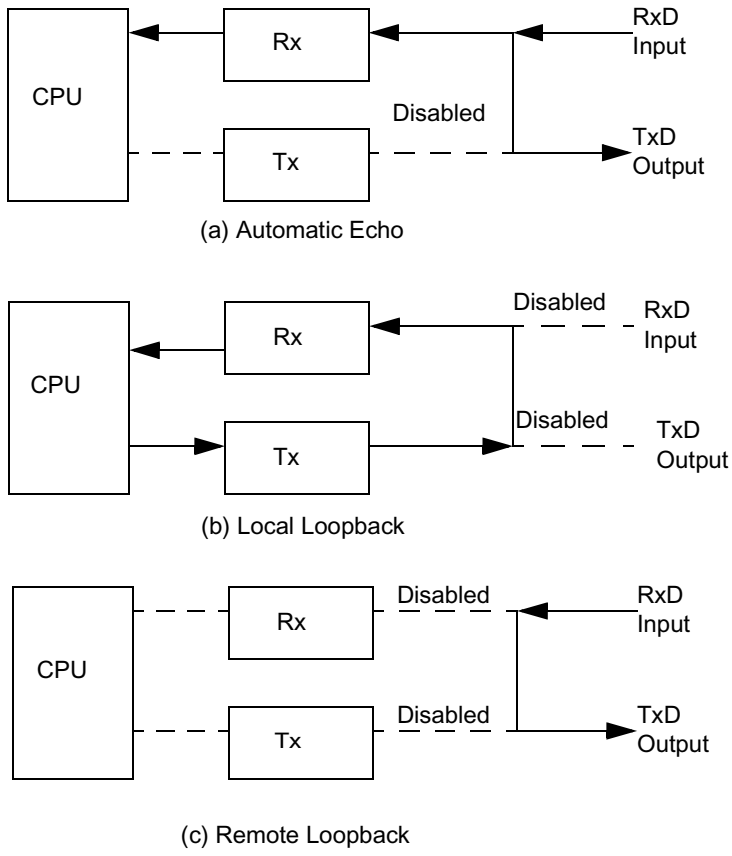

Figure 15-7 Looping Modes Functional Diagram

15.3.4 MULTIDROP MODE

The UART can be programmed to operate in a wakeup mode for multidrop or multiprocessor applications. Functional timing information for the multidrop mode is shown in Figure 15-8. The mode is selected by setting bits 3 and 4 in UART mode register 1 (UMR1). This mode of operation connects the master station to several slave stations (maximum of 256). In this mode, the master transmits an address character followed by a block of data characters targeted for one of the slave stations. The slave stations channel receivers are disabled; however, they continuously monitor the data stream sent out by the master station. When the master sends an address character, the slave receiver channel notifies its respective CPU by setting the RxRDY bit in the USR and generating an interrupt (if programmed to do so). Each slave station CPU then compares the received address to its station address and enables its receiver if it wants to

	15 … 6	5 … 0
Field	—	ADDR
Reset	0000_0000_0000_0000	
R/W	R/W	
Address	MBAR + 0 x 410	

Figure 16-8 QSPI Address Register (QAR)

Note: All QSPI registers must be accessed as 16-bits only.

16.5.6 QSPI DATA REGISTER (QDR)

The QDR, shown in Figure 16-9, is used to access QSPI RAM indirectly. The CPU reads and writes all data from and to the QSPI RAM through this register.

	15 … 0
Field	DATA
Reset	0000_0000_0000_0000
R/W	R/W
Address	MBAR + 0 x 414

Figure 16-9 QSPI Data Register (QDR)

Note: All QSPI registers must be accessed as 16-bits only.

16.5.7 COMMAND RAM REGISTERS (QCR0–QCR15)

The command RAM is accessed using the upper byte of QDR. The QSPI cannot modify information in command RAM.

There are 16 bytes in the command RAM. Each byte is divided into two fields. The chip select field enables external peripherals for transfer. The command field provides transfer operations.

Note: The command RAM is accessed only using the most significant byte of QDR and indirect addressing based on QAR[ADDR].

Figure 16-10 shows the command RAM register.

Section 19
Debug Support

This section details the MCF5249 hardware debug support. The MCF5249 implements an enhanced debug architecture. The original design plus these enhancements is known as Revision A (or Rev. A). The enhanced functionality is clearly identified in this section. The Rev. A enhancements are backward compatible with the original ColdFire debug definition.

The general topic of debug support is divided into three separate areas:

1. Real-Time Trace Support
2. Background Debug Mode (BDM)
3. Real-Time Debug Support

Note: To enable Debug Mode, MTMOD[3:0] pins must be = 0001.

The logic required to support these three areas is contained in a debug module as shown in Figure 19-1.

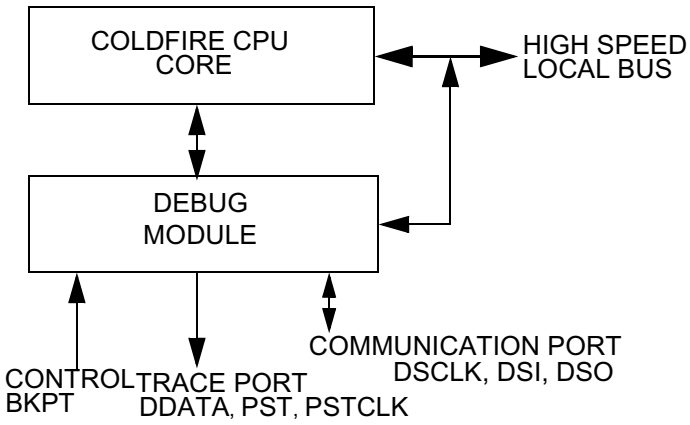

Figure 19-1 Processor/Debug Module Interface

19.1 BREAKPOINT ($\overline{\text{BKPT}}$)

This section describes signals associated with the debug module. All ColdFire debug signals are unidirectional and are related to the rising-edge of the processor core's clock signal.

19.1.1 DEBUG SUPPORT SIGNALS

The $\overline{\text{BKPT}}$ active-low input signal is used to request a manual breakpoint. Its assertion causes the processor to enter a halted state after the completion of the current instruction. The halt status is reflected on the processor status (PST) pins as the value $F.

19.1.2 DEBUG DATA (DDATA[3:0])

These output signals display the hardware register breakpoint status as a default, or optionally, captured address and operand values. The capturing of data values is controlled by the setting of the

Table 19-28 Data Breakpoint Register (DBR)

BITS	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIELD	ADDRESS [31:0]															
RESET	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	WRITE ONLY															
ADDR																
BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	ADDRESS [31:0]															
RESET	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	WRITE ONLY															

DATA[31:0]–Data Breakpoint Value

This field contains the 32-bit value to be compared with the data value from the processor's local bus as a breakpoint trigger.

Table 19-29 Data Breakpoint Mask Register (DBMR)

BITS	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIELD	MASK [31:0]															
RESET	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	WRITE ONLY															
BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	MASK [31:0]															
RESET	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W	WRITE ONLY															

MASK[31:0]–Data Breakpoint Mask

This field contains the 32-bit mask for the data breakpoint trigger. A zero in a bit position causes the corresponding bit in the DBR to be compared to the appropriate bit of the internal data bus. A one causes that bit to be ignored

The data breakpoint register supports both aligned and misaligned references. The relationship between the processor address, the access size, and the corresponding location within the 32-bit data bus is shown in Table 19-30.

.

Table 19-36 BDM Address Attribute (BAAR) Bit Descriptions

BIT NAME	DESCRIPTION
R[7]	0 = Write 1 = Read
SZ[6:5]	Size 00 = Longword 01 = Byte 10 = Word 11 = Reserved
TT[4:3]	Transfer Type See the TT definition in the AATR description, Section 19.4.2.2 Address Attribute Trigger Register.
TM[2:0]	Transfer Modifier See the TM definition in the AATR description, Section 19.4.2.2 Address Attribute Trigger Register.

19.4.3 CONCURRENT BDM AND PROCESSOR OPERATION

The debug module supports concurrent operation of both the processor and most BDM commands. BDM commands may be executed while the processor is running, except for the operations that access processor/memory registers:

- Read/Write Address and Data Registers
- Read/Write Control Registers

For BDM commands that access memory, the debug module requests the processor's local bus. The processor responds by stalling the instruction fetch pipeline and then waiting until all current bus activity is complete. At that time, the processor relinquishes the local bus to allow the debug module to perform the required operation. After the conclusion of the debug module bus cycle, the processor reclaims ownership of the bus.

The development system must use caution in configuring the breakpoint registers if the processor is executing. The debug module does not contain any hardware interlocks, so Motorola recommends that the TDR be disabled while the breakpoint registers are being loaded. At the conclusion of this process, the TDR can be written to define the exact trigger. This approach guarantees that no spurious breakpoint triggers occur.

Because there are no hardware interlocks in the debug unit, no BDM operations are allowed while the CPU is writing the debug's registers ($\overline{\text{BKPT}}$ and DSCLK must be inactive).

20.4 JTAG REGISTERS

20.4.1 JTAG INSTRUCTION SHIFT REGISTER

The MCF5249 IEEE 1149.1A Standard implementation uses a 4-bit instruction-shift register without parity. This register transfers its value to a parallel hold register and applies one of eight possible instructions on the falling edge of TCK when the TAP state machine is in the update-IR state. To load the instructions into the shift portion of the register, place the serial data on the TDI pin prior to each rising edge of TCK. The MSB of the instruction shift register is the bit closest to the TDI pin and the LSB is the bit closest to the TDO pin.

Table 20-2 lists the public, usable instructions that are supported along with their encoding.

Table 20-2 JTAG Instructions

INSTRUCTION	ABBR	CLASS	IR[3:0]	INSTRUCTION SUMMARY
EXTEST	EXT	Required	0000	Select BS register while applying fixed values to output pins and asserting functional reset
IDCODE	IDC	Optional	0001	Selects IDCODE register for shift
SAMPLE/ PRELOAD	SMP	Required	0010	Selects BS register for shift, sample, and preload without disturbing functional operation
CLAMP	CMP	Optional	0011	Selects bypass while applying fixed values to output pins and asserting functional reset
HIGHZ	HIZ	Optional	0100	Selects the bypass register while three-stating all output pins and asserting functional reset
RINGOSC	RING	Optional	0111	User defined function for device test
ORGATE	OR	Optional	1000	User defined function for device test
BYPASS	BYP	Required	1111	Selects the bypass register for data operations

The IEEE 1149.1A Standard requires the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. IDCODE, CLAMP, HIGHZ are optional standard instructions that the MCF5249 implementation supports and are described in the IEEE Standard 1149.1. The RINGOSC and ORGATE are user defined instructions only used for device test during manufacturing.

20.4.1.1 EXTEST Instruction

The external test instruction (EXTEST) selects the boundary-scan register. The EXTEST instruction forces all output pins and bidirectional pins configured as outputs to the preloaded fixed values (with the SAMPLE/PRELOAD instruction) and held in the boundary-scan update registers. The EXTEST instruction can also configure the direction of bidirectional pins and establish high-impedance states on some pins. The EXTEST instruction becomes active on the falling edge of TCK in the update-IR state when the data held in the instruction-shift register is equivalent to hex 0.

20.4.1.2 IDCODE

The IDCODE instruction selects the 32-bit IDcode register for connection as a shift path between the TDI pin and the TDO pin. This instruction lets users interrogate the MCF5249 to determine its version number

Table 21-5 Clock Timing Specification

NUM	CHARACTERISTIC	MIN	MAX	UNITS
	CRIN Frequency[1]	11.29	33.86	MHz
C5	PSTCLK cycle time	7.1	—	nSec
C6	PSTCLK duty cycle	40	60	%
C7	SCLK cycle time	14.2	—	nSec
C8	SCLK duty cycle	45	55	%

[1] There are only three choices for the valid Audio frequencies 11.29 MHz, 16.93 MHz, or 33.86 MHz; no other values are allowed. The System Clock is derived from one of these crystals via an internal PLL.

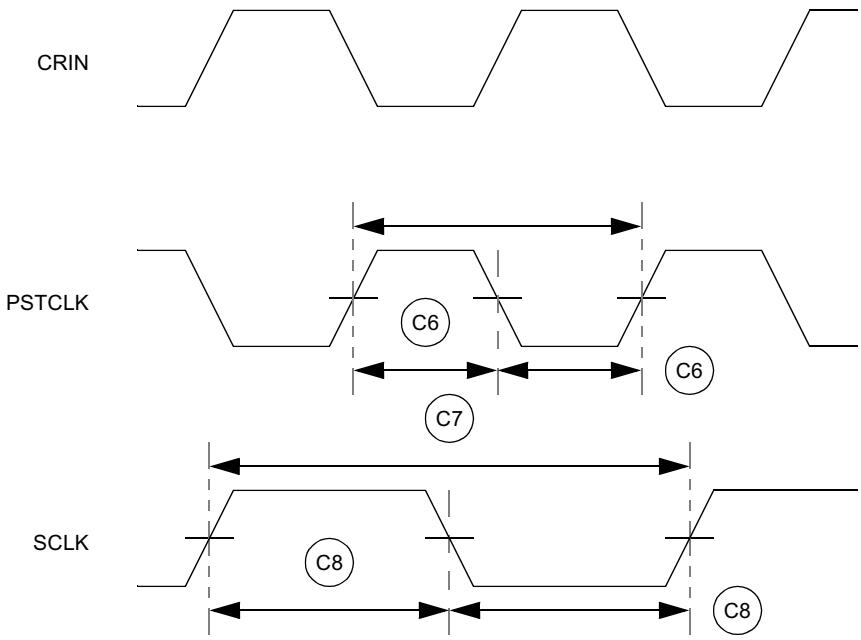

Figure 21-4 Clock Timing Definition

Note: Signals above are shown in relation to the clock. No relationship between signals is implied or intended.

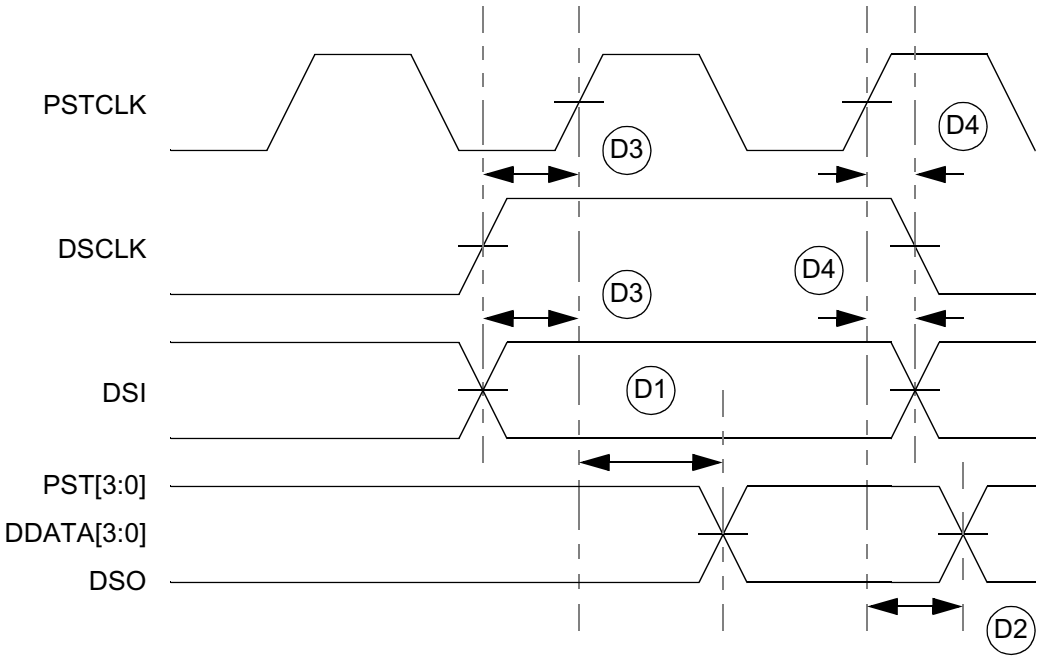

Figure 21-9 Debug Timing Definition

Table 21-10 Timer Module AC Timing Specification

NUM	CHARACTERISTIC	MIN	MAX	UNITS
T1	TIN Cycle time	tbd	—	bus clocks
T2	TIN Valid to SCLK (input setup)	tbd	—	nSec
T3	SCLK to TIN Invalid (input hold)	tbd	—	nSec
T4	SCLK to TOUT Valid (output valid)	—	tbd	nSec
T5	SCLK to TOUT Invalid (output hold)	tbd	—	nSec
T6	TIN Pulse Width	tbd	—	bus clocks
T7	TOUT Pulse Width	tbd	—	bus clocks

Table 22-3 160 MAPBGA Pin Assignments

PIN BGA	NAME	TYPE	DESCRIPTION
L2	A15	o	SDRAM address / static adr
M1	A16	o	SDRAM address / static adr
L3	PAD-VDD		PAD-VDD
L3	PAD-VDD		PAD-VDD
M2	A19	o	SDRAM address / static adr
N1	A20	o	SDRAM address / static adr
L4	QSPI_CS1/GPIO24	io	QSPI select 1
M3	TEST2	i	Structural test
N2	SDRAM_CS1	o	SDRAM chip select out 1
M4	SDATA1_BS1/GPIO9	i/o	MemoryStick/SD
P1	SDRAS	o	SDRAM RAS
P2	SDCAS	o	SDRAM CAS
N3	SDWE	o	SDRAM write enable
P3	SDLDQM	o	SDRAM LDQM
N4	GPIO5	i/o	general purpose i/o
P4	QSPI_CS0/GPIO29	i/o	QSPI chip select 0
N5	QSPI_DOUT/GPIO26	i/o	Qspsi data out
L5	GPIO6	i/o	general purpose i/o
P5	DATA21	i/o	data bus bit 21
N6	DATA19	i/o	data bus bit 19
L6	QSPI_CS2/GPIO21	i/o	QSPI chip select 2
P6	DATA20	i/o	data bus bit 20
L7	DATA22	i/o	data bus bit 22
P7	DATA18	i/o	data bus bit 18
K7	DATA23	i/o	data bus bit 23
N7	DATA17	i/o	data bus bit 17
L8	QSPI_CS3/GPIO22	io	QSPI Chip Select 3
K8	PAD-VDD		PAD-VDD
K8	PAD-VDD		PAD-VDD
P8	DATA16	i/o	data bus bit 16
N8	SDRAM_CS2 / GPIO7	i/o	SDRAM chip select out 2 gpo
P9	EBUOUT2 / GPO 37	o	audio interfaces EBU out 2
L9	CFLG/GPIO18	io	CFLG input
N9	EBUOUT1 / GPO 36	o	audio interfaces EBU out 1
K9	CORE-GND		CORE-GND
K9	CORE-GND		CORE-GND
P10	EBUIN3 / ADIN0/GPI 38	i	audio interfaces EBU in 3 A/D convertor input 0
N10	EBUIN2 / GPI 37	i	audio interfaces EBU in 2