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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1.25K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 32x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051f206-gq |

## NOTES:

## NOTES:

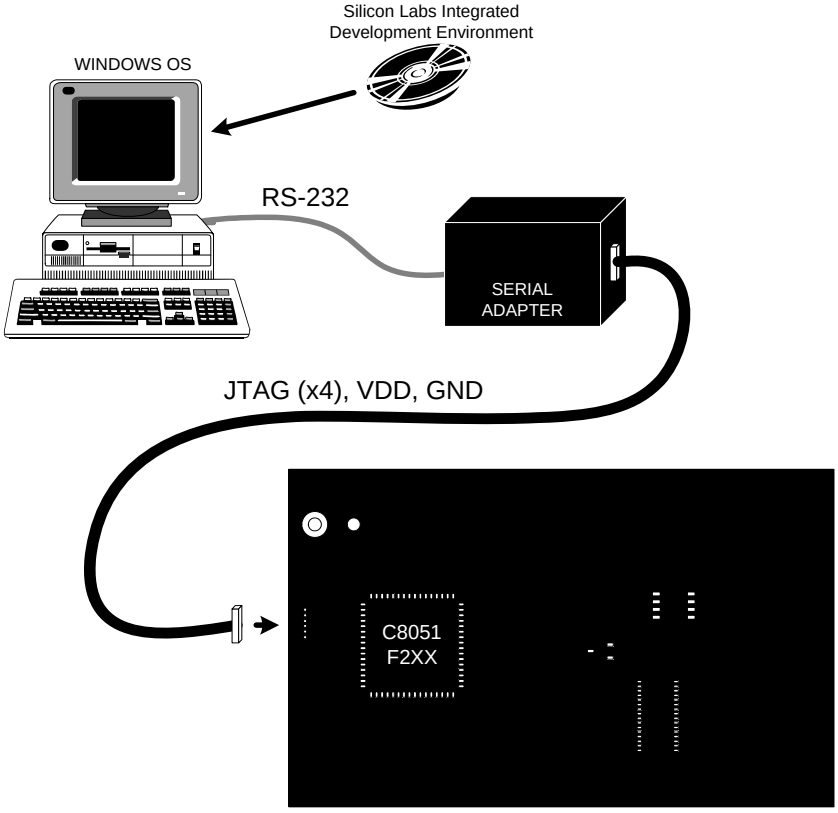


**Figure 1.8. Degub Environment Diagram**

## 1.4. Digital/Analog Configurable I/O

The standard 8051 Ports (0, 1, 2, and 3) are available on the device. The ports behave like standard 8051 ports with a few enhancements.

Each port pin can be configured as either a push-pull or open-drain output. Any input that is configured as an analog input will have its corresponding weak pull-up turned off.

Digital resources (timers, SPI, UART, system clock, and comparators) are routed to corresponding I/O pins by configuring the port multiplexer. Port multiplexers are programmed by setting bits in SFR's (please see Section 14). Any of the 32 external port pins may be configured as either analog inputs or digital I/O (See Figure 1.9), so effectively, all port pins are dual function.

## Table 5.1. 8-Bit ADC Electrical Characteristics

VDD = 3.0 V, VREF = 2.40 V, PGA Gain = 1, –40 to +85 ×C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **DC Accuracy** | | | | | |
| Resolution | | — | 8 | — | bits |
| Integral Nonlinearity | | — | — | ±1/2 | LSB |
| Differential Nonlinearity | Guaranteed Monotonic | — | — | ±1/2 | LSB |
| Offset Error | | ±2 | — | ±1/2 | LSB |
| Gain Error | | ±2 | — | ±1/2 | LSB |
| Offset Temperature Coefficient | | | ±0.25 | — | ppm/°C |
| **Dynamic Performance** (10 kHz sine-wave input, 0 to –1 dB of full scale, 100 ksps) | | | | | |
| Signal-to-Noise Plus Distortion | | 49.5 | — | — | dB |
| Total Harmonic Distortion | Up to the 5$^{th}$ harmonic | –60 | –65 | — | dB |
| Spurious-Free Dynamic Range | | — | –65 | — | dB |
| **Conversion Rate** | | | | | |
| Conversion Time in SAR Clocks | | 16 | — | — | clocks |
| SAR Clock Frequency | | | — | 2.5 | MHz |
| Track/Hold Acquisition Time | | 1.5 | — | — | µs |
| Throughput Rate | | — | — | 100 | ksps |
| **Analog Inputs** | | | | | |
| Input Voltage Range | | 0 | — | $V_{DD}$ | V |
| Input Capacitance | | — | 10 | — | pF |
| **Power Specifications** | | | | | |
| Power Supply Current | Operating Mode, 100 ksps | — | 0.45 | 1.0 | mA |
| Power Supply Current in Shutdown | | — | 0.1 | 1 | µA |
| Power Supply Rejection | | — | ±0.3 | — | mV/V |

## 6.2. ADC Modes of Operation

The ADC has a maximum conversion speed of 100 ksps. The ADC conversion clock is derived from the system clock. The ADC conversion clock is derived from a divided version of SYSCLK. Divide ratios of 1, 2, 4, 8, or 16 are supported by setting the ADCSC bits in the ADC0CF Register. This is useful to adjust conversion speed to accommodate different system clock speeds.

A conversion can be initiated in one of two ways, depending on the programmed states of the ADC Start of Conversion Mode bits (ADSTM1, ADSTM0) in ADC0CN. Conversions may be initiated by:

1. Writing a 1 to the ADBUSY bit of ADC0CN;
2. A Timer 2 overflow (i.e. timed continuous conversions).

Writing a 1 to ADBUSY provides software control of the ADC whereby conversions are performed "on-demand". During conversion, the ADBUSY bit is set to 1 and restored to 0 when conversion is complete. The falling edge of ADBUSY triggers an interrupt (when enabled) and sets the ADCINT interrupt flag in the ADC0CN register. Note: When conversions are performed "on-demand", the ADCINT flag, not ADBUSY, should be polled to determine when the conversion has completed. Converted data is available in the ADC data word register, ADC0H.

The ADCTM bit in register ADC0CN controls the ADC track-and-hold mode. In its default state, the ADC input is continuously tracked, except when a conversion is in progress. Setting ADCTM to 1 allows one of two different low power track-and-hold modes to be specified by states of the ADSTM1-0 bits (also in ADC0CN):

1. Tracking begins with a write of 1 to ADBUSY and lasts for 3 SAR clocks;
2. Tracking starts with an overflow of Timer 2 and lasts for 3 SAR clocks.

Tracking can be disabled (shutdown) when the entire chip is in low power standby or sleep modes.

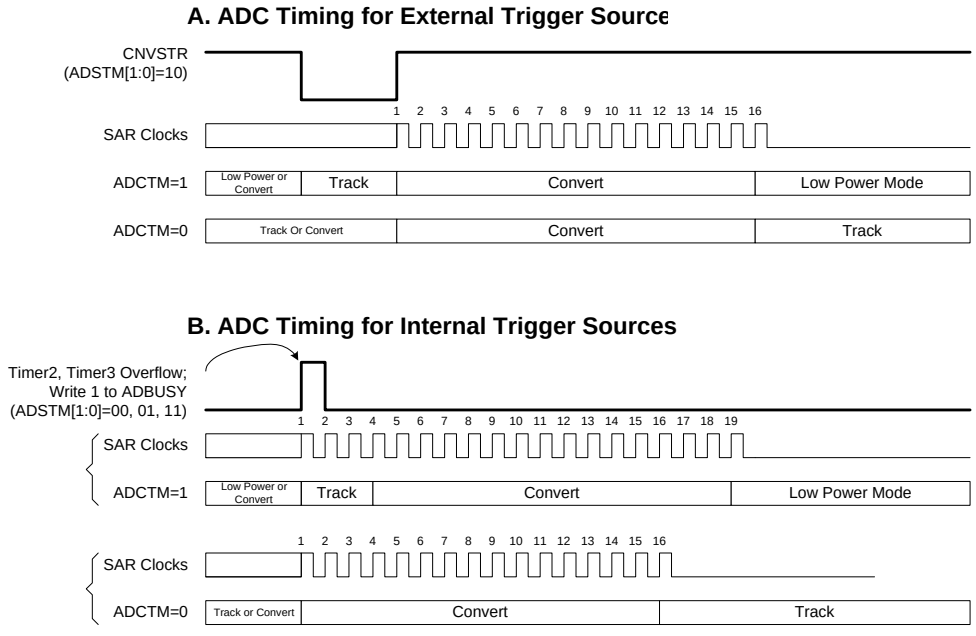


**Figure 6.2. 12-Bit ADC Track and Conversion Example Timing**

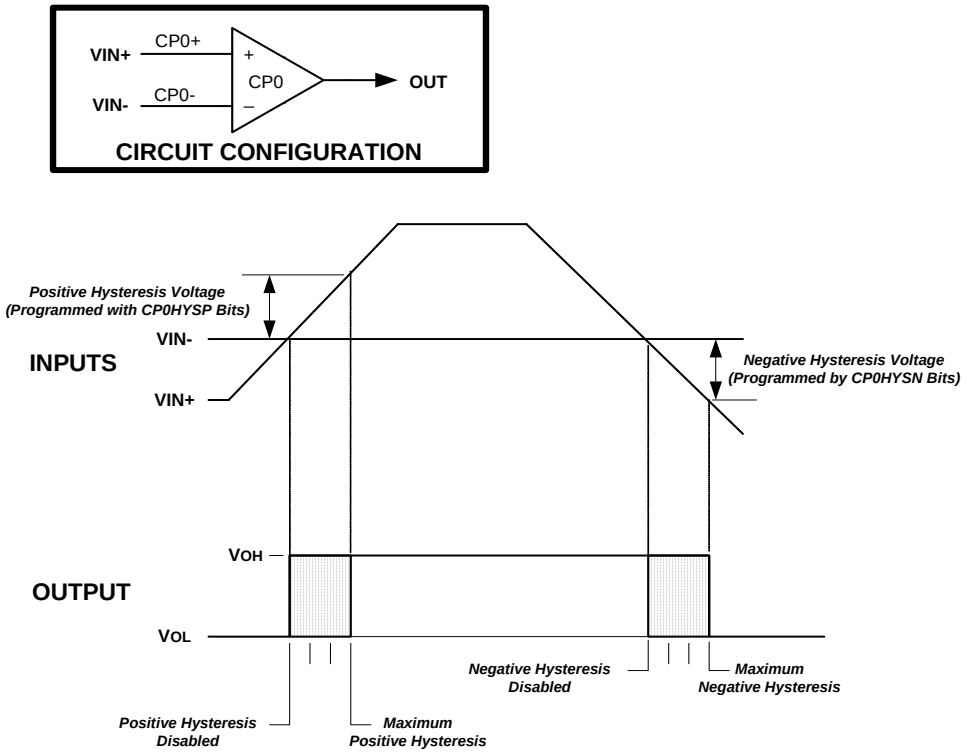


**Figure 8.2. Comparator Hysteresis Plot**

## SFR Definition 9.4. PSW: Program Status Word

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R | Reset Value |
|---|---|---|---|---|---|---|---|---|
| CY | AC | F0 | RS1 | RS0 | OV | F1 | PARITY | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (bit addressable) | SFR Address: 0xD0 |

Bit7: CY: Carry Flag.
This bit is set when the last arithmetic operation results in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: AC: Auxiliary Carry Flag.
This bit is set when the last arithmetic operation results in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: F0: User Flag 0.
This is a bit-addressable, general-purpose flag for use under software control.

Bits4–3: RS1–RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

| RS1 | RS0 | Register Bank | Address |
|---|---|---|---|
| 0 | 0 | 0 | 0x00–0x07 |
| 0 | 1 | 1 | 0x08–0x0F |
| 1 | 0 | 2 | 0x10–0x17 |
| 1 | 1 | 3 | 0x18–0x1F |

Note: Any instruction which changes the RS1–RS0 bits must not be immediately followed by the “MOV Rn, A” instruction.

Bit2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:
•An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
•A MUL instruction results in an overflow (result is greater than 255).
•A DIV instruction causes a divide-by-zero condition.
The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: PARITY: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

## SFR Definition 9.5. ACC: Accumulator

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| ACC.7 | ACC.6 | ACC.5 | ACC.4 | ACC.3 | ACC.2 | ACC.1 | ACC.0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (bit addressable) | SFR Address: 0xE0 |

Bits 7–0: ACC: Accumulator
This register is the accumulator for arithmetic operations.

## SFR Definition 9.6. B: B Register

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| B.7 | B.6 | B.5 | B.4 | B.3 | B.2 | B.1 | B.0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (bit addressable) | SFR Address: 0xF0 |

Bits 7–0: B: B Register
This register serves as a second accumulator for certain arithmetic operations.

### 9.4.6. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described below. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

**SFR Definition 9.8. IE: Interrupt Enable**

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| EA | - | ET2 | ES | ET1 | EX1 | ET0 | EX0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (bit addressable) | SFR Address: 0xA8 |

Bit7: EA: Enable All Interrupts.
This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings.
0: Disable all interrupt sources.
1: Enable each interrupt according to its individual mask setting.

Bit6: UNUSED. Read = 0, Write = don't care.

Bit5: ET2: Enable Timer 2 Interrupt.
This bit sets the masking of the Timer 2 interrupt.
0: Disable all Timer 2 interrupts.
1: Enable interrupt requests generated by the TF2 flag (T2CON.7)

Bit4: ES: Enable Serial Port (UART) Interrupt.
This bit sets the masking of the Serial Port (UART) interrupt.
0: Disable all UART interrupts.
1: Enable interrupt requests generated by the R1 flag (SCON.0) or T1 flag (SCON.1).

Bit3: ET1: Enable Timer 1 Interrupt.
This bit sets the masking of the Timer 1 interrupt.
0: Disable all Timer 1 interrupts.
1: Enable interrupt requests generated by the TF1 flag (TCON.7).

Bit2: EX1: Enable External Interrupt 1.
This bit sets the masking of external interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the /INT1 pin.

Bit1: ET0: Enable Timer 0 Interrupt.
This bit sets the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5).

Bit0: EX0: Enable External Interrupt 0.
This bit sets the masking of external interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the /INT0 pin.

## SFR Definition 9.9. IP: Interrupt Priority

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 (bit addressable) | SFR Address: 0xB8 |

Bits7–6: UNUSED. Read = 00b, Write = don't care.

Bit5: PT2 Timer 2 Interrupt Priority Control.
This bit sets the priority of the Timer 2 interrupts.
0: Timer 2 interrupts set to low priority level.
1: Timer 2 interrupts set to high priority level.

Bit4: PS: Serial Port (UART) Interrupt Priority Control.
This bit sets the priority of the Serial Port (UART) interrupts.
0: UART interrupts set to low priority level.
1: UART interrupts set to high priority level.

Bit3: PT1: Timer 1 Interrupt Priority Control.
This bit sets the priority of the Timer 1 interrupts.
0: Timer 1 interrupts set to low priority level.
1: Timer 1 interrupts set to high priority level.

Bit2: PX1: External Interrupt 1 Priority Control.
This bit sets the priority of the External Interrupt 1 interrupts.
0: External Interrupt 1 set to low priority level.
1: External Interrupt 1 set to high priority level.

Bit1: PT0: Timer 0 Interrupt Priority Control.
This bit sets the priority of the Timer 0 interrupts.
0: Timer 0 interrupts set to low priority level.
1: Timer 0 interrupt set to high priority level.

Bit0: PX0: External Interrupt 0 Priority Control.
This bit sets the priority of the External Interrupt 0 interrupts.
0: External Interrupt 0 set to low priority level.
1: External Interrupt 0 set to high priority level.

## SFR Definition 9.11. EIE2: Extended Interrupt Enable 2

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| EXVLD | - | ESCI3 | ESCI2 | ESCI1 | ESCI0 | EADC0 | - | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xE7 |

Bit7: EXVLD: Enable External Clock Source Valid (XTLVLD) Interrupt.
This bit sets the masking of the XTLVLD interrupt.
0: Disable all XTLVLD interrupts.
1: Enable interrupt requests generated by the XTLVLD flag (OSCXCN.7)

Bit6: Reserved. Must write 0. Reads 0.

Bit5: ESCI3: Enable Software Controlled Interrupt 3.
This bit sets the masking of Software Controlled Interrupt 3.
0: Disable Software Controlled Interrupt 3.
1: Enable interrupt requests generated setting the Software Controlled Interrupt Bit 3.

Bit4: ESCI2: Enable Software Controlled Interrupt 2.
This bit sets the masking of Software Controlled Interrupt 2.
0: Disable Software Controlled Interrupt 2.
1: Enable interrupt requests generated setting the Software Controlled Interrupt Bit 2.

Bit3: ESCI1: Enable Software Controlled Interrupt 1.
This bit sets the masking of Software Controlled Interrupt 1.
0: Disable Software Controlled Interrupt 1.
1: Enable interrupt requests generated setting the Software Controlled Interrupt Bit 1.

Bit2: ESCI0: Enable Software Controlled Interrupt 0.
This bit sets the masking of Software Controlled Interrupt 0.
0: Disable Software Controlled Interrupt 0.
1: Enable interrupt requests generated setting the Software Controlled Interrupt Bit 0.

Bit1: EADC0: Enable ADC0 End of Conversion Interrupt.
This bit sets the masking of the ADC0 End of Conversion Interrupt.
0: Disable ADC0 Conversion Interrupt.
1: Enable interrupt requests generated by the ADC0 Conversion Interrupt.

Bit0: Reserved. Read = 0, Write = don't care.

## SFR Definition 9.12. EIP1: Extended Interrupt Priority 1

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| PCP1R | PCP1F | PCP0R | PCP0F | - | PWADC0 | - | PSPI0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xF6 |

Bit7: PCP1R: Comparator 1 (CP1) Rising Interrupt Priority Control.
This bit sets the priority of the CP1 interrupt.
0: CP1 rising interrupt set to low priority level.
1: CP1 rising interrupt set to high priority level.

Bit6: PCP1F: Comparator 1 (CP1) Falling Interrupt Priority Control.
This bit sets the priority of the CP1 interrupt.
0: CP1 falling interrupt set to low priority level.
1: CP1 falling interrupt set to high priority level.

Bit5: PCP0R: Comparator 0 (CP0) Rising Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: CP0 rising interrupt set to low priority level.
1: CP0 rising interrupt set to high priority level.

Bit4: PCP0F: Comparator 0 (CP0) Falling Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: CP0 falling interrupt set to low priority level.
1: CP0 falling interrupt set to high priority level.

Bit3: Reserved. Read = 0, Write = don't care.

Bit2: PWADC0: Analog-to-Digital Converter 0 window compare (ADC0) Interrupt Priority Control.
This bit sets the priority of the ADC0 window compare interrupt.
0: ADC0 window compare interrupt set to low priority level.
1: ADC0 window compare interrupt set to high priority level.

Bit1: UNUSED. Read = 0, Write = don't care.

Bit0: PSPI0: Serial Peripheral Interface 0 Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.

## 12. Reset Sources

The reset circuitry of the MCU allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the CIP-51 halts program execution, forces the external port pins to a known state and initializes the SFRs to their defined reset values. Interrupts and timers are disabled. On exit, the program counter (PC) is reset, and program execution starts at location 0x0000.

All of the SFRs are reset to predefined values. The reset values of the SFR bits are defined in the SFR detailed descriptions. The contents of internal data memory are not changed during a reset and any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic ones), activating internal weak pull-ups which take the external I/O pins to a high state. The weak pull-ups are enabled during and after the reset. If the source of reset is from the $V_{DD}$ Monitor or writing a '1' to the PORSF bit, the $\overline{RST}$ pin is driven low until the end of the $V_{DD}$ reset timeout.

On exit from the reset state, the MCU uses the internal oscillator running at 2MHz as the system clock by default. Refer to Section 13 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval. (Section 12.7 details the use of the Watchdog Timer.) Once the system clock source is stable, program execution begins at location 0x0000.

There are six sources for putting the MCU into the reset state: power-on/power-fail ($V_{DD}$ monitor), external $\overline{RST}$ pin, software commanded, Comparator 0, Missing Clock Detector, and Watchdog Timer. Each reset source is described below:

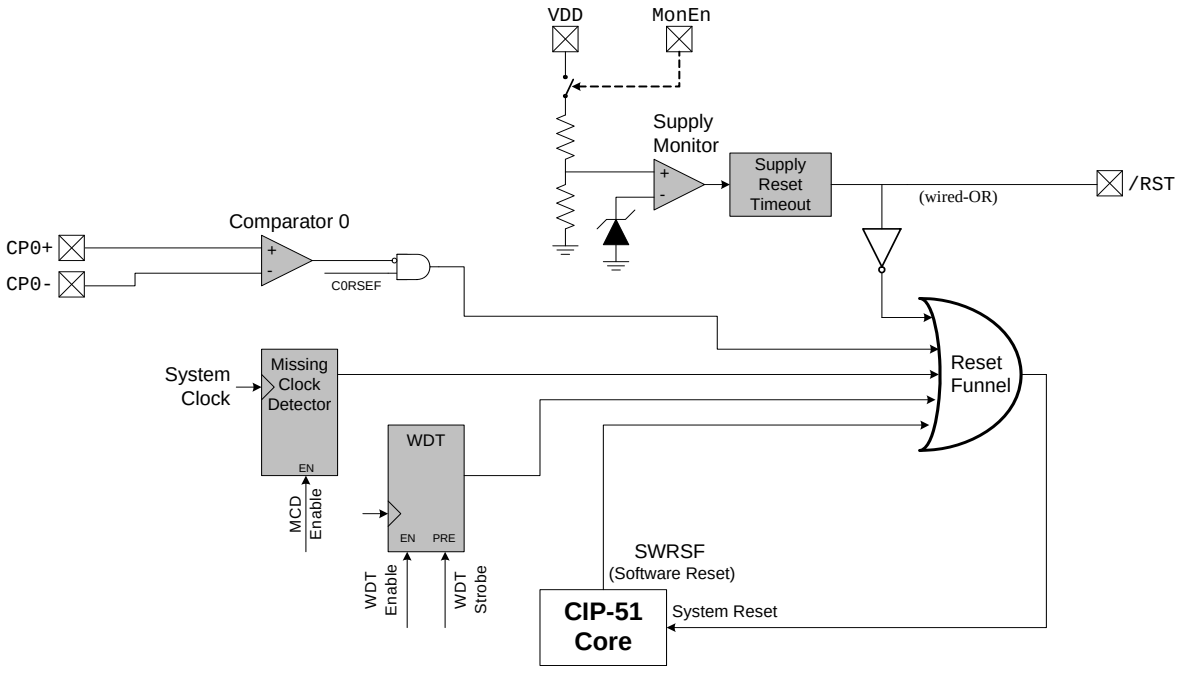


**Figure 12.1. Reset Sources Diagram**

## 15. Serial Peripheral Interface Bus

The Serial Peripheral Interface (SPI) provides access to a four-wire, full-duplex, serial bus. SPI supports the connection of multiple slave devices to a master device on the same bus. A separate slave-select signal (NSS) is used to select a slave device and enable a data transfer between the master and the selected slave. Multiple masters on the same bus are also supported. Collision detection is provided when two or more masters attempt a data transfer at the same time. The SPI can operate as either a master or a slave. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency.

When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less that 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of ¼ the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

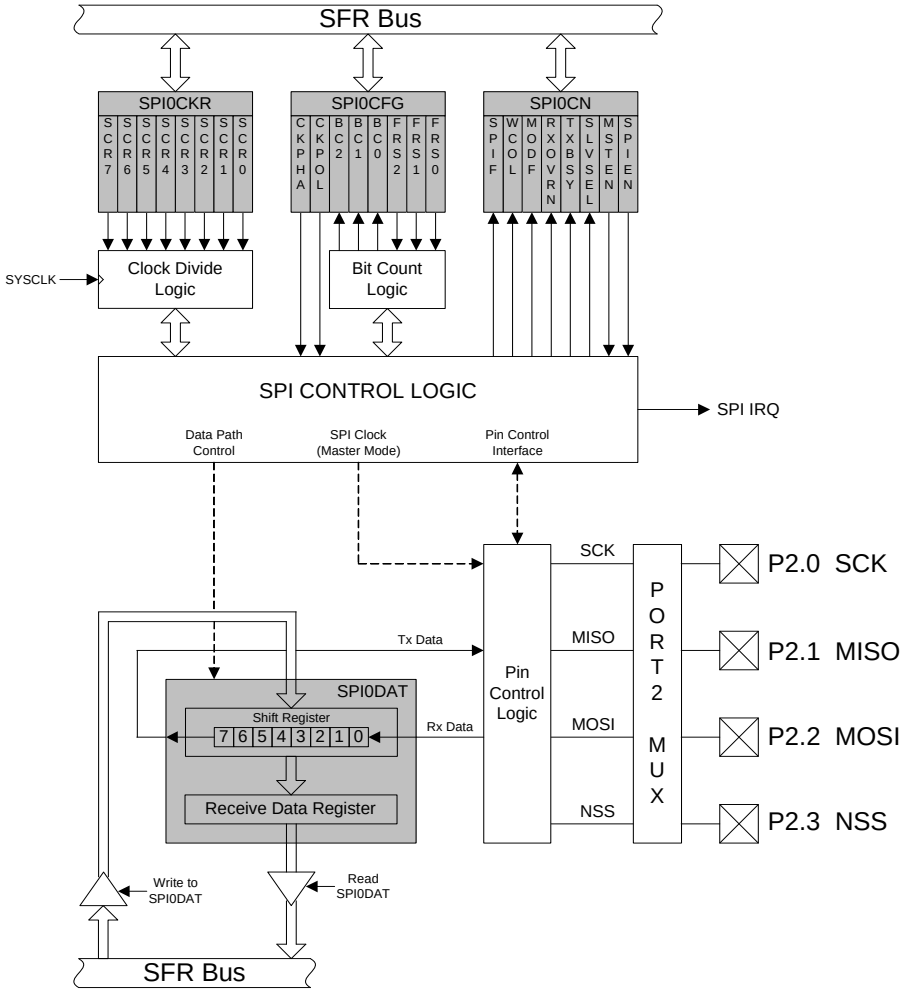


**Figure 15.1. SPI Block Diagram**

## SFR Definition 15.1. SPI0CFG: SPI Configuration

| R/W | R/W | R | R | R | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| CKPHA | CKPOL | BC2 | BC1 | BC0 | SPIFRS2 | SPIFRS1 | SPIFRS0 | 00000111 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x9A |

Bit7: CKPHA: SPI Clock Phase.
This bit controls the SPI clock phase.
0: Data sampled on first edge of SCK period.
1: Data sampled on second edge of SCK period.

Bit6: CKPOL: SPI Clock Polarity.
This bit controls the SPI clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

Bits5–3: BC2–BC0: SPI Bit Count.
Indicates which of the up to 8 bits of the SPI word have been transmitted.

| BC2–BC0 | | | Bit Transmitted |
|---|---|---|---|
| 0 | 0 | 0 | Bit 0 (LSB) |
| 0 | 0 | 1 | Bit 1 |
| 0 | 1 | 0 | Bit 2 |
| 0 | 1 | 1 | Bit 3 |
| 1 | 0 | 0 | Bit 4 |
| 1 | 0 | 1 | Bit 5 |
| 1 | 1 | 0 | Bit 6 |
| 1 | 1 | 1 | Bit 7 (MSB) |

Bits2–0: SPIFRS2–SPIFRS0: SPI Frame Size.
These three bits determine the number of bits to shift in/out of the SPI shift register during a data transfer in master mode. They are ignored in slave mode.

| SPIFRS | | | Bits Shifted |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | 6 |
| 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 8 |

## 16.2. Multiprocessor Communications

Modes 2 and 3 support multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0.

Setting the SM2 bit (SCON.5) of a slave processor configures its UART such that when a stop bit is received, the UART will generate an interrupt only if the ninth bit is logic one (RB8 = 1) signifying an address byte has been received. In the UART's interrupt handler, software will compare the received address with the slave's own assigned 8-bit address. If the addresses match, the slave will clear its SM2 bit to enable interrupts on the reception of the following data byte(s). Slaves that weren't addressed leave their SM2 bits set and do not generate interrupts on the reception of the following data bytes, thereby ignoring the data. Once the entire message is received, the addressed slave resets its SM2 bit to ignore all transmissions until it receives the next address byte.

Multiple addresses can be assigned to a single slave and/or a single address can be assigned to multiple slaves, thereby enabling "broadcast" transmissions to more than one slave simultaneously. The master processor can be configured to receive all transmissions or a protocol can be implemented such that the master/slave role is temporarily reversed to enable half-duplex transmission between the original master and slave(s).

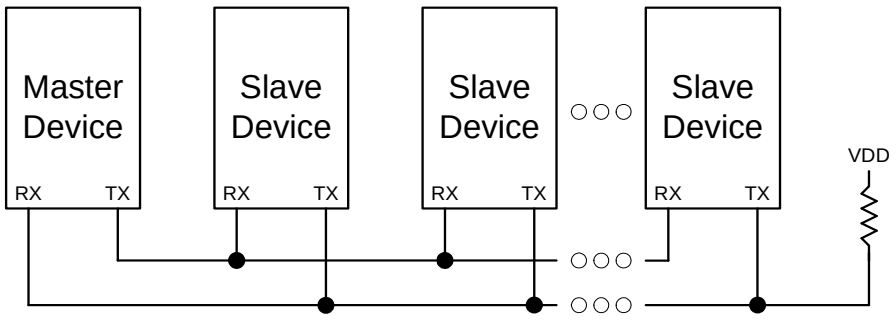


**Figure 16.7. UART Multi-Processor Mode Interconnect Diagram**

**Table 16.2. Oscillator Frequencies for Standard Baud Rates**

| Oscillator Frequency (MHz) | Divide Factor | Timer 1 Load Value* | Resulting Baud Rate** |
|---|---|---|---|
| 24.0 | 208 | 0xF3 | 115200 (115384) |
| 23.592 | 205 | 0xF3 | 115200 (113423) |
| 22.1184 | 192 | 0xF4 | 115200 |
| 18.432 | 160 | 0xF6 | 115200 |
| 16.5888 | 144 | 0xF7 | 115200 |
| 14.7456 | 128 | 0xF8 | 115200 |
| 12.9024 | 112 | 0xF9 | 115200 |
| 11.0592 | 96 | 0xFA | 115200 |
| 9.216 | 80 | 0xFB | 115200 |

# 17. Timers

The CIP-51 implements three, 16-bit counter/timers comparable with those found in the standard 8051 MCU's. These can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 offers additional capabilities not available in Timers 0 and 1, such as capture and baud rate generation.

| Timer 0 and Timer 1: | Timer 2: |
|---|---|
| 13-bit counter/timer | 16-bit counter/timer with auto-reload |
| 16-bit counter/timer | 16-bit counter/timer with capture |
| 8-bit counter/timer with auto-reload | Baud rate generator |
| Two 8-bit counter/timers (Timer 0 only) | |

When functioning as a timer, the counter/timer registers are incremented on each clock tick. Clock ticks are derived from the system clock divided by either one or twelve as specified by the Timer Clock Select bits (T2M–T0M) in CKCON. The twelve-clocks-per-tick option provides compatibility with the older generation of the 8051 family. Applications that require a faster timer can use the one-clock-per-tick option.

When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (P0.4/T0, P0.5/T1, or P0.6/T2. Events with a frequency of up to one-fourth the system clock's frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is sampled.

## 17.1. Timer 0 and Timer 1

Timer 0 and Timer 1 are accessed and controlled through SFR's. Each counter/timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control (TCON) register is used to enable Timer 0 and Timer 1 as well as indicate their status. Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits M1–M0 in the Counter/Timer Mode (TMOD) register. Each timer can be configured independently. Following is a detailed description of each operating mode.

### 17.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as a 13-bit counter/timer in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSB's of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. Clearing C/T selects the system clock as the input for the timer. When C/T0 is set to logic 1, high-to-low transitions at the selected input pin increment the timer register. (Refer to section 14 for information on selecting and configuring external I/O pins.)

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is 0 or the input signal /INT0 is logic-level one. Setting GATE0 to logic 1 allows the timer to be controlled by the external input signal /INT0, facilitating pulse width measurements.

## SFR Definition 17.2. TMOD: Timer Mode

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| GATE1 | C/T1 | T1M1 | T1M0 | GATE0 | C/T0 | T0M1 | T0M0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x89 |

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic level one.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin P0.5/T1.

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

| T1M1 | T1M0 | Mode |
|---|---|---|
| 0 | 0 | Mode 0: 13-bit counter/timer |
| 0 | 1 | Mode 1: 16-bit counter/timer |
| 1 | 0 | Mode 2: 8-bit counter/timer with auto-reload |
| 1 | 1 | Mode 3: Timer 1 Inactive/stopped |

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic level one.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin P0.4/T0.

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

| T0M1 | T0M0 | Mode |
|---|---|---|
| 0 | 0 | Mode 0: 13-bit counter/timer |
| 0 | 1 | Mode 1: 16-bit counter/timer |
| 1 | 0 | Mode 2: 8-bit counter/timer with auto-reload |
| 1 | 1 | Mode 3: Two 8-bit counter/timers |

## SFR Definition 17.3. CKCON: Clock Control

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | - | T2M | T1M | T0M | - | - | - | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x8E |

Bits7–6: UNUSED. Read = 00b, Write = don't care.

Bit5: T2M: Timer 2 Clock Select.
This bit controls the division of the system clock supplied to Timer 2. This bit is ignored when the timer is in baud rate generator mode or counter mode (i.e. C/T2 = 1).
0: Timer 2 uses the system clock divided by 12.
1: Timer 2 uses the system clock.

Bit4: T1M: Timer 1 Clock Select.
This bit controls the division of the system clock supplied to Timer 1.
0: Timer 1 uses the system clock divided by 12.
1: Timer 1 uses the system clock.

Bit3: T0M: Timer 0 Clock Select.
This bit controls the division of the system clock supplied to Counter/Timer 0.
0: Counter/Timer uses the system clock divided by 12.
1: Counter/Timer uses the system clock.

Bits2–0: UNUSED. Read = 000b, Write = don't care.

### SFR Definition 17.4. TL0: Timer 0 Low Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x8A |

Bits 7–0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

### SFR Definition 17.5. TL1: Timer 1 Low Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x8B |

Bits 7–0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

### SFR Definition 17.6. TH0: Timer 0 High Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x8C |

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

### SFR Definition 17.7. TH1: Timer 1 High Byte

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x8D |

Bits 7–0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.