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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f206

NOTES:

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS. Figure 1.5 shows a comparison of peak throughputs of various 8-bit microcontroller cores with their maximum system clocks.

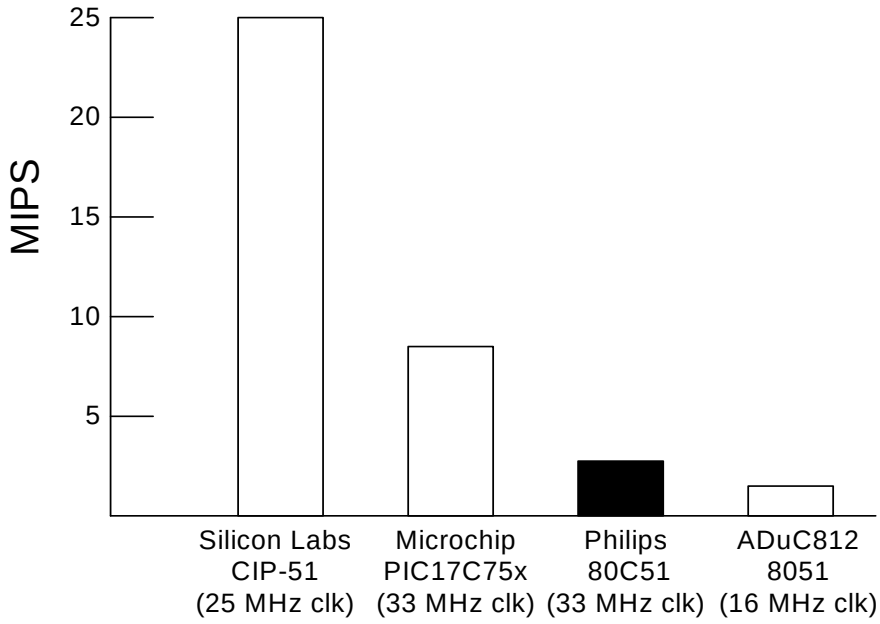


Figure 1.5. Comparison of Peak MCU Throughputs

1.1.3. Additional Features

The C8051F206, C8051F220/1/6 and C8051F230/1/6 have several key enhancements both inside and outside the CIP-51 core to improve overall performance and ease of use in end applications.

The extended interrupt handler provides 22 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing the numerous analog and digital peripherals to interrupt the controller. (An interrupt driven system requires less intervention by the MCU, giving it more effective throughput.) The extra interrupt sources are very useful when building multi-tasking, real-time systems.

There are up to six reset sources for the MCU: an on-board V_{DD} monitor, a Watchdog Timer, a missing clock detector, a voltage level detection from Comparator 0, a forced software reset, and an external reset pin. The $\overline{\text{RST}}$ pin is bi-directional, accommodating an external reset, or allowing the internally generated reset to be output on the $\overline{\text{RST}}$ pin. The on-board V_{DD} monitor is enabled by pulling the MONEN pin high (digital 1). The user may disable each reset source except for the V_{DD} monitor and Reset Input Pin from software. The watchdog timer may be permanently enabled in software after a power-on reset during MCU initialization.

The MCU has an internal, stand-alone clock generator that is used by default as the system clock after reset. If desired, the clock source may be switched "on the fly" to the external oscillator, which can use a crystal, ceramic resonator, capacitor, RC, or external clock source to generate the system clock. This can be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) external crystal source, while periodically switching to the fast (up to 16MHz) internal oscillator as needed.

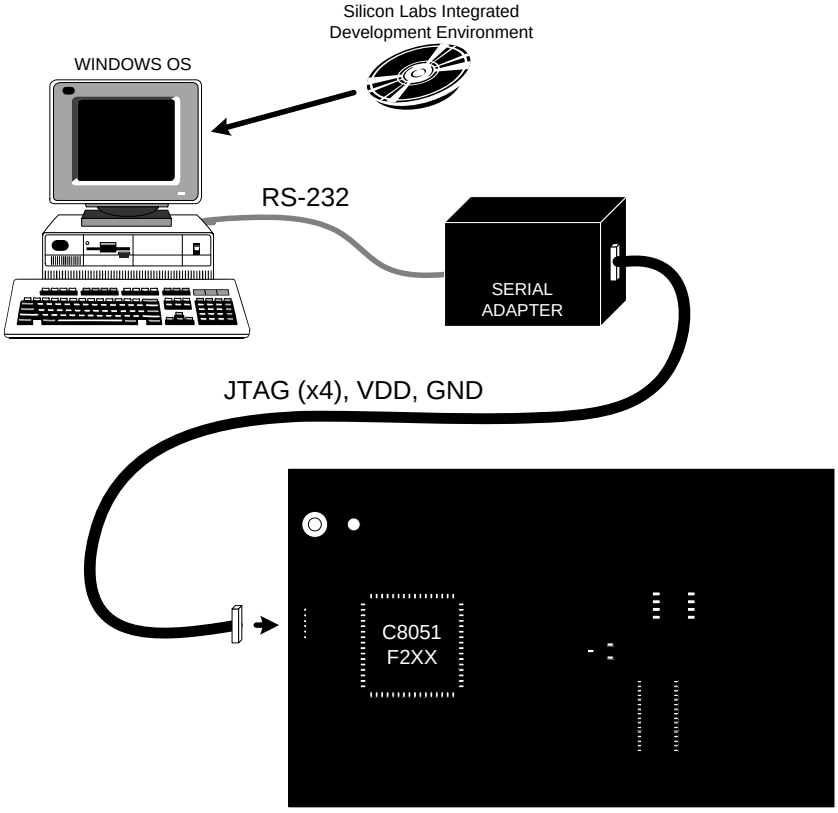


Figure 1.8. Degub Environment Diagram

1.4. Digital/Analog Configurable I/O

The standard 8051 Ports (0, 1, 2, and 3) are available on the device. The ports behave like standard 8051 ports with a few enhancements.

Each port pin can be configured as either a push-pull or open-drain output. Any input that is configured as an analog input will have its corresponding weak pull-up turned off.

Digital resources (timers, SPI, UART, system clock, and comparators) are routed to corresponding I/O pins by configuring the port multiplexer. Port multiplexers are programmed by setting bits in SFR's (please see Section 14). Any of the 32 external port pins may be configured as either analog inputs or digital I/O (See Figure 1.9), so effectively, all port pins are dual function.

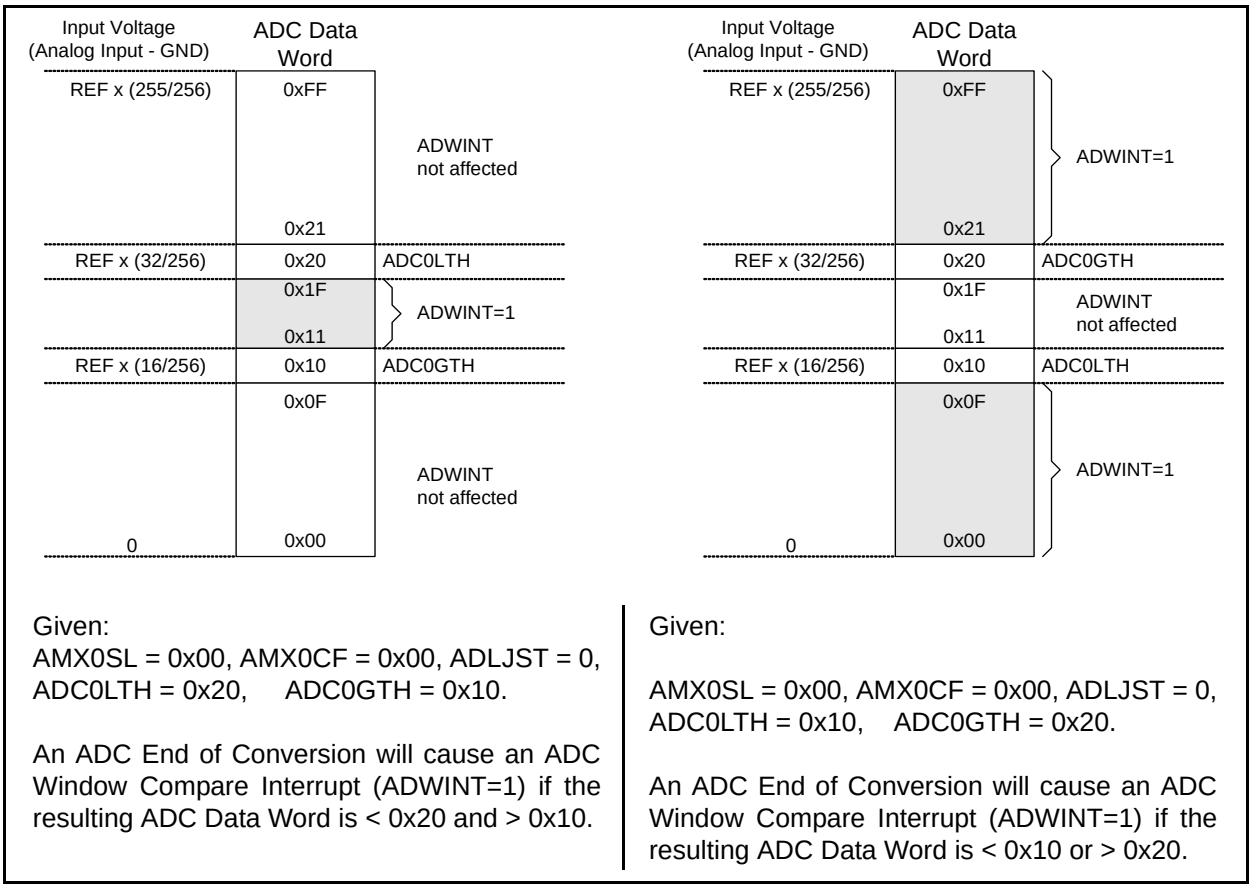
SFR Definition 5.2. ADC0CF: ADC Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCSC2	ADCSC1	ADCSC0	-	-	AMPGN2	AMPGN1	AMPGN0	01100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBC

Bits7–5: ADCSC2–0: ADC SAR Conversion Clock Period Bits
000: SAR Conversion Clock = 1 System Clock
001: SAR Conversion Clock = 2 System Clocks
010: SAR Conversion Clock = 4 System Clocks
011: SAR Conversion Clock = 8 System Clocks
1xx: SAR Conversion Clock = 16 Systems Clocks
NOTE: SAR conversion clock should be less than or equal to 2MHz.

Bits4–3: UNUSED. Read = 00b; Write = don't care

Bits2–0: AMPGN2–0: ADC Internal Amplifier Gain
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
11x: Gain = 0.5



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,
ADC0LTH = 0x20, ADC0GTH = 0x10.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x20 and > 0x10.

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0,
ADC0LTH = 0x10, ADC0GTH = 0x20.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x10 or > 0x20.

Figure 5.3. 8-Bit ADC Window Interrupt Examples

Table 6.1. 12-Bit ADC Electrical Characteristics (C8015F206 only)

V_{DD} = 3.0 V, VREF = 2.40 V (REFBE=0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	±1	±2	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±2	LSB
Offset Error		±20	±5	—	LSB
Full Scale Error	Differential mode	—	—	–20±10	LSB
Offset Temperature Coefficient		—	±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to –1 dB of full scale, 100 ksps)					
Signal-to-Noise Plus Distortion		63	66	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	–60	–72	—	dB
Spurious-Free Dynamic Range		60	76	—	dB
Conversion Rate					
Conversion Time in SAR Clocks		16	—	—	clocks
SAR Clock Frequency		—	—	2.0	MHz
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Voltage Conversion Range		0	—	VREF	V
Input Voltage	Any pin (in Analog Input Mode)	GND	—	V_{DD}	V
Input Capacitance		—	10	—	pF
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC)	Operating Mode, 100 ksps	—	0.45	1.0	mA
Power Supply Rejection		—	±0.3	—	mV/V

Table 7.1. Reference Electrical Characteristics

V_{DD} = 3.0 V, Temperature –40 to +85 ×C

External Reference ([REFSL1: REFSL0] = 00), V_{REF} = 2.4 V)		Min	Typ	Max	Units
Input Voltage Range		1.00	—	(V_{DD}) – 0.3 V	V
Input Current		—	0.1	10	µA
Input Resistance		100	—	—	MΩ

SFR Definition 8.2. CPT1CN: Comparator 1 Control

R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CP1EN	CP1OUT	CP1RIF	CP1FIF	CP1HYP1	CP1HYP0	CP1HYN1	CP1HYN0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9F

Bit7: CP1EN: Comparator 1 Enable Bit
0: Comparator 1 Disabled.
1: Comparator 1 Enabled.

Bit6: CP1OUT: Comparator 1 Output State Flag
0: Voltage on CP1+ < CP1–
1: Voltage on CP1+ > CP1–

Bit5: CP1RIF: Comparator 1 Rising-Edge Interrupt Flag
0: No Comparator 1 Rising-Edge Interrupt has occurred since this flag was cleared
1: Comparator 1 Rising-Edge Interrupt has occurred since this flag was cleared

Bit4: CP1FIF: Comparator 1 Falling-Edge Interrupt Flag
0: No Comparator 1 Falling-Edge Interrupt has occurred since this flag was cleared
1: Comparator 1 Falling-Edge Interrupt has occurred since this flag was cleared

Bit3–2: CP1HYP1–0: Comparator 1 Positive Hysteresis Control Bits
00: Positive Hysteresis Disabled
01: Positive Hysteresis = 2 mV
10: Positive Hysteresis = 4 mV
11: Positive Hysteresis = 10 mV

Bit1–0: CP1HYN1–0: Comparator 1 Negative Hysteresis Control Bits
00: Negative Hysteresis Disabled
01: Negative Hysteresis = 2 mV
10: Negative Hysteresis = 4 mV
11: Negative Hysteresis = 10 mV

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0–R7 of the currently selected register bank. **@Ri -** Data RAM location addressed indirectly through register R0–R1 **rel -** 8-bit, signed (two's compliment) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct -** 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF). **#data -** 8-bit constant **#data 16 -** 16-bit constant **bit -** Direct-addressed bit in Data RAM or SFR. **addr 11 -** 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr 16 -** 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

Table 9.3. Special Function Registers (Continued)

SFR's are listed in alphabetical order.

Address	Register	Description	Page No.
0xA4	PRT0CF	Port 0 Configuration	105
0xA5	PRT1CF	Port 1 Configuration	106
0xA6	PRT2CF	Port 2 Configuration	107
0xA7	PRT3CF	Port 3 Configuration	108
0xE1	PRT0MX	Port 0 Multiplexer I/O Configuration	103
0xE2	PRT1MX	Port 1 Multiplexer I/O Configuration	104
0xE3	PRT2MX	Port 2 Multiplexer I/O Configuration	104
0x8F	PSCTL	Program Store RW Control	88
0xD0	PSW	Program Status Word	72
0xCB	RCAP2H	Counter/Timer 2 Capture (High Byte)	138
0xCA	RCAP2L	Counter/Timer 2 Capture (Low Byte)	138
0xD1	REF0CN	Voltage Reference Control Register	50
0xEF	RSTSRC	Reset Source Register	95
0x99	SBUF	Serial Data Buffer (UART)	123
0x98	SCON	Serial Port Control (UART)	124
0x81	SP	Stack Pointer	71
0x9A	SPI0CFG	Serial Peripheral Interface Configuration	114
0x9D	SPI0CKR	SPI Clock Rate	116
0xF8	SPI0CN	SPI Bus Control	115
0x9B	SPI0DAT	SPI Port 1Data	116
0xAD	SWCINT	Software Controlled Interrupt Register	75
0xC8	T2CON	Counter/Timer 2 Control	137
0x88	TCON	Counter/Timer Control	129
0x8C	TH0	Counter/Timer 0 Data Word (High Byte)	132
0x8D	TH1	Counter/Timer 1 Data Word (High Byte)	132
0xCD	TH2	Counter/Timer 2 Data Word (High Byte)	138
0x8A	TL0	Counter/Timer 0 Data Word (Low Byte)	132
0x8B	TL1	Counter/Timer 1 Data Word (Low Byte)	132
0xCC	TL2	Counter/Timer 2 Data Word (Low Byte)	138
0x89	TMOD	Counter/Timer Mode	130
0xFF	WDTCN	Watchdog Timer Control	94
0x84–86, 0x91–97, 0x9C, 0xA1–A3, 0xA9–AC, 0xAE, 0xB3–B5, 0xB9–BA, 0xBD–BE,0xC0–C4, 0xC6,0xCE–CF,0xD2–DF,0xE9–EE,0xF5,0xF9–FE	Reserved		

Notes:

1. C8051F230/1/6 Do not have these registers.
2. C8051F221/231 Does not have this register (32 pin package).
3. On the C8051F206 and C8051F226/236 only.
4. On the C8051F206 only (12-bit ADC)

SFR Definition 9.13. EIP2: Extended Interrupt Priority 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PXVLD	-	PSCI3	PSCI2	PSCI1	PSCI0	PADC0	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF7

Bit7: PXVLD: External Clock Source Valid (XTLVLD) Interrupt Priority Control.
This bit sets the priority of the XTLVLD interrupt.
0: XTLVLD interrupt set to low priority level.
1: XTLVLD interrupt set to high priority level.

Bit6: Reserved. Must write 0. Reads 0.

Bit5: PSCI3: Software Controlled Interrupt 3 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 3.
0: External Interrupt 7 set to low priority level.
1: External Interrupt 7 set to high priority level.

Bit4: PSCI2: Software Controlled Interrupt 2 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 2.
0: Software Controlled Interrupt 2 set to low priority level.
1: Software Controlled Interrupt 2 set to high priority level.

Bit3: PSCI1: Software Controlled Interrupt 1 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 1.
0: Software Controlled Interrupt 1 set to low priority level.
1: Software Controlled Interrupt 1 set to high priority level.

Bit2: PSCI0: Software Controlled Interrupt 0 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 0.
0: Software Controlled Interrupt 0 set to low priority level.
1: Software Controlled Interrupt 0 set to high priority level.

Bit1: PADC0: ADC End of Conversion Interrupt Priority Control.
This bit sets the priority of the ADC0 End of Conversion Interrupt.
0: ADC0 End of Conversion interrupt set to low priority level.
1: ADC0 End of Conversion interrupt set to high priority level.

Bit0: Reserved. Read = 0, Write = don't care.

write/erase operations are disabled. Note that code execution in the 8051 is stalled while the Flash is being programmed or erased.

Table 10.1. Flash Memory Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 ×C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Endurance		20 k	100 k	—	Erase/Wr
Erase/Write Cycle Time		—	10	—	ms

Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX instruction and read using the MOVC instruction.

The MCU incorporates an additional 128-byte sector of Flash memory located at 0x2000 – 0x207F. This sector can be used for program code or data storage. However, its smaller sector size makes it particularly well suited as general purpose, non-volatile scratchpad memory. Even though Flash memory can be written a single byte at a time, an entire sector must be erased first. In order to change a single byte of a multi-byte data set, the data must be moved to temporary storage. Next, the sector is erased, the data set updated and the data set returned to the original sector. The 128-byte sector-size facilitates updating data without wasting program memory space by allowing the use of internal data RAM for temporary storage. (A normal 512-byte sector is too large to be stored in the 256-byte internal data memory.)

10.2. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as prevent the viewing of proprietary program code and constants. The Program Store Write Enable (PSCTL.0) and the Program Store Erase Enable (PSCTL.1) bits protect the Flash memory from accidental modification by software. These bits must be explicitly set to logic 1 before software can modify the Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the JTAG interface or by software running on the system controller.

A set of security lock bytes stored at 0x1DFE and 0x1DFF protect the Flash program memory from being read or altered across the JTAG interface. Each bit in a security lock-byte protects one 1 kB block of memory. Clearing a bit to logic 0 in a Read lock byte prevents the corresponding block of Flash memory from being read across the JTAG interface. Clearing a bit in the Write/Erase lock byte protects the block from JTAG erasures and/or writes. The Read lock byte is at location 0x1DFF. The Write/Erase lock byte is located at 0x1DFE. Figure 10.1 shows the location and bit definitions of the security bytes. The 512-byte sector containing the lock byte cannot be erased by software. Writing to the reserved area should not be performed.

SFR Definition 13.2. OSCXCN: External Oscillator Control

R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
XTLVLD	XOSCMD2	XOSCMD1	XOSCMD0	-	XFCN2	XFCN1	XFCN0	00110000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xB1

Bit7: XTLVLD: Crystal Oscillator Valid Flag
(Valid only when XOSCMD = 1xx.)
0: Crystal Oscillator is unused or not yet stable
1: Crystal Oscillator is running and stable

Bits6–4: XOSCMD2–0: External Oscillator Mode Bits
00x: Off. XTAL1 pin is grounded internally.
010: System Clock from External CMOS Clock on XTAL1 pin.
011: System Clock from External CMOS Clock on XTAL1 pin divided by 2.
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = undefined, Write = don't care

Bits2–0: XFCN2–0: External Oscillator Frequency Control Bits
000–111: see table below

XFCN	Crystal (XOSCMD = 11x)	RC (XOSCMD = 10x)	C (XOSCMD = 10x)
000	f ≤ 12.5 kHz	f ≤ 25 kHz	K Factor = 0.44
001	12.5 kHz < f ≤ 30.3 kHz	25 kHz < f ≤ 50 kHz	K Factor = 1.4
010	30.35 kHz < f ≤ 93.8 kHz	50 kHz < f ≤ 100 kHz	K Factor = 4.4
011	93.8 kHz < f ≤ 26 7kHz	100 kHz < f ≤ 200 kHz	K Factor = 13
100	267 kHz < f ≤ 722 kHz	200 kHz < f ≤ 400 kHz	K Factor = 38
101	722 kHz < f ≤ 2.23 MHz	400 kHz < f ≤ 800 kHz	K Factor = 100
110	2.23 MHz < f ≤ 6.74 MHz	800 kHz < f ≤ 1.6 MHz	K Factor = 420
111	f > 6.74 MHz	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1400

CRYSTAL MODE (Circuit from Figure 13.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match the crystal frequency.

RC MODE (Circuit from Figure 13.1, Option 2; XOSCMD = 10x)
Choose oscillation frequency range where:
$f = 1.23(10^3) / (R \times C)$, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pull-up resistor value in kΩ

C MODE (Circuit from Figure 13.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
$f = KF / (C \times AV+)$, where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
V_{DD} = Power supply voltage on MCU in volts

13.1. External Crystal Example

If a crystal were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 1. For an ECS-110.5-20-4 crystal, the resonate frequency is 11.0592 MHz, the intrinsic capacitance is 7 pF, and the ESR is 60 W. The compensation capacitors should be 33 pF each, and the PWB parasitic capacitance is estimated to be 2 pF. The appropriate External Oscillator Frequency Control value (XFCN) from the Crystal column in the table in SFR Definition 13.2 (OSCXCN Register) should be 111b.

The Crystal Oscillator Valid Flag (XTLVLD in register OSCXCN) is set to logic 1 by hardware when the external oscillator is running and stable. The XTLVLD detection circuit requires a startup time of at least 1ms between enabling the oscillator and checking the XTLVLD flag. Switching to the external oscillator before 1ms can result in unpredictable behavior. The recommend procedure is:

1. Enable the external oscillator
2. Wait 1 ms
3. Poll for XTLVLD '0' ==> '1'
4. Switch to the external oscillator

Switching to the external oscillator before the crystal oscillator has stabilized could result in unpredictable behavior.

NOTE: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device, keeping the traces as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

13.2. External RC Example

If an external RC network were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 2. The capacitor must be no greater than 100 pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kW and C = 50 pF:

f = 1.23(103)/RC = 1.23(103) / [246 x 50] = 0.1 MHz = 100 kHz

XFCN ³ log2(f/25 kHz)
XFCN ³ log2(100 kHz/25 kHz) = log2(4)
XFCN ³ 2, or code 010

13.3. External Capacitor Example

If an external capacitor were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 3. The capacitor must be no greater than 100 pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume V_{DD} = 3.0 V and C = 50 pF:

f = KF / (C x V_{DD}) = KF / (50 x 3)
f = KF / 150

If a frequency of roughly 90kHz is desired, select the K Factor from the table in SFR Definition 13.2 as KF = 13:

f = 13 /150 = 0.087 MHz, or 87 kHz

Therefore, the XFCN value to use in this example is 011.

16.1. UART Operational Modes

The UART provides four operating modes (one synchronous and three asynchronous) selected by setting configuration bits in the SCON register. These four modes offer different baud rates and communication protocols. The four modes are summarized in Table 16.1 below. Detailed descriptions follow.

Table 16.1. UART Modes

Mode	Synchronization	Baud Clock	Data Bits	Start/Stop Bits
0	Synchronous	SYSCLK/12	8	None
1	Asynchronous	Timer 1 or Timer 2 Overflow	8	1 Start, 1 Stop
2	Asynchronous	SYSCLK/32 or SYSCLK/64	9	1 Start, 1 Stop
3	Asynchronous	Timer 1 or Timer 2 Overflow	9	1 Start, 1 Stop

16.1.1. Mode 0: Synchronous Mode

Mode 0 provides synchronous, half-duplex communication. Serial data is transmitted and received on the RX pin. The TX pin provides the shift clock for both transmit and receive. The MCU must be the master since it generates the shift clock for transmission in both directions (see the interconnect diagram in Figure 16.2).

Eight data bits are transmitted/received, LSB first (see the timing diagram in Figure 16.3). Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the eighth bit time. Data reception begins when the REN Receive Enable bit (SCON.4) is set to logic 1 and the RI Receive Interrupt Flag (SCON.0) is cleared. One cycle after the eighth bit is shifted in, the RI flag is set and reception stops until software clears the RI bit. An interrupt will occur if enabled when either TI or RI are set.

The Mode 0 baud rate is system clock frequency divided by twelve.

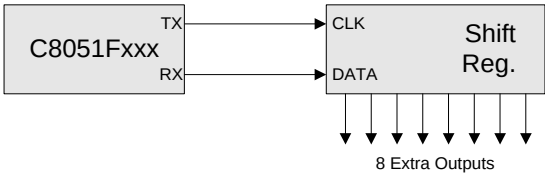


Figure 16.2. UART Mode 0 Interconnect

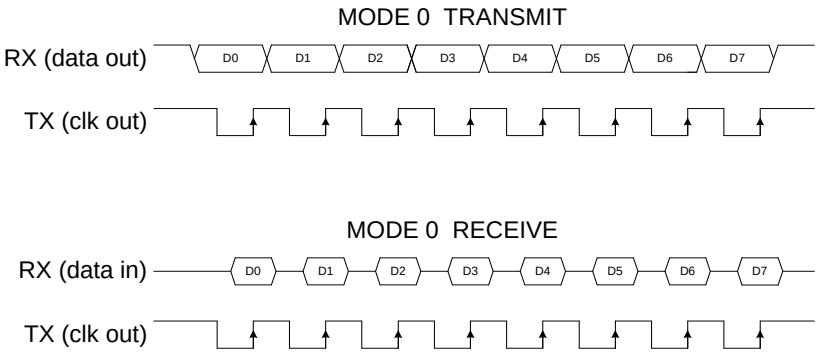


Figure 16.3. UART Mode 0 Timing Diagram

16.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit (see the timing diagram in Figure 16.4). Data are transmitted from the TX pin and received at the RX pin (see the interconnection diagram in Figure 16.5). On receive, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2).

Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: RI must be logic 0, and if SM2 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data are stored in SBUF, the stop bit is stored in RB8, and the RI flag is set. If these conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set. An interrupt will occur if enabled when either TI or RI is set.

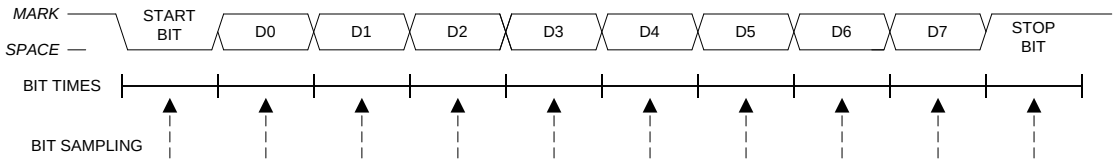


Figure 16.4. UART Mode 1 Timing Diagram

The baud rate generated in Mode 1 is a function of timer overflow. The UART can use Timer 1 operating in 8-bit Counter/Timer with Auto-Reload Mode, or Timer 2 operating in Baud Rate Generator Mode to generate the baud rate (note that the TX and RX clock sources are selected separately). On each timer overflow event (a rollover from all ones (0xFF for Timer 1, 0xFFFF for Timer 2) to zero), a clock is sent to the baud rate logic.

When Timer 1 is selected as a baud rate source, the SMOD bit (PCON.7) selects whether or not to divide the Timer 1 overflow rate by two. On reset, the SMOD bit is logic 0, thus selecting the lower speed baud rate by default. The SMOD bit affects the baud rate generated by Timer 1 as follows:

Mode 1 Baud Rate = (1 / 32) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 0).
Mode 1 Baud Rate = (1 / 16) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 1).

When Timer 2 is selected as a baud rate source, the baud rate generated by Timer 2 is as follows:

Mode 1 Baud Rate = (1 / 16) x T2_OVERFLOWRATE.

The Timer 1 overflow rate is determined by the Timer 1 clock source (T1CLK) and reload value (TH1). The frequency of T1CLK can be selected as SYSCLK, SYSCLK/12, or an external clock source. The Timer 1 overflow rate can be calculated as follows:

T1_OVERFLOWRATE = T1CLK / (256 – TH1).

For example, assume TMOD = 0x20.

Table 16.2. Oscillator Frequencies for Standard Baud Rates (Continued)

Oscillator Frequency (MHz)	Divide Factor	Timer 1 Load Value*	Resulting Baud Rate**
7.3728	64	0xFC	115200
5.5296	48	0xFD	115200
3.6864	32	0xFE	115200
1.8432	16	0xFF	115200
24.576	320	0xEC	76800
25.0	434	0xE5	57600 (57870)
25.0	868	0xCA	28800
24.576	848	0xCB	28800 (28921)
24.0	833	0xCC	28800 (28846)
23.592	819	0xCD	28800 (28911)
22.1184	768	0xD0	28800
18.432	640	0xD8	28800
16.5888	576	0xDC	28800
14.7456	512	0xE0	28800
12.9024	448	0xE4	28800
11.0592	348	0xE8	28800
9.216	320	0xEC	28800
7.3728	256	0xF0	28800
5.5296	192	0xF4	28800
3.6864	128	0xF8	28800
1.8432	64	0xFC	28800

SFR Definition 16.1. SBUF: Serial (UART) Data Buffer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x99

Bits7–0: SBUF.[7:0]: Serial Data Buffer Bits 7–0 (MSB-LSB)
This is actually two registers; a transmit and a receive buffer register. When data is moved to SBUF, it goes to the transmit buffer and is held for serial transmission. Moving a byte to SBUF is what initiates the transmission. When data is moved from SBUF, it comes from the receive buffer.

SFR Definition 17.8. T2CON: Timer 2 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:
							(bit addressable)	0xC8

Bit7: TF2: Timer 2 Overflow Flag.
Set by hardware when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software. TF2 will not be set when RCLK and/or TCLK are logic 1.

Bit6: EXF2: Timer 2 External Flag.
Set by hardware when either a capture or reload is caused by a high-to-low transition on the T2EX input pin and EXEN2 is logic 1. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 Interrupt service routine. This bit is not automatically cleared by hardware and must be cleared by software.

Bit5: RCLK: Receive Clock Flag.
Selects which timer is used for the UART's receive clock in modes 1 or 3.
0: Timer 1 overflows used for receive clock.
1: Timer 2 overflows used for receive clock.

Bit4: TCLK: Transmit Clock Flag.
Selects which timer is used for the UART's transmit clock in modes 1 or 3.
0: Timer 1 overflows used for transmit clock.
1: Timer 2 overflows used for transmit clock.

Bit3: EXEN2: Timer 2 External Enable.
Enables high-to-low transitions on T2EX to trigger captures or reloads when Timer 2 is not operating in Baud Rate Generator mode.
0: High-to-low transitions on T2EX ignored.
1: High-to-low transitions on T2EX cause a capture or reload.

Bit2: TR2: Timer 2 Run Control.
This bit enables/disables Timer 2.
0: Timer 2 disabled.
1: Timer 2 enabled.

Bit1: C/T2: Counter/Timer Select.
0: Timer Function: Timer 2 incremented by clock defined by T2M (CKCON.5).
1: Counter Function: Timer 2 incremented by high-to-low transitions on external input pin P0.6/T2.

Bit0: CP/RL2: Capture/Reload Select.
This bit selects whether Timer 2 functions in capture or auto-reload mode. EXEN2 must be logic 1 for high-to-low transitions on T2EX to be recognized and used to trigger captures or reloads. If RCLK or TCLK is set, this bit is ignored and Timer 2 will function in auto-reload mode.
0: Auto-reload on Timer 2 overflow or high-to-low transition at T2EX (EXEN2 = 1).
1: Capture on high-to-low transition at T2EX (EXEN2 = 1).

JTAG Register Definition 18.4. FLASHDAT: JTAG Flash Data

										Reset Value
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0	FAIL	BUSY	0000000000
Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This register is used to read or write data to the Flash memory across the JTAG interface.

Bits9–2: DATA7–0: Flash Data Byte.
Bit1: FAIL: Flash Fail Bit.
- 0: Previous Flash memory operation was successful.
- 1: Previous Flash memory operation failed. Usually indicates the associated memory location was locked.

Bit0: BUSY: Flash Busy Bit.
- 0: Flash interface logic is not busy.
- 1: Flash interface logic is processing a request. Reads or writes while BUSY = 1 will not initiate another operation

JTAG Register Definition 18.5. FLASHSCL: JTAG Flash Scale

								Reset Value
FOSE	FRAE	-	-	FLSCL3	FLSCL2	FLSCL1	FLSCL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This register controls the Flash read timing circuit and the prescaler required to generate the correct timing for Flash operations.

Bit7: FOSE: Flash One-Shot Enable Bit.
- 0: Flash read strobe is a full clock-cycle wide.
- 1: Flash read strobe is 50nsec.

Bit6: FRAE: Flash Read Always Bit.
- 0: The Flash output enable and sense amplifier enable are on only when needed to read the Flash memory.
- 1: The Flash output enable and sense amplifier enable are always on. This can be used to limit the variations in digital supply current due to switching the sense amplifiers, thereby reducing digitally induced noise.

Bits5–4: UNUSED. Read = 00b, Write = don't care.

Bits3–0: FLSCL3–0: Flash Prescaler Control Bits.
The FLSCL3–0 bits control the prescaler used to generate timing signals for Flash operations. Its value should be written before any Flash write or erase operations are initiated. The value written should be the smallest integer for which:

FLSCL[3:0] > log2(fSYSCLK / 50kHz)

Where fSYSCLK is the system clock frequency. All Flash read/write/erase operations are disallowed when FLSCL[3:0] = 1111b.