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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 25MHz |
| Connectivity | SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 32x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-TQFP |
| Supplier Device Package | 48-TQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/c8051f220-gqr |

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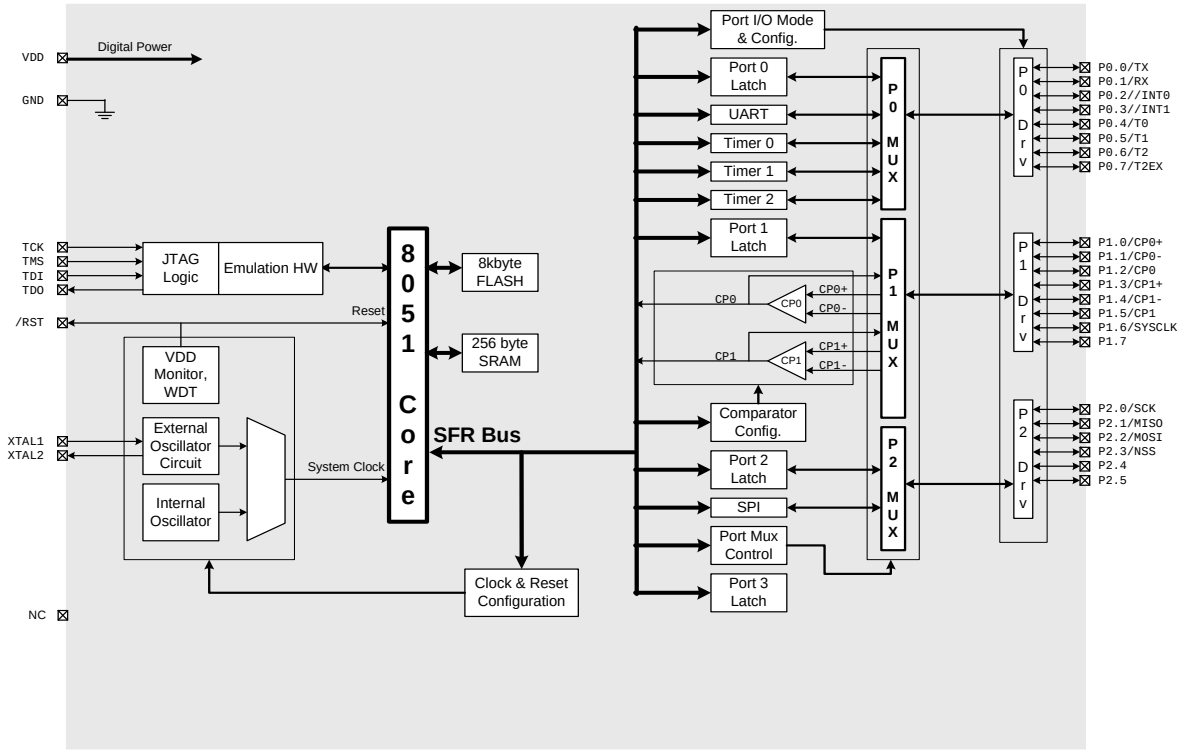



**Figure 1.4. C8051F231 Block Diagram (32 LQFP)**

## 1.1. CIP-51™ Microcontroller Core

### 1.1.1. Fully 8051 Compatible

The C8051F206, C8051F220/1/6 and C8051F230/1/6 utilize Silcon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set. Standard 803x/805x assemblers and compilers can be used to develop software. The core contains the peripherals included with a standard 8052, including three 16-bit counter/timers, a full-duplex UART, 256 bytes of internal RAM, an optional 1024 bytes of XRAM, 128 byte Special Function Register (SFR) address space, and four byte-wide I/O Ports.

### 1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The number of instructions versus the system clock cycles to execute them is as follows:

| **Instructions** | 26 | 50 | 5 | 14 | 7 | 3 | 1 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|
| **Clocks to Execute** | 1 | 2 | 2/3 | 3 | 3/4 | 4 | 4/5 | 5 | 8 |

# 2. Absolute Maximum Ratings

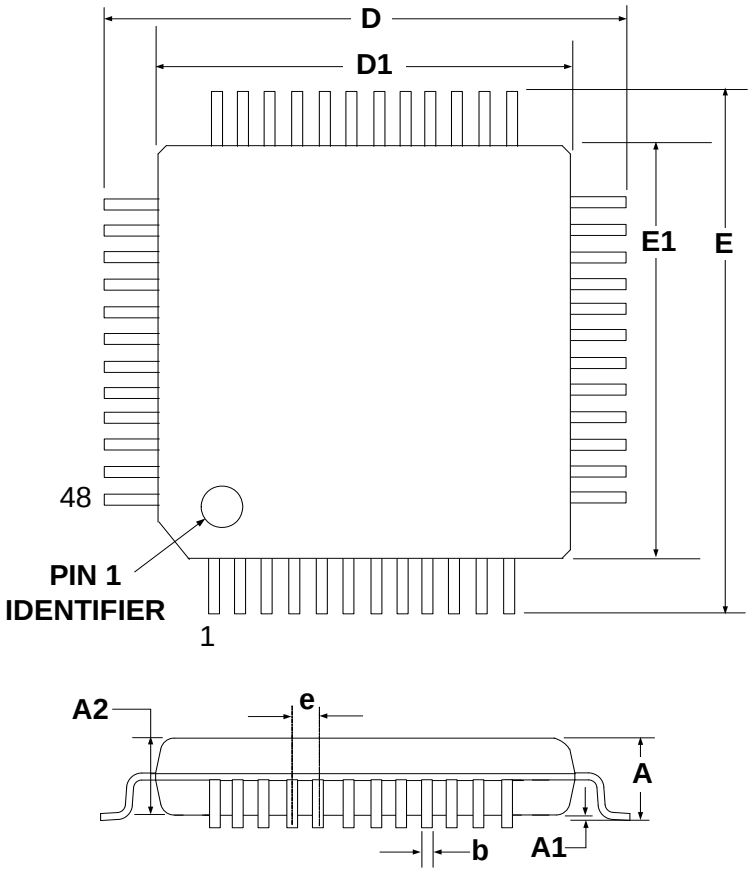
## Table 2.1. Absolute Maximum Ratings*

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Ambient Temperature under Bias | | –55 | — | 125 | °C |
| Storage Temperature | | –65 | — | 150 | °C |
| Voltage on any Pin (except $V_{DD}$ and Port I/O) with respect to DGND | | –0.3 | — | $V_{DD}$ + 0.3 | V |
| Voltage on any Port I/O Pin or $\overline{RST}$ pins with respect to DGND | | –0.3 | — | 5.8 | V |
| Voltage on $V_{DD}$ with respect to DGND | | –0.3 | | 4.2 | V |
| Total Power Dissipation | | — | 1.0 | 800 | W |
| Maximum Output Current Sunk by any Port pin | | — | — | 200 | mA |
| Maximum Output Current Sunk by any other I/O pin | | — | — | 25 | mA |
| Maximum Output Current Sourced by any Port pin | | — | — | 200 | mA |
| Maximum Output Current Sourced by any other I/O pin | | — | — | 25 | mA |

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 4.1. Pin Definitions (Continued)**

| Name | 'F206, F220, 226, 230, 236 | 'F221, 231 | Type | Description |
|---|---|---|---|---|
| | 48-Pin | 32-Pin | | |
| P2.7 | 18 | | D I/O<br>A In | Port2 Bit7. (See the Port I/O Sub-System section for complete description). |
| P3.0 | 44 | | D I/O<br>A In | Port3 Bit0. (See the Port I/O Sub-System section for complete description). |
| P3.1 | 43 | | D I/O<br>A In | Port3 Bit1. (See the Port I/O Sub-System section for complete description). |
| P3.2 | 42 | | D I/O<br>A In | Port3 Bit2. (See the Port I/O Sub-System section for complete description). |
| P3.3 | 41 | | D I/O<br>A In | Port3 Bit3. (See the Port I/O Sub-System section for complete description). |
| P3.4 | 30 | | D I/O<br>A In | Port3 Bit4. (See the Port I/O Sub-System section for complete description). |
| P3.5 | 29 | | D I/O<br>A In | Port3 Bit5. (See the Port I/O Sub-System section for complete description). |
| P3.6 | 20 | | D I/O<br>A In | Port3 Bit6. (See the Port I/O Sub-System section for complete description). |
| P3.7 | 19 | | D I/O<br>A In | Port3 Bit7. (See the Port I/O Sub-System section for complete description). |




| | MIN (mm) | NOM (mm) | MAX (mm) |
|---|---|---|---|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| D | - | 9.00 | - |
| D1 | - | 7.00 | - |
| e | - | 0.50 | - |
| E | - | 9.00 | - |
| E1 | - | 7.00 | - |

**Figure 4.3. TQFP-48 Package Drawing**

### SFR Definition 5.4. ADC0H: ADC Data Word (‘F220/1/6 and ‘F206)

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| MSB | | | | | | | LSB | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xBF |

Bits7–0: ADC Data Word Bits

**EXAMPLE**: ADC Data Word Conversion Map

| AIN – GND(Volts) | ADC0H |
|---|---|
| REF x (255/256) | 0xFF |
| REF x ½ | 0x80 |
| REF x (127/256) | 0x7F |
| 0 | 0x00 |

## 5.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH and ADC0LTH).

### SFR Definition 5.5. ADC0GTH: ADC Greater-Than Data (‘F220/1/6 and ‘F206)

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 11111111 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xC5 |

Bits7–0:
The high byte of the ADC Greater-Than Data Word.

### SFR Definition 5.6. ADC0LTH: ADC Less-Than Data Byte (‘F220/1/6 and ‘F206)

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xC7 |

Bits7–0:
The high byte of the ADC Less-Than Data Word.

## Table 5.1. 8-Bit ADC Electrical Characteristics

VDD = 3.0 V, VREF = 2.40 V, PGA Gain = 1, –40 to +85 ×C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **DC Accuracy** | | | | | |
| Resolution | | — | 8 | — | bits |
| Integral Nonlinearity | | — | — | ±1/2 | LSB |
| Differential Nonlinearity | Guaranteed Monotonic | — | — | ±1/2 | LSB |
| Offset Error | | ±2 | — | ±1/2 | LSB |
| Gain Error | | ±2 | — | ±1/2 | LSB |
| Offset Temperature Coefficient | | | ±0.25 | — | ppm/°C |
| **Dynamic Performance** (10 kHz sine-wave input, 0 to –1 dB of full scale, 100 ksps) | | | | | |
| Signal-to-Noise Plus Distortion | | 49.5 | — | — | dB |
| Total Harmonic Distortion | Up to the 5$^{th}$ harmonic | –60 | –65 | — | dB |
| Spurious-Free Dynamic Range | | — | –65 | — | dB |
| **Conversion Rate** | | | | | |
| Conversion Time in SAR Clocks | | 16 | — | — | clocks |
| SAR Clock Frequency | | | — | 2.5 | MHz |
| Track/Hold Acquisition Time | | 1.5 | — | — | µs |
| Throughput Rate | | — | — | 100 | ksps |
| **Analog Inputs** | | | | | |
| Input Voltage Range | | 0 | — | $V_{DD}$ | V |
| Input Capacitance | | — | 10 | — | pF |
| **Power Specifications** | | | | | |
| Power Supply Current | Operating Mode, 100 ksps | — | 0.45 | 1.0 | mA |
| Power Supply Current in Shutdown | | — | 0.1 | 1 | µA |
| Power Supply Rejection | | — | ±0.3 | — | mV/V |

# 6. ADC (12-Bit, C8051F206 Only)

**Description**

The ADC subsystem for the C8051F206 consists of configurable analog multiplexer (AMUX), a programmable gain amplifier (PGA), and a 100ksps, 12-bit successive-approximation-register ADC with integrated track-and-hold and programmable window detector (see Figure 6.1). The AMUX, PGA, Data Conversion Modes, and Window Detector are all configurable under software control via the Special Function Register's shown in Figure 6.1. The ADC subsystem (ADC, track-and-hold and PGA) is enabled only when the ADCEN bit in the ADC Control register (ADC0CN, Figure 6.5) is set to 1. The ADC subsystem is in low power shutdown when this bit is 0.

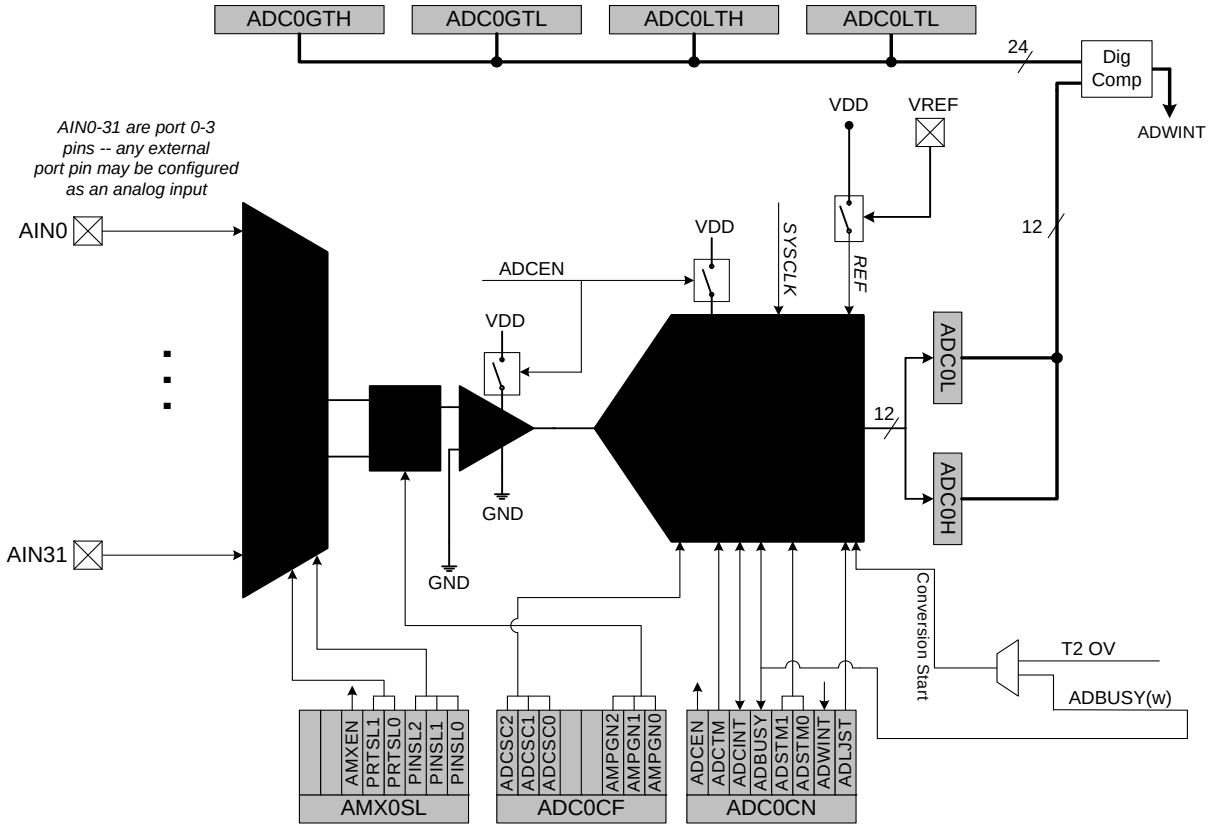



**Figure 6.1. 12-Bit ADC Functional Block Diagram**

## 6.1. Analog Multiplexer and PGA

Any external port pin (ports 0-3) may be selected via software. The AMX0SL SFR is used to select the desired analog input pin. (See SFR Definition 5.1). When the AMUX is enabled, the user selects which port is to be used (bits PRTSL0–1), and then the pin in the selected port (bits PINSL0–2) to be the analog input.

The PGA amplifies the AMUX output signal by an amount determined by the states of the AMPGN2–0 bits in the ADC Configuration register, ADC0CF (SFR Definition 5.2). The PGA can be software-programmed for gains of 0.5, 1, 2, 4, 8 or 16. It defaults to a gain of 1 on reset.

**Table 9.4. Interrupt Summary (Continued)**

| Interrupt Source | Interrupt Vector | Priority Order | Interrupt-Pending Flag | Enable |
|---|---|---|---|---|
| ADC0 End of Conversion | 0x007B | 15 | ADCINT (ADC0CN.5) | EADC0 (EIE2.1) |
| Software Controlled Interrupt 0 | 0x0083 | 16 | SCI0 (SWCINT.4) | ESCI0 (EIE2.2) |
| Software Controlled Interrupt 1 | 0x008B | 17 | SCI1 (SWCINT.5) | ESCI1 (EIE2.3) |
| Software Controlled Interrupt 2 | 0x0093 | 18 | SCI2 (SWCINT.6) | ESCI2 (EIE2.4) |
| Software Controlled Interrupt 3 | 0x009B | 19 | SCI3 (SWCINT.7) | ESCI3 (EIE2.5) |
| Unused Interrupt Location | 0x00A3 | 20 | None | Reserved (EIE2.6) |
| External Crystal OSC Ready | 0x00AB | 21 | XTLVLD (OSCXCN.7) | EXVLD (EIE2.7) |

### 9.4.4. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP–EIP2) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate.

### 9.4.5. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. NOTE: If a Flash write or erase is performed, the MCU is stalled during the operation and interrupts will not be serviced until the operation is complete. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

## 11. On-Chip XRAM (C8051F206/226/236)

The C8051F206/226/236 features 1024 Bytes of RAM mapped into the external data memory space. All address locations may be accessed using the external move instruction (MOVX) and the data pointer (DPTR), or using indirect MOVX addressing mode. If the MOVX instruction is used with an 8-bit operand (such as @R1), then the high byte is the External Memory Interface Control Register (EMI0CN, shown in SFR Definition 11.1). Addressing using 8 bits will map to one of four 256-byte pages, and these pages are selected by setting the PGSEL bits in the EMI0CN register.

NOTE: The MOVX instruction is also used for write to the Flash memory. Please see section 10 for details. The MOVX instruction will access XRAM by default.

For any of the addressing modes, the upper 6 bits of the 16-bit external data memory address word are "don't cares". As a result, the 1024-byte RAM is mapped modulo style ("wrap around") over the entire 64k of possible address values. For example, the XRAM byte at address 0x0000 is also at address 0x0400, 0x0800, 0x0C00, 0x1000, etc. This feature is useful when doing a linear memory fill, as the address pointer does not have to be reset when reaching the RAM block boundary.

### SFR Definition 11.1. EMI0CN: External Memory Interface Control

| R | R | R | R | R | R | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | PGSEL1 | PGSEL0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xAF |

Bits7–2: Not Used -read only 000000b
Bits1–0: XRAM Page Select Bits PGSEL[1:0]
The XRAM Page Select bits provide the high byte of the 16-bit external memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. The upper 6 bits are "don't cares", so the 1k address blocks are repeated modulo over the entire data memory address space.
00:0x000 – 0x0FF
01:0x100 – 0x1FF
10:0x200 – 0x2FF
11:0x300 – 0x3FF

## SFR Definition 12.2. RSTSRC: Reset Source

| | R | R/W | R/W | R | R | R/W | R | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | | C0RSEF | SWRSEF | WDTRSF | MCDRSF | PORSF | PINRSF | xxxxxxxx |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xEF |

(Note: Do not use read-modify-write operations on this register.)

Bit7: RESERVED.
Bit6: Not Used. Read only 0b.
Bit5: C0RSEF: Comparator 0 Reset Enable and Flag
Write
0: Comparator 0 is not a reset source
1: Comparator 0 is a reset source (active low)
Read
Note: The value read from C0RSEF is not defined if Comparator 0 has not been enabled as a reset source.
0: Source of prior reset was not from Comparator 0
1: Source of prior reset was from Comparator 0
Bit4: SWRSF: Software Reset Force and Flag
Write
0: No Effect
1: Forces an internal reset. $\overline{\text{RST}}$ pin is not affected.
Read
0: Prior reset source was not from write to the SWRSF bit.
1: Prior reset source was from write to the SWRSF bit.
Bit3: WDTRSF: Watchdog Timer Reset Flag (Read only)
0: Source of prior reset was not from WDT timeout.
1: Source of prior reset was from WDT timeout.
Bit2: MCDRSF: Missing Clock Detector Flag (Read only)
0: Source of prior reset was not from Missing Clock Detector timeout.
1: Source of prior reset was from Missing Clock Detector timeout.
Bit1: PORSF: Power-On Reset Force and Flag
Write
0: No effect
1: Forces a Power-On Reset. $\overline{\text{RST}}$ is driven low.
Read
0: Source of prior reset was not from POR.
1: Source of prior reset was from POR.
Bit0: PINRSF: HW Pin Reset Flag
0: Source of prior reset was not from $\overline{\text{RST}}$ pin.
1: Source of prior reset was from $\overline{\text{RST}}$ pin.

### SFR Definition 13.1. OSCICN: Internal Oscillator Control

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| MSCLKE | - | - | IFRDY | CLKSL | IOSCEN | IFCN1 | IFCN0 | 00000100 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xB2 |

Bit7: MSCLKE: Missing Clock Enable Bit
0: Missing Clock Detector Disabled
1: Missing Clock Detector Enabled; triggers a reset if a missing clock is detected
Bits6–5: UNUSED. Read = 00b, Write = don't care
Bit4: IFRDY: Internal Oscillator Frequency Ready Flag
0: Internal Oscillator Frequency not running at speed specified by the IFCN bits.
1: Internal Oscillator Frequency running at speed specified by the IFCN bits.
Bit3: CLKSL: System Clock Source Select Bit
0: Uses Internal Oscillator as System Clock.
1: Uses External Oscillator as System Clock.
Bit2: IOSCEN: Internal Oscillator Enable Bit
0: Internal Oscillator Disabled
1: Internal Oscillator Enabled
Bits1–0: IFCN1-0: Internal Oscillator Frequency Control Bits
00: Internal Oscillator typical frequency is 2 MHz.
01: Internal Oscillator typical frequency is 4 MHz.
10: Internal Oscillator typical frequency is 8 MHz.
11: Internal Oscillator typical frequency is 16 MHz.

### Table 13.1. Internal Oscillator Electrical Characteristics

–40 to +85 ×C unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Internal Oscillator Frequency | OSCICN.[1:0] = 00<br>OSCICN.[1:0] = 01<br>OSCICN.[1:0] = 10<br>OSCICN.[1:0] = 11 | 1.5<br>3.0<br>6.0<br>12 | 2.0<br>4.0<br>8.0<br>16 | 2.5<br>5.0<br>10<br>20 | MHz |
| Internal Oscillator Current Consumption | OSCICN.2 = 1 | — | 200 | — | µA |
| Internal Oscillator Temperature Stability | | — | 4 | — | ppm/°C |
| Internal Oscillator Power Supply ($V_{DD}$) Stability | | — | 6.4 | — | %/V |

## SFR Definition 13.2. OSCXCN: External Oscillator Control

| R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| XTLVLD | XOSCMD2 | XOSCMD1 | XOSCMD0 | - | XFCN2 | XFCN1 | XFCN0 | 00110000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xB1 |

Bit7: XTLVLD: Crystal Oscillator Valid Flag
(Valid only when XOSCMD = 1xx.)
0: Crystal Oscillator is unused or not yet stable
1: Crystal Oscillator is running and stable

Bits6–4: XOSCMD2–0: External Oscillator Mode Bits
00x: Off. XTAL1 pin is grounded internally.
010: System Clock from External CMOS Clock on XTAL1 pin.
011: System Clock from External CMOS Clock on XTAL1 pin divided by 2.
10x: RC/C Oscillator Mode with divide by 2 stage.
110: Crystal Oscillator Mode
111: Crystal Oscillator Mode with divide by 2 stage.

Bit3: RESERVED. Read = undefined, Write = don't care

Bits2–0: XFCN2–0: External Oscillator Frequency Control Bits
000–111: see table below

| XFCN | Crystal (XOSCMD = 11x) | RC (XOSCMD = 10x) | C (XOSCMD = 10x) |
|---|---|---|---|
| 000 | f ≤ 12.5 kHz | f ≤ 25 kHz | K Factor = 0.44 |
| 001 | 12.5 kHz < f ≤ 30.3 kHz | 25 kHz < f ≤ 50 kHz | K Factor = 1.4 |
| 010 | 30.35 kHz < f ≤ 93.8 kHz | 50 kHz < f ≤ 100 kHz | K Factor = 4.4 |
| 011 | 93.8 kHz < f ≤ 26 7kHz | 100 kHz < f ≤ 200 kHz | K Factor = 13 |
| 100 | 267 kHz < f ≤ 722 kHz | 200 kHz < f ≤ 400 kHz | K Factor = 38 |
| 101 | 722 kHz < f ≤ 2.23 MHz | 400 kHz < f ≤ 800 kHz | K Factor = 100 |
| 110 | 2.23 MHz < f ≤ 6.74 MHz | 800 kHz < f ≤ 1.6 MHz | K Factor = 420 |
| 111 | f > 6.74 MHz | 1.6 MHz < f ≤ 3.2 MHz | K Factor = 1400 |

**CRYSTAL MODE** (Circuit from Figure 13.1, Option 1; XOSCMD = 11x)
Choose XFCN value to match the crystal frequency.

**RC MODE** (Circuit from Figure 13.1, Option 2; XOSCMD = 10x)
Choose oscillation frequency range where:
**$f = 1.23(10^3) / (R \times C)$**, where
f = frequency of oscillation in MHz
C = capacitor value in pF
R = Pull-up resistor value in kΩ

**C MODE** (Circuit from Figure 13.1, Option 3; XOSCMD = 10x)
Choose K Factor (KF) for the oscillation frequency desired:
**$f = KF / (C \times AV+)$**, where
f = frequency of oscillation in MHz
C = capacitor value on XTAL1, XTAL2 pins in pF
$V_{DD}$ = Power supply voltage on MCU in volts

### SFR Definition 14.2. PRT1MX: Port I/O MUX Register 1

| R | R/W | R | R | R | R | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| - | SYSCKE | - | - | - | - | CP1OEN | CP0OEN | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xE2 |

Bit7: UNUSED. Read = 0.
Bit6: SYSCKE: SYSCLK Output Enable Bit
0: SYSCLK unavailable at the port pin.
1: SYSCLK output routed to pin P1.6
Bits 5–2: UNUSED. Read = 0000b, Write = don't care.
Bit1: CP1OEN: Comparator 1 Output Enable bit.
0: CP1 unavailable at Port pin.
1: CP1 routed to Port Pin P1.5.
Bit0: CP0OEN: Comparator 0 Output Enable Bit
0: CP0 unavailable at port pin.
1: CP0 routed to port pin P1.2.

### SFR Definition 14.3. PRT2MX: Port I/O MUX Register 2

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| GWPUD | P3WPUD | P2WPUD | P1WPUD | P0WPUD | - | - | SPI0OEN | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xE3 |

Bit 7: GWPUD: Global Port I/O Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for all ports.
1: Weak Pull-ups Disabled (Bits 6–3 Don't cares)
Bit 6: P3WPUD: Port 3 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 3
1: Weak Pull-ups Disabled for port 3
Bit 5: P2WPUD: Port 2 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 2.
1: Weak Pull-ups Disabled for port 2
Bit 4: P1WPUD: Port 1 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 1
1: Weak Pull-ups Disabled for port 1
Bit 3: P0WPUD: Port 0 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 0
1: Weak Pull-ups Disabled for port 0
Bits 2–1: UNUSED. Read = 00b, Write = don't care.
Bit 0: SPI0OEN: SPI Bus I/O Enable Bit.
0: SPI I/O unavailable at port pins.
1: SCK, MISO, MOSI, NSS routed to pins P2.0, P2.1, P2.2, and P2.3 respectively.

### SFR Definition 14.15. P3MODE: Port3 Digital/Analog Input Mode*

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 11111111 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0xF4 |

Bits7–0: Port3 Digital/Analog Output Mode
0: Corresponding Port3 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port3 pin Digital Input is enabled.

* (Available on C8051F206, C8051F220/6 and C8051F230/6)

## Table 14.1. Port I/O DC Electrical Characteristics

**$V_{DD}$ = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.**

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output High Voltage | $I_{OH}$ = –10 uA, Port I/O push-pull<br>$I_{OH}$ = –3 mA, Port I/O push-pull<br>$I_{OH}$ = –10 mA, Port I/O push-pull | $V_{DD}$ – 0.1<br>$V_{DD}$ – 0.7 | <br><br>$V_{DD}$ – 0.8 | | V |
| Output Low Voltage | $I_{OL}$ = 10 uA<br>$I_{OL}$ = 8.5 mA<br>$I_{OL}$ = 25 mA | | <br><br>1.0 | 0.1<br>0.6 | V |
| Input High Voltage | | 0.7 x $V_{DD}$ | | | V |
| Input Low Voltage | | | | 0.3 x $V_{DD}$ | V |
| Input Leakage Current | DGND < Port Pin < $V_{DD}$, Pin Tri-state<br>Weak Pull-up Off<br>Weak Pull-up On | | <br><br>30 | ±1 | µA |
| Capacitive Loading | | | 3 | | pF |

## SFR Definition 17.1. TCON: Timer Control

| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | Reset Value |
|---|---|---|---|---|---|---|---|---|
| TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00000000 |
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | SFR Address: 0x88 |

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 input signal's logic level when IT1 = 0.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT1 is level triggered.
1: /INT1 is edge triggered.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 input signal's logic level when IT0 = 0.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT0 is level triggered.
1: /INT0 is edge triggered.

## 17.2. Timer 2

Timer 2 is a 16-bit counter/timer formed by the two 8-bit SFR's: TL2 (low byte) and TH2 (high byte). As with Timers 0 and 1, Timer 2 can use either the system clock or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/T2 bit (T2CON.1) selects the clock source for Timer 2. Clearing C/T2 selects the system clock as the input for the timer (divided by either one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to 1, high-to-low transitions at the T2 input pin increment the counter/timer register. (Refer to Section 14 for information on selecting and configuring external I/O pins.) Timer 2 can also be used to start an ADC Data Conversion (see section 5).

Timer 2 offers capabilities not found in Timer 0 and Timer 1. It operates in one of three modes: 16-bit Counter/Timer with Capture, 16-bit Counter/Timer with Auto-Reload or Baud Rate Generator Mode. Timer 2's operating mode is selected by setting configuration bits in the Timer 2 Control (T2CON) register. Below is a summary of the Timer 2 operating modes and the T2CON bits used to configure the counter/timer. Detailed descriptions of each mode follow.

| RCLK | TCLK | CP/RL2 | TR2 | Mode |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 16-bit Counter/Timer with Capture |
| 0 | 0 | 0 | 1 | 16-bit Counter/Timer with Auto-Reload |
| 0 | 1 | X | 1 | Baud Rate Generator for TX |
| 1 | 0 | X | 1 | Baud Rate Generator for RX |
| 1 | 1 | X | 1 | Baud Rate Generator for TX and RX |
| X | X | X | 0 | Off |

### 17.2.2. Mode 1: 16-bit Counter/Timer with Auto-Reload

The Counter/Timer with Auto-Reload mode sets the TF2 timer overflow flag when the counter/timer register overflows from 0xFFFF to 0x0000. An interrupt is generated if enabled. On overflow, the 16-bit value held in the two capture registers (RCAP2H, RCAP2L) is automatically loaded into the counter/timer register and the timer is restarted.

Counter/Timer with Auto-Reload mode is selected by clearing the CP/RL2 bit. Setting TR2 to logic 1 enables and starts the timer. Timer 2 can use either the system clock or transitions on an external input pin as its clock source, as specified by the C/T2 bit. If EXEN2 is set to logic 1, a high-to-low transition on T2EX will also cause Timer 2 to be reloaded. If EXEN2 is cleared, transitions on T2EX will be ignored.

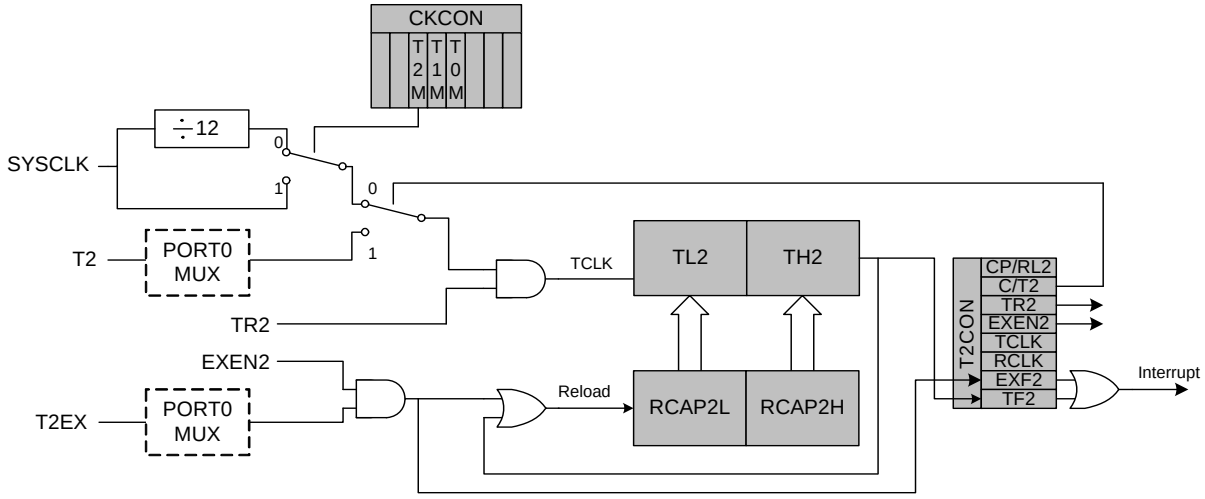



**Figure 17.5. T2 Mode 1 Block Diagram**

## JTAG Register Definition 18.2. FLASHCON: JTAG Flash Control

| WRMD3 | WRMD2 | WRMD1 | WRMD0 | RDMD3 | RDMD2 | RDMD1 | RDMD0 | Reset Value |
|---|---|---|---|---|---|---|---|---|
| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | 00000000 |

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bits7–4: WRMD3–0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
- 0000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
- 0001: A FLASHDAT write initiates a write of FLASHDAT into the memory address selected by the FLASHADR register. FLASHADR is incremented by one when complete.
- 0010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. FLASHDAT must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR = 0x1DFE – 0x1DFF, the entire user space will be erased (i.e. entire Flash memory except for Reserved area 0x1E00 – 0x1FFF).

(All other values for WRMD3–0 are reserved.)

Bits3–0: RDMD3–0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
- 0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
- 0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
- 0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.

(All other values for RDMD3–0 are reserved.)

## JTAG Register Definition 18.3. FLASHADR: JTAG Flash Address

| | | | | | | | | | | | | | | | | Reset Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | 0x0000 |
| Bit15 | | | | | | | | | | | | | | | Bit0 | |

This register holds the address for all JTAG Flash read, write, and erase operations. This register autoincrements after each read or write, regardless of whether the operation succeeded or failed.

Bits15–0: Flash Operation 16-bit Address.

## 18.2. Boundary Scan Bypass and ID Code

The MCU does not support boundary scan (IEEE 1149.1), however, it does support the bypass and ID code functions. Because the MCU utilizes JTAG for Flash memory programming and debug support, and other devices in a system may use JTAG boundary scan, the MCU supports being placed in BYPASS so the user may maintain a single JTAG port for a system. Additionally, the MCU supports an ID code.

### 18.2.1. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard 1-bit JTAG Bypass data register.

### 18.2.2. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

**JTAG Register Definition 18.6. DEVICEID: JTAG Device ID**

| Version | Part Number | Manufacturer ID | 1 | Reset Value |
|---|---|---|---|---|
| Bit31 Bit28 | Bit27 Bit12 | Bit11 Bit1 | Bit0 | 0xn0000243 |

Version = 0000b (Revision A)
= 0001b (Revision B)

Part Number = 0000 0000 0000 0001b (C8051F206/220/1/6, C8051F230/1/6)

Manufacturer ID = 0010 0100 001b (Silicon Laboratories)

## 18.3. Debug Support

The MCU has on-chip JTAG and debug circuitry that provide non-intrusive, full speed, in-circuit debug using the production part installed in the end application using the four pin JTAG I/F. Silicon Labs' debug system supports inspection and modification of memory and registers, breakpoints, stack tracing, and single stepping. No additional target RAM, program memory, or communications channels are required. All the digital and analog peripherals are functional and work correctly (remain in sync) while emulating. The WDT is disabled when the MCU is halted during single stepping or at a breakpoint.

The C8051F2xxDK is a development kit with all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8061F206, C8051F220/1/6 and C8051F230/1/6. The kit includes an Integrated Development Environment (IDE) which has a debugger and integrated 8051 assembler. It has an RS-232 to JTAG interface module referred to as the EC. The kit also includes RS-232 and JTAG cables, and wall-mount power supply.