Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 32x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f220

9.5. Power Management Modes 83
9.5.1. Idle Mode 83
9.5.2. Stop Mode 83
10. Flash Memory 85
10.1. Programming The Flash Memory 85
10.2. Security Options 86
11. On-Chip XRAM (C8051F206/226/236) 90
12. Reset Sources 91
12.1. Power-on Reset 92
12.2. Software Forced Reset 92
12.3. Power-fail Reset 92
12.4. External Reset 93
12.5. Missing Clock Detector Reset 93
12.6. Comparator 0 Reset 93
12.7. Watchdog Timer Reset 93
12.7.1. Watchdog Usage 93
13. Oscillator 97
13.1. External Crystal Example 100
13.2. External RC Example 100
13.3. External Capacitor Example 100
14. Port Input/Output 101
14.1. Port I/O Initialization 101
14.2. General Purpose Port I/O 105
15. Serial Peripheral Interface Bus 110
15.1. Signal Descriptions 111
15.1.1. Master Out, Slave In 111
15.1.2. Master In, Slave Out 111
15.1.3. Serial Clock 111
15.1.4. Slave Select 111
15.2. Serial Clock Timing 113
15.3. SPI Special Function Registers 113
16. UART 117
16.1. UART Operational Modes 118
16.1.1. Mode 0: Synchronous Mode 118
16.1.2. Mode 1: 8-Bit UART, Variable Baud Rate 119
16.1.3. Mode 2: 9-Bit UART, Fixed Baud Rate 121
16.1.4. Mode 3: 9-Bit UART, Variable Baud Rate 121
16.2. Multiprocessor Communications 122
17. Timers 125
17.1. Timer 0 and Timer 1 125
17.1.1. Mode 0: 13-bit Counter/Timer 125
17.1.2. Mode 1: 16-bit Counter/Timer 126
17.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload 127
17.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only) 128

SFR Definition 14.4. P0: Port0 Register 105
SFR Definition 14.5. PRT0CF: Port0 Configuration Register 105
SFR Definition 14.6. P0MODE: Port0 Digital/Analog Input Mode 106
SFR Definition 14.7. P1: Port1 Register 106
SFR Definition 14.8. PRT1CF: Port1 Configuration Register 106
SFR Definition 14.9. P1MODE: Port1 Digital/Analog Input Mode 107
SFR Definition 14.10. P2: Port2 Register 107
SFR Definition 14.11. PRT2CF: Port2 Configuration Register 107
SFR Definition 14.12. P2MODE: Port2 Digital/Analog Input Mode 108
SFR Definition 14.13. P3: Port3 Register* 108
SFR Definition 14.14. PRT3CF: Port3 Configuration Register* 108
SFR Definition 14.15. P3MODE: Port3 Digital/Analog Input Mode* 109
SFR Definition 15.1. SPI0CFG: SPI Configuration 114
SFR Definition 15.2. SPI0CN: SPI Control 115
SFR Definition 15.3. SPI0CKR: SPI Clock Rate Register 116
SFR Definition 15.4. SPI0DAT: SPI Data Register 116
SFR Definition 16.1. SBUF: Serial (UART) Data Buffer 123
SFR Definition 16.2. SCON: Serial Port Control 124
SFR Definition 17.1. TCON: Timer Control 129
SFR Definition 17.2. TMOD: Timer Mode 130
SFR Definition 17.3. CKCON: Clock Control 131
SFR Definition 17.4. TL0: Timer 0 Low Byte 132
SFR Definition 17.5. TL1: Timer 1 Low Byte 132
SFR Definition 17.6. TH0: Timer 0 High Byte 132
SFR Definition 17.7. TH1: Timer 1 High Byte 132
SFR Definition 17.8. T2CON: Timer 2 Control 137
SFR Definition 17.9. RCAP2L: Timer 2 Capture Register Low Byte 138
SFR Definition 17.10. RCAP2H: Timer 2 Capture Register High Byte 138
SFR Definition 17.11. TL2: Timer 2 Low Byte 138
SFR Definition 17.12. TH2: Timer 2 High Byte 138
JTAG Register Definition 18.1. IR: JTAG Instruction 139
JTAG Register Definition 18.2. FLASHCON: JTAG Flash Control 141
JTAG Register Definition 18.3. FLASHADR: JTAG Flash Address 141
JTAG Register Definition 18.4. FLASHDAT: JTAG Flash Data 142
JTAG Register Definition 18.5. FLASHSCL: JTAG Flash Scale 142
JTAG Register Definition 18.6. DEVICEID: JTAG Device ID 143

1. System Overview

The C8051F2xx is a family of fully integrated, mixed-signal System on a Chip MCU's available with a true 12-bit ('F206) multi-channel ADC, 8-bit multi-channel ADC ('F220/1/6 and 'F206), or without an ADC ('F230/1/6). Each model features an 8051-compatible microcontroller core with 8 kB of Flash memory. There are also UART and SPI serial interfaces implemented in hardware (not "bit-banged" in user software). Products in this family feature 22 or 32 general purpose I/O pins, some of which can be used for assigned digital peripheral interface. Any pins may be configured for use as analog input to the analog-to-digital converter ('F220/1/6 and 'F206 only). (See the Product Selection Guide in Table 1.1 for a quick reference of each MCUs' feature set.)

Other features include an on-board V_{DD} monitor, WDT, and clock oscillator. On-board Flash memory can be reprogrammed in-circuit, and may also be used for non-volatile data storage. Integrated peripherals can also individually shut down any or all of the peripherals to conserve power. All parts have 256 bytes of SRAM. Also, an additional 1024 bytes of RAM is available in the 'F206/226/236.

On-board JTAG debug support allows non-intrusive (uses no on-chip resources), full speed, in-circuit debug using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional when emulating using JTAG.

Each MCU is specified for 2.7 to 3.6 V operation over the industrial temperature range (45 to +85 ℃) and is available in the 48-pin TFQP and 32-pin LFQP. The Port I/Os are tolerant for input signals up to 5 V.

Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	SPI	UART	Timers (16-bit)	Digital Port I/O s	ADC Resolution (bits)	ADC Max Speed (ksps)	ADC Inputs	Voltage Comparators	Package
C8051F206	25	8 k	1280	✓	✓	3	32	12	100	32	2	48TQFP
C8051F220	25	8 k	256	✓	✓	3	32	8	100	32	2	48TQFP
C8051F221	25	8 k	256	✓	✓	3	22	8	100	22	2	32LQFP
C8051F226	25	8 k	1280	✓	✓	3	32	8	100	32	2	48TQFP
C8051F230	25	8 k	256	✓	✓	3	32				2	48TQFP
C8051F231	25	8 k	256	✓	✓	3	22				2	32LQFP
C8051F236	25	8 k	1280	✓	✓	3	32				2	48TQFP

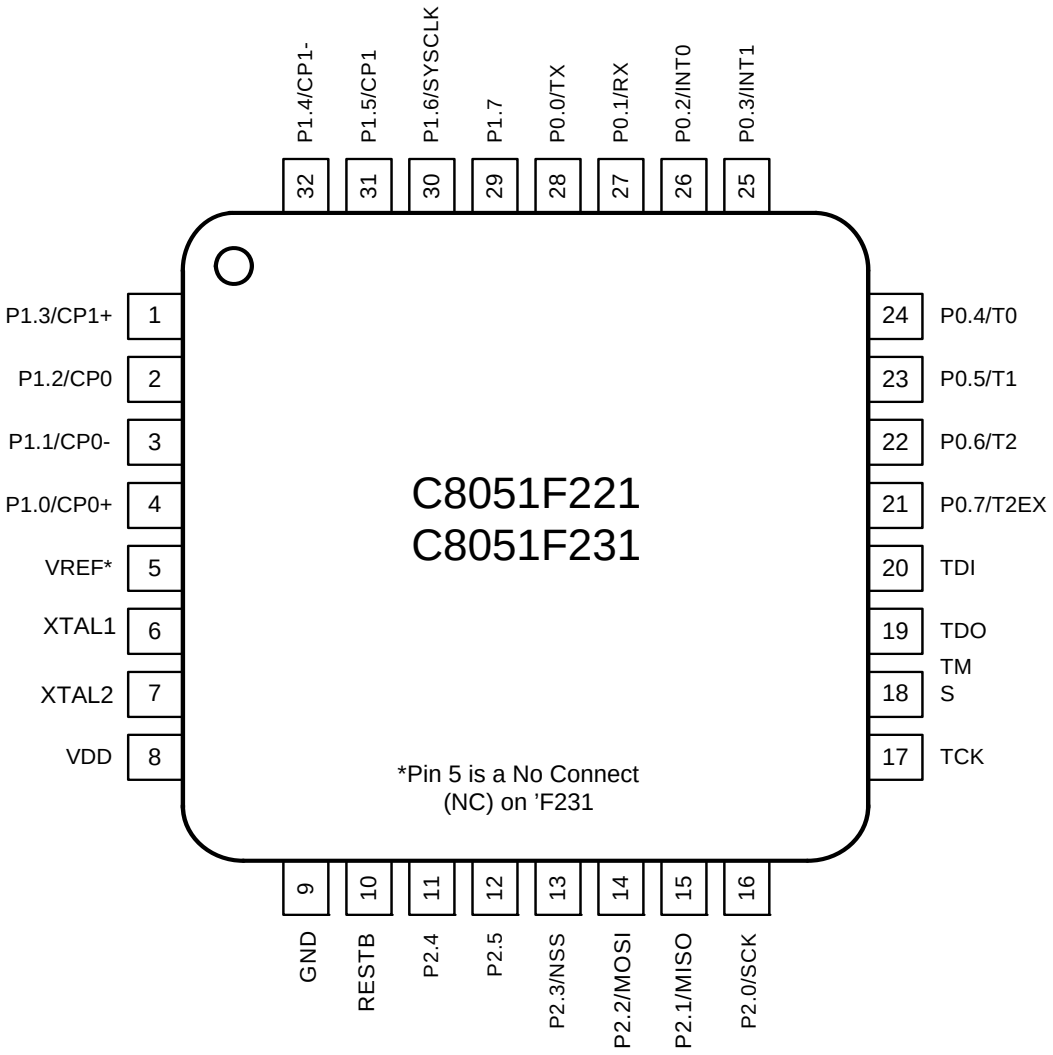

Figure 4.2. LQFP-32 Pin Diagram

Table 5.1. 8-Bit ADC Electrical Characteristics

VDD = 3.0 V, VREF = 2.40 V, PGA Gain = 1, 40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			8		bits
Integral Nonlinearity				–1/2	LSB
Differential Nonlinearity	Guaranteed Monotonic			–1/2	LSB
Offset Error		–2		–1/2	LSB
Gain Error		–2		–1/2	LSB
Offset Temperature Coefficient			–0.25		ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to 1 dB of full scale, 100 ksps)					
Signal-to-Noise Plus Distortion		49.5			dB
Total Harmonic Distortion	Up to the 5th harmonic	60	65		dB
Spurious-Free Dynamic Range			65		dB
Conversion Rate					
Conversion Time in SAR Clocks		16			clocks
SAR Clock Frequency				2.5	MHz
Track/Hold Acquisition Time		1.5			µs
Throughput Rate				100	ksps
Analog Inputs					
Input Voltage Range		0		V_{DD}	V
Input Capacitance			10		pF
Power Specifications					
Power Supply Current	Operating Mode, 100 ksps		0.45	1.0	mA
Power Supply Current in Shutdown			0.1	1	µA
Power Supply Rejection			–0.3		mV/V

9.2.5. Stack

A programmer's stack can be located anywhere in the 256-byte data memory. The stack area is designated using the Stack Pointer (SP, 0x81) SFR. The SP will point to the last location used. The next value pushed on the stack is placed at SP+1 and then SP is incremented. A reset initializes the stack pointer to location 0x07. Therefore, the first value pushed on the stack is placed at location 0x08, which is also the first register (R0) of register bank 1. Thus, if more than one register bank is to be used, the SP should be initialized to a location in the data memory not being used for data storage. The stack depth can extend up to 256 bytes.

The MCU also has built-in hardware for a stack record. The stack record is a 32-bit shift register, where each Push or increment SP pushes one record bit onto the register, and each Call pushes two record bits onto the register. (A Pop or decrement SP pops one record bit, and a Return pops two record bits, also.) The stack record circuitry can also detect an overflow or underflow on the 32-bit shift register, and can notify the emulator software even with the MCU running full-speed debug.

12. Reset Sources

The reset circuitry of the MCU allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the CIP-51 halts program execution, forces the external port pins to a known state and initializes the SFRs to their defined reset values. Interrupts and timers are disabled. On exit, the program counter (PC) is reset, and program execution starts at location 0x0000.

All of the SFRs are reset to predefined values. The reset values of the SFR bits are defined in the SFR detailed descriptions. The contents of internal data memory are not changed during a reset and any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic ones), activating internal weak pull-ups which take the external I/O pins to a high state. The weak pull-ups are enabled during and after the reset. If the source of reset is from the V_{DD} Monitor or writing a '1' to the PORSF bit, the $\overline{RST}$ pin is driven low until the end of the V_{DD} reset timeout.

On exit from the reset state, the MCU uses the internal oscillator running at 2MHz as the system clock by default. Refer to Section 13 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval. (Section 12.7 details the use of the Watchdog Timer.) Once the system clock source is stable, program execution begins at location 0x0000.

There are six sources for putting the MCU into the reset state: power-on/power-fail (V_{DD} monitor), external $\overline{RST}$ pin, software commanded, Comparator 0, Missing Clock Detector, and Watchdog Timer. Each reset source is described below:

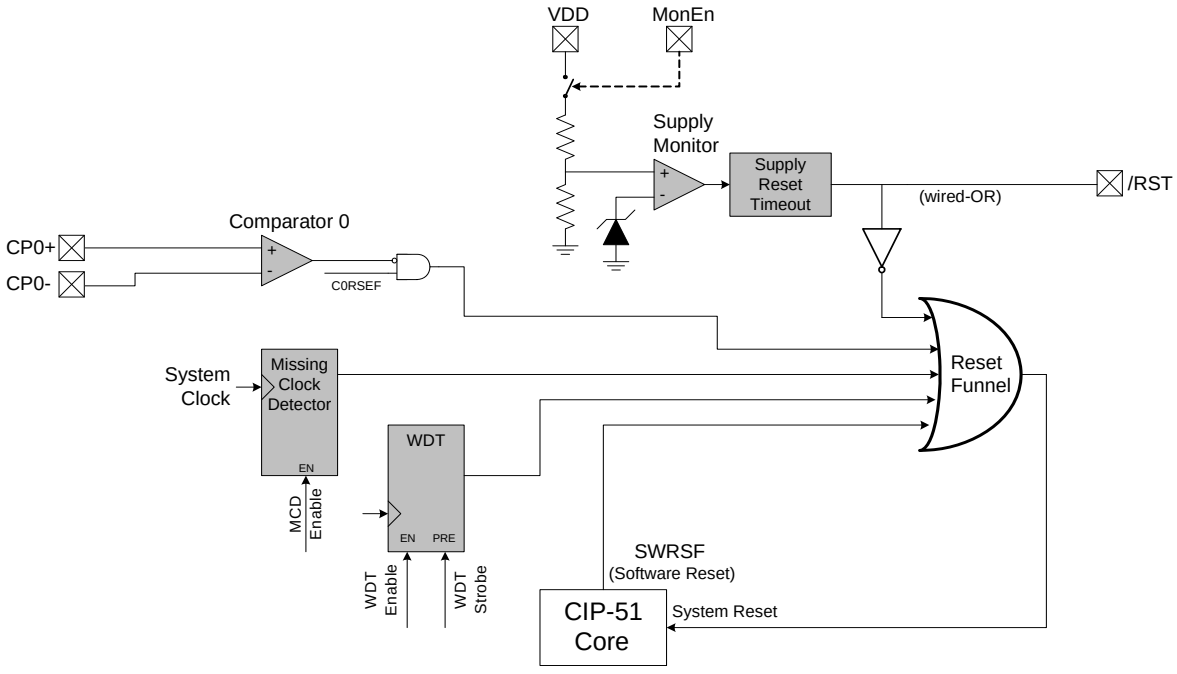

Figure 12.1. Reset Sources Diagram

SFR Definition 14.12. P2MODE: Port2 Digital/Analog Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF3

Bits7 0: Port2 Digital/Analog Output Mode
0: Corresponding Port2 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port2 pin Digital Input is enabled.

SFR Definition 14.13. P3: Port3 Register*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xB0

Bits7 0: P3.[7:0]
(Write)
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding PRT3CF.n bit = 0)
(Read)
0: P3.n is logic low.
1: P3.n is logic high.

SFR Definition 14.14. PRT3CF: Port3 Confi guration Register*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA7

Bits7 0: PRT3CF.[7:0]: Output Configurat ion Bits for P3.7 P3.0 (respectively)
0: Corresponding P3.n Output Mode is Open-Drain.
1: Corresponding P3.n Output Mode is Push-Pull.

NOTES: