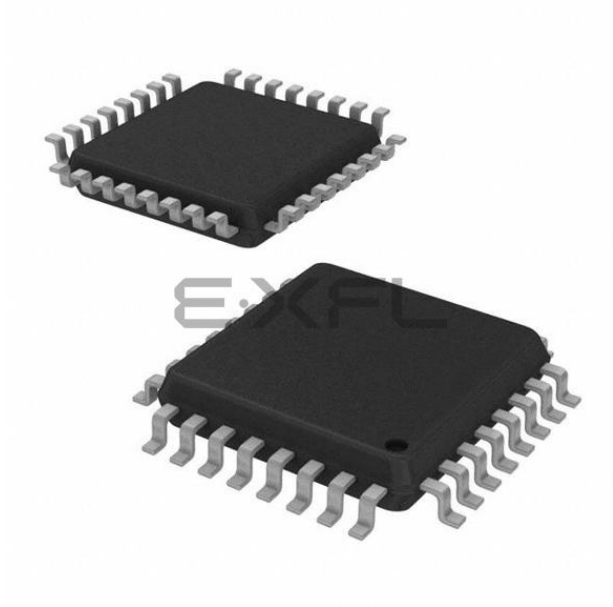

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	22
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 22x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f221-gqr

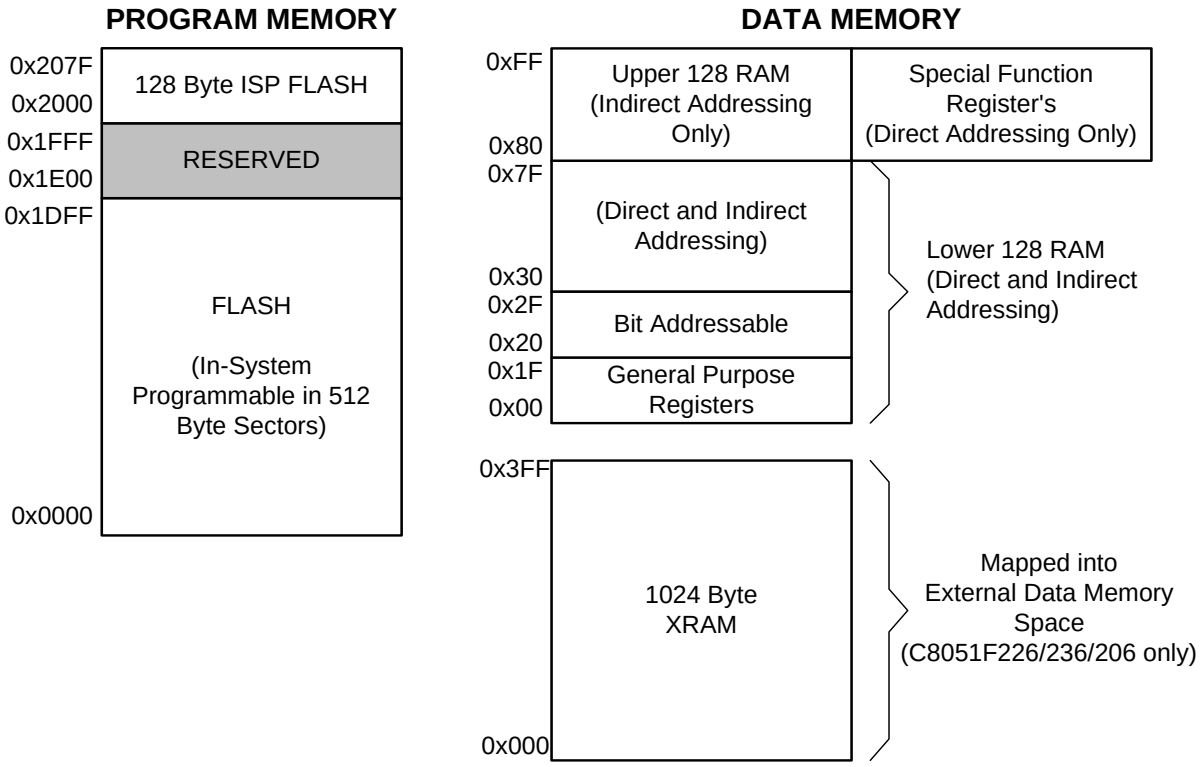


Figure 1.7. On-Board Memory Map

1.3. JTAG

The C8051F2xx have on-chip JTAG and debug logic that provide non-intrusive, full speed, in-circuit debug using the production part installed in the end application using the four-pin JTAG I/F. The C8051F2xxDK is a development kit with all the hardware and software necessary to develop application code and perform in-circuit debug with the C8051F2xx. The kit includes software with a developer's studio and debugger, an integrated 8051 assembler, and an RS-232 to JTAG interface module referred to as the EC. It also has a target application board with a C8051F2xx installed and large prototyping area, plus the RS-232 and JTAG cables, and wall-mount power supply. The Development Kit requires a Windows OS (Windows 95 or later) computer with one available RS-232 serial port. As shown in Figure 1.8, the PC is connected via RS-232 to the EC. A six-inch ribbon cable connects the EC to the user's application board, picking up the four JTAG pins and V_{DD} and GND. The EC takes its power from the application board. It requires roughly 20 mA at 2.7–3.6 V. For applications where there is not sufficient power available from the target board, the provided power supply can be connected directly to the EC.

This is a vastly superior configuration for developing and debugging embedded applications compared to standard MCU Emulators, which use on-board "ICE Chips" and target cables and require the MCU in the application board to be socketed. Silicon Labs' debug environment both increases ease of use, and preserves the performance of the precision analog peripherals.

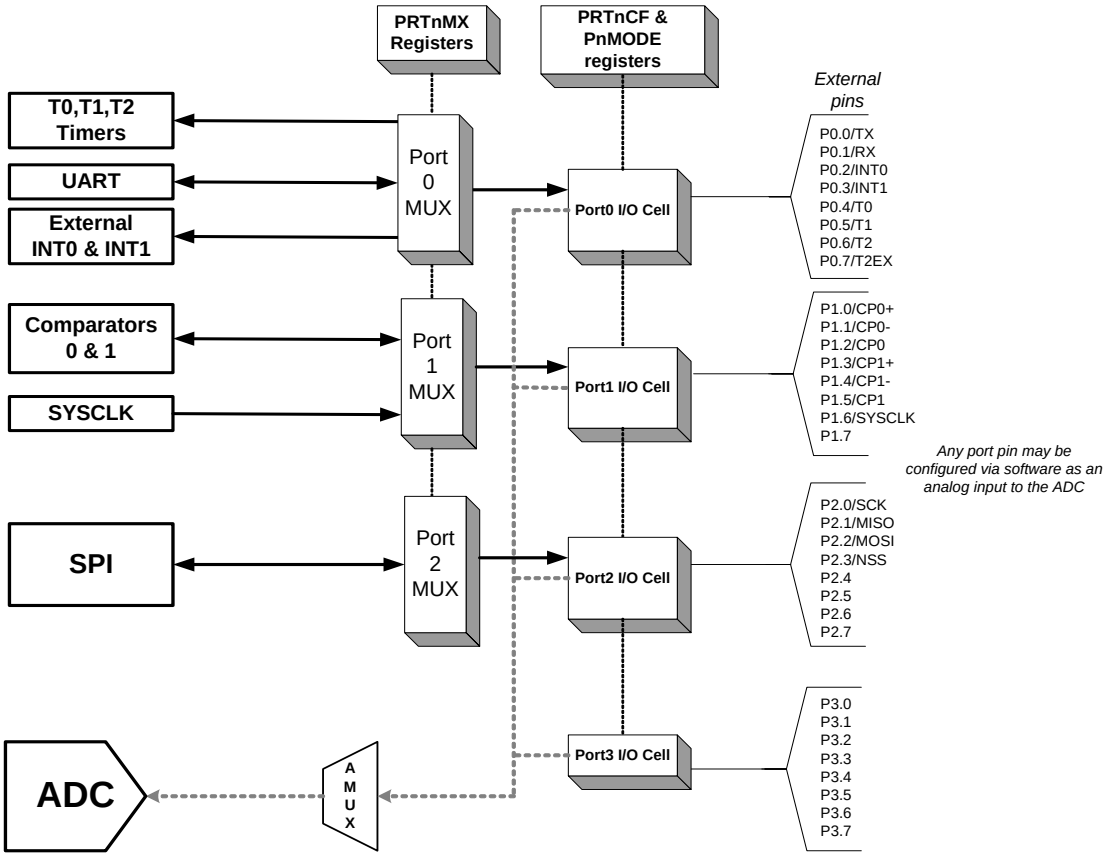


Figure 1.9. Port I/O Functional Block Diagram

1.5. Serial Ports

The C8051F206, C8051F220/1/6 and C8051F230/1/6 include a Full-Duplex UART and SPI Bus. Each of the serial buses is fully implemented in hardware and makes extensive use of the CIP-51's interrupts, thus requiring very little intervention by the CPU. The serial buses do not have to "share" resources such as timers, interrupts, or Port I/O, so both of the serial buses may be used simultaneously. (You may use Timer1, Timer 2, or SYSCLK to generate baud rates for UART).

1.6. Analog to Digital Converter

The C8051F220/1/6 has an on-chip 8-bit SAR ADC and the C8051F206 has a 12-bit SAR ADC with a programmable gain amplifier. With a maximum throughput of 100ksps, the ADC offers true 8-bit with an INL of ±1/4 LSB, and or 12-bit accuracy with ±2 LSB. The voltage reference can be the power supply (V_{DD}), or an external reference voltage (VREF). Also, the system controller can place the ADC into a power-saving shutdown mode when not in use. A programmable gain amplifier follows the analog multiplexer. The gain can be set in software from 0.5 to 16 in powers of 2.

Conversions can be initiated in two ways; a software command or an overflow on Timer 2. This flexibility allows the start of conversion to be triggered by software events, or convert continuously. A completed conversion causes an interrupt, or a status bit can be polled in software to determine the end of conversion. The resulting 8-bit data word is latched into an SFR upon completion of a conversion.

Table 5.1. 8-Bit ADC Electrical Characteristics

VDD = 3.0 V, VREF = 2.40 V, PGA Gain = 1, –40 to +85 ×C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution		—	8	—	bits
Integral Nonlinearity		—	—	±1/2	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1/2	LSB
Offset Error		±2	—	±1/2	LSB
Gain Error		±2	—	±1/2	LSB
Offset Temperature Coefficient			±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to –1 dB of full scale, 100 ksps)					
Signal-to-Noise Plus Distortion		49.5	—	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	–60	–65	—	dB
Spurious-Free Dynamic Range		—	–65	—	dB
Conversion Rate					
Conversion Time in SAR Clocks		16	—	—	clocks
SAR Clock Frequency			—	2.5	MHz
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Input Voltage Range		0	—	V_{DD}	V
Input Capacitance		—	10	—	pF
Power Specifications					
Power Supply Current	Operating Mode, 100 ksps	—	0.45	1.0	mA
Power Supply Current in Shutdown		—	0.1	1	µA
Power Supply Rejection		—	±0.3	—	mV/V

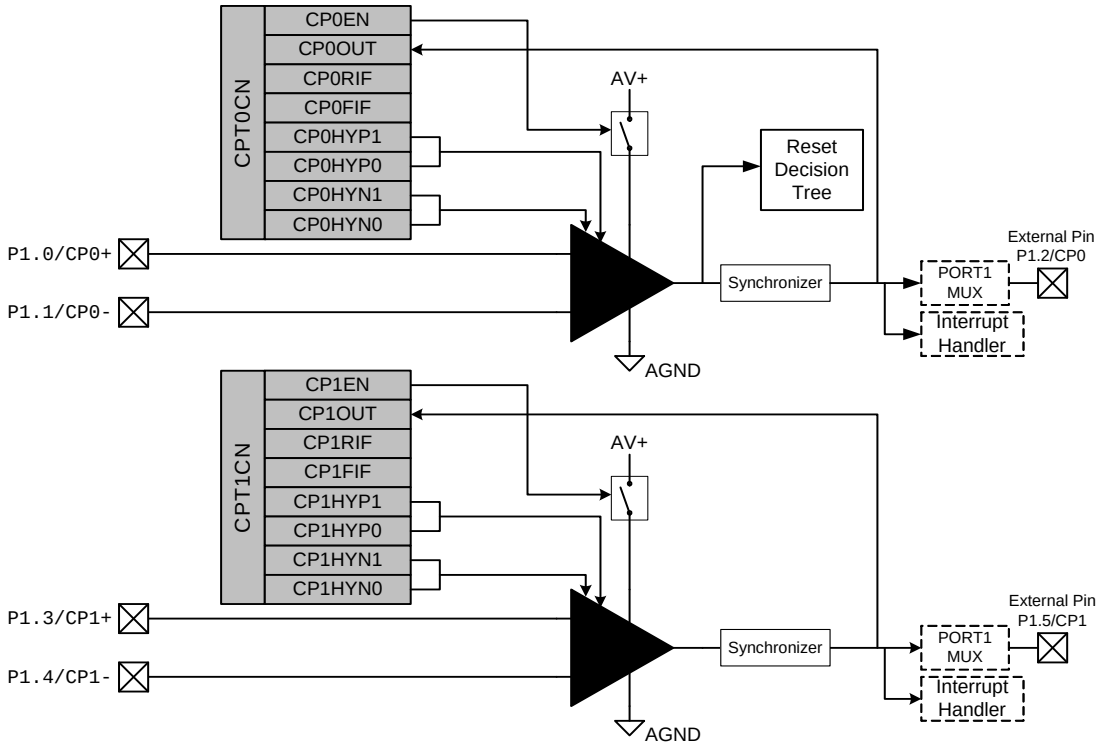


Figure 8.1. Comparator Functional Block Diagram

Table 9.3. Special Function Registers

SFR's are listed in alphabetical order.

Address	Register	Description	Page No.
0xE0	ACC	Accumulator	73
0xBC	ADC0CF	ADC Configuration	35
0xE8	ADC0CN	ADC Control	36
0xC5	ADC0GTH[1]	ADC Greater-Than Data Word (High Byte)	37
0xC4	ADC0GTL[4]	ADC Greater-Than Data Word (Low Byte)	46
0xBF	ADC0H[1]	ADC Data Word (High Byte)	37
0xBE	ADC0L[4]	ADC Data Word (Low Byte)	45
0xC7	ADC0LTH[1]	ADC Less-Than Data Word (High Byte)	46
0xCE	ADC0LTL[4]	ADC Less-Than Data Word (Low Byte)	47
0xBB	AMX0SL	ADC MUX Channel Selection	34
0xF0	B	B Register	73
0x8E	CKCON	Clock Control	131
0x9E	CPT0CN	Comparator 0 Control	55
0x9F	CPT1CN	Comparator 1 Control	56
0x83	DPH	Data Pointer (High Byte)	71
0x82	DPL	Data Pointer (Low Byte)	71
0xE6	EIE1	Extended Interrupt Enable 1	79
0xE7	EIE2	Extended Interrupt Enable 2	80
0xF6	EIP1	External Interrupt Priority 1	81
0xF7	EIP2	External Interrupt Priority 2	82
0xAF	EMI0CN[3]	External Memory Interface Control	90
0xB7	FLACL	Flash Memory Read Limit	89
0xB6	FLSCL	Flash Memory Timing Prescaler	89
0xA8	IE	Interrupt Enable	77
0xB8	IP	Interrupt Priority Control	78
0xB2	OSCICN	Internal Oscillator Control	98
0xB1	OSCXCN	External Oscillator Control	99
0x80	P0	Port 0 Latch	105
0x90	P1	Port 1 Latch	106
0xA0	P2	Port 2 Latch	107
0xB0	P3	Port 3 Latch	108
0xF1	P0MODE	Port0 Digital/Analog Output Mode	106
0xF2	P1MODE	Port1 Digital/Analog Output Mode	107
0xF3	P2MODE	Port2 Digital/Analog Output Mode	108
0xF4	P3MODE[2]	Port3 Digital/Analog Output Mode	109
0x87	PCON	Power Control	84

9.4.6. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described below. Refer to the datasheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

SFR Definition 9.8. IE: Interrupt Enable

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EA	-	ET2	ES	ET1	EX1	ET0	EX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xA8

Bit7: EA: Enable All Interrupts.
This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings.
0: Disable all interrupt sources.
1: Enable each interrupt according to its individual mask setting.

Bit6: UNUSED. Read = 0, Write = don't care.

Bit5: ET2: Enable Timer 2 Interrupt.
This bit sets the masking of the Timer 2 interrupt.
0: Disable all Timer 2 interrupts.
1: Enable interrupt requests generated by the TF2 flag (T2CON.7)

Bit4: ES: Enable Serial Port (UART) Interrupt.
This bit sets the masking of the Serial Port (UART) interrupt.
0: Disable all UART interrupts.
1: Enable interrupt requests generated by the R1 flag (SCON.0) or T1 flag (SCON.1).

Bit3: ET1: Enable Timer 1 Interrupt.
This bit sets the masking of the Timer 1 interrupt.
0: Disable all Timer 1 interrupts.
1: Enable interrupt requests generated by the TF1 flag (TCON.7).

Bit2: EX1: Enable External Interrupt 1.
This bit sets the masking of external interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the /INT1 pin.

Bit1: ET0: Enable Timer 0 Interrupt.
This bit sets the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupts.
1: Enable interrupt requests generated by the TF0 flag (TCON.5).

Bit0: EX0: Enable External Interrupt 0.
This bit sets the masking of external interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the /INT0 pin.

9.5. Power Management Modes

The CIP-51 core has two software programmable power management modes: Idle and Stop. Idle mode halts the CPU while leaving the external peripherals and internal clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the system clock is stopped. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power. SFR Definition 9.14 describes the Power Control Register (PCON) used to control the CIP-51's power management modes.

Although the CIP-51 has Idle and Stop modes built in (as with any standard 8051 architecture), power management of the entire MCU is better accomplished by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and put into low power mode. Turning off the active oscillator saves even more power, but requires a reset to restart the MCU.

9.5.1. Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt or $\overline{\text{RST}}$ is asserted. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU will resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

Note: If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from Idle mode when a future interrupt occurs. Any instructions that set the IDLE bit should be followed by an instruction that has 2 or more op-code bytes, for example:

```
// in 'C':
PCON |= 0x01;          // set IDLE bit
PCON  = PCON;          // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL   PCON,  #01h      ; set IDLE bit
MOV  PCON,  PCON       ; ... followed by a 3-cycle dummy instruction
```

If enabled, the WDT will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section 12.7 Watchdog Timer for more information on the use and configuration of the WDT.

9.5.2. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes. In Stop mode, the CPU and oscillators are stopped, effectively shutting

down all digital peripherals. Each analog peripheral must be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to sleep for longer than the MCD timeout of 100µsec.

SFR Definition 9.14. PCON: Power Control Register

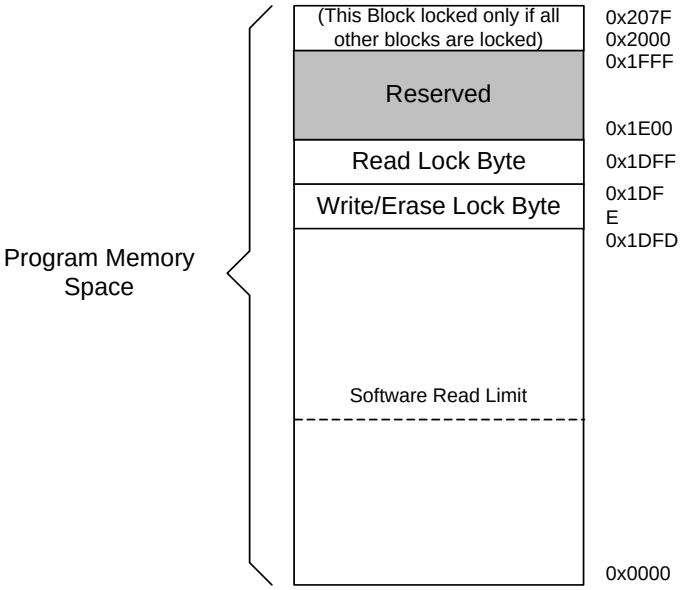
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x87

Bit7: SMOD: Serial Port Baud Rate Doubler Enable.
0: Serial Port baud rate is that defined by Serial Port Mode in SCON.
1: Serial Port baud rate is double that defined by Serial Port Mode in SCON.

Bits6–2: GF4–GF0: General Purpose Flags 4–0.
These are general purpose flags for use under software control.

Bit1: STOP: Stop Mode Select.
Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
1: Goes into power down mode. (Turns off internal oscillator).

Bit0: IDLE: Idle Mode Select.
Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.
1: Goes into idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)



Read and Write/Erase Security Bits. (Bit 7 is MSB.)

Bit	Memory Block
7	0x1C00 - 0x1DFD
6	0x1800 - 0x1BFF
5	0x1400 - 0x17FF
4	0x1000 - 0x13FF
3	0x0C00 - 0x0FFF
2	0x0800 - 0x0BFF
1	0x0400 - 0x07FF
0	0x0000 - 0x03FF

Flash Read Lock Byte

Bits7–0: Each bit locks a corresponding block of memory. (Bit 7 is MSB.)

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Write/Erase Lock Byte

Bits7–0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Access Limit Register (FLACL)

The content of this register is used as the high byte of the 16-bit software read limit address. The 16-bit read limit address value is calculated as 0xNN00 where NN is replaced by content of this register on reset. Software running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase, locations below this address. Any attempts to read locations below this limit will return the value 0x00.

Figure 10.1. Flash Program Memory Security Bytes

The lock bits can always be read and cleared to logic 0 regardless of the security setting applied to the block containing the security bytes. This allows additional blocks to be protected after the block containing the security bytes has been locked. However, the only means of removing a lock once set is to erase the entire program memory space by performing a JTAG erase operation. NOTE: Erasing the Flash memory block containing the security bytes will automatically initiate erasure of the entire program memory space (except for the reserved area). This erasure can only be performed via the JTAG. If a non-security byte in the 0x1C00–0x1DFF page is written to in order to perform an erasure of that page, then that page including the security bytes will be erased.

12.1. Power-on Reset

The CIP-51 incorporates a power supply monitor that holds the MCU in the reset state until V_{DD} rises above the VRST level during power-up. (See Figure 12.2 for timing diagram, and refer to Table 12.1 for the Electrical Characteristics of the power supply monitor circuit.) The $\overline{RST}$ pin is asserted (low) until the end of the 100msec V_{DD} Monitor timeout in order to allow the V_{DD} supply to become stable. On 48-pin packages, the V_{DD} monitor is enabled by pulling the MONEN pin high and is disabled by pulling the MONEN pin low. The MONEN pin should never be left floating. On 32-pin packages, the V_{DD} monitor is always enabled and cannot be disabled.

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC Register are indeterminate. PORSF is cleared by all other resets. Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The content of internal data memory should be assumed to be undefined after a power-on reset.

12.2. Software Forced Reset

Writing a 1 to the PORSF bit forces a Power-On Reset as described in Section 12.1.

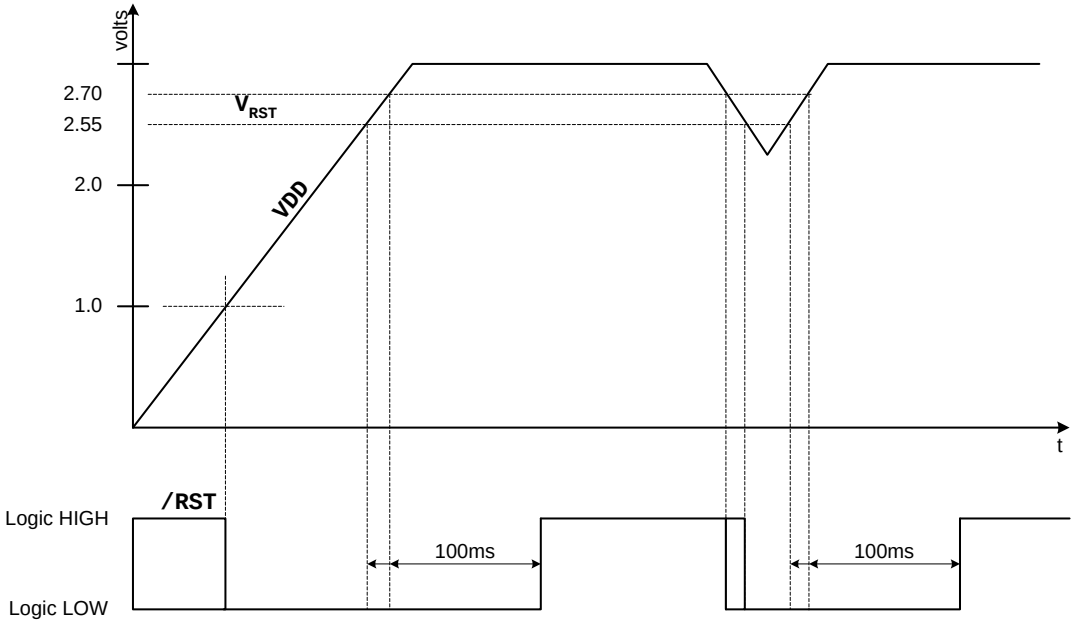


Figure 12.2. V_{DD} Monitor Timing Diagram

12.3. Power-fail Reset

When the V_{DD} monitor is enabled, the MONEN pin (not on C8051F221/F231 32 pin parts) is "pulled high", and power-down transition or power irregularity causes V_{DD} to drop below VRST, the power supply monitor will drive the $\overline{RST}$ pin low and return the CIP-51 to the reset state (see Figure 12.2). When V_{DD} returns to a level above VRST, the CIP-51 will leave the reset state in the same manner as that for the power-on reset. Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag is set, the data may no longer be valid.

SFR Definition 14.2. PRT1MX: Port I/O MUX Register 1

R	R/W	R	R	R	R	R/W	R/W	Reset Value
-	SYSCKE	-	-	-	-	CP1OEN	CP0OEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE2

Bit7: UNUSED. Read = 0.
Bit6: SYSCKE: SYSCLK Output Enable Bit
0: SYSCLK unavailable at the port pin.
1: SYSCLK output routed to pin P1.6
Bits 5–2: UNUSED. Read = 0000b, Write = don't care.
Bit1: CP1OEN: Comparator 1 Output Enable bit.
0: CP1 unavailable at Port pin.
1: CP1 routed to Port Pin P1.5.
Bit0: CP0OEN: Comparator 0 Output Enable Bit
0: CP0 unavailable at port pin.
1: CP0 routed to port pin P1.2.

SFR Definition 14.3. PRT2MX: Port I/O MUX Register 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GWPUD	P3WPUD	P2WPUD	P1WPUD	P0WPUD	-	-	SPI0OEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE3

Bit 7: GWPUD: Global Port I/O Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for all ports.
1: Weak Pull-ups Disabled (Bits 6–3 Don't cares)
Bit 6: P3WPUD: Port 3 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 3
1: Weak Pull-ups Disabled for port 3
Bit 5: P2WPUD: Port 2 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 2.
1: Weak Pull-ups Disabled for port 2
Bit 4: P1WPUD: Port 1 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 1
1: Weak Pull-ups Disabled for port 1
Bit 3: P0WPUD: Port 0 Weak Pull-up Disable Bit
0: Weak Pull-ups Enabled for port 0
1: Weak Pull-ups Disabled for port 0
Bits 2–1: UNUSED. Read = 00b, Write = don't care.
Bit 0: SPI0OEN: SPI Bus I/O Enable Bit.
0: SPI I/O unavailable at port pins.
1: SCK, MISO, MOSI, NSS routed to pins P2.0, P2.1, P2.2, and P2.3 respectively.

SFR Definition 14.12. P2MODE: Port2 Digital/Analog Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF3

Bits7–0: Port2 Digital/Analog Output Mode
0: Corresponding Port2 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port2 pin Digital Input is enabled.

SFR Definition 14.13. P3: Port3 Register*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xB0

Bits7–0: P3.[7:0]
(Write)
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding PRT3CF.n bit = 0)
(Read)
0: P3.n is logic low.
1: P3.n is logic high.

SFR Definition 14.14. PRT3CF: Port3 Configuration Register*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA7

Bits7–0: PRT3CF.[7:0]: Output Configuration Bits for P3.7–P3.0 (respectively)
0: Corresponding P3.n Output Mode is Open-Drain.
1: Corresponding P3.n Output Mode is Push-Pull.

15. Serial Peripheral Interface Bus

The Serial Peripheral Interface (SPI) provides access to a four-wire, full-duplex, serial bus. SPI supports the connection of multiple slave devices to a master device on the same bus. A separate slave-select signal (NSS) is used to select a slave device and enable a data transfer between the master and the selected slave. Multiple masters on the same bus are also supported. Collision detection is provided when two or more masters attempt a data transfer at the same time. The SPI can operate as either a master or a slave. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency.

When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less that 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of ¼ the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

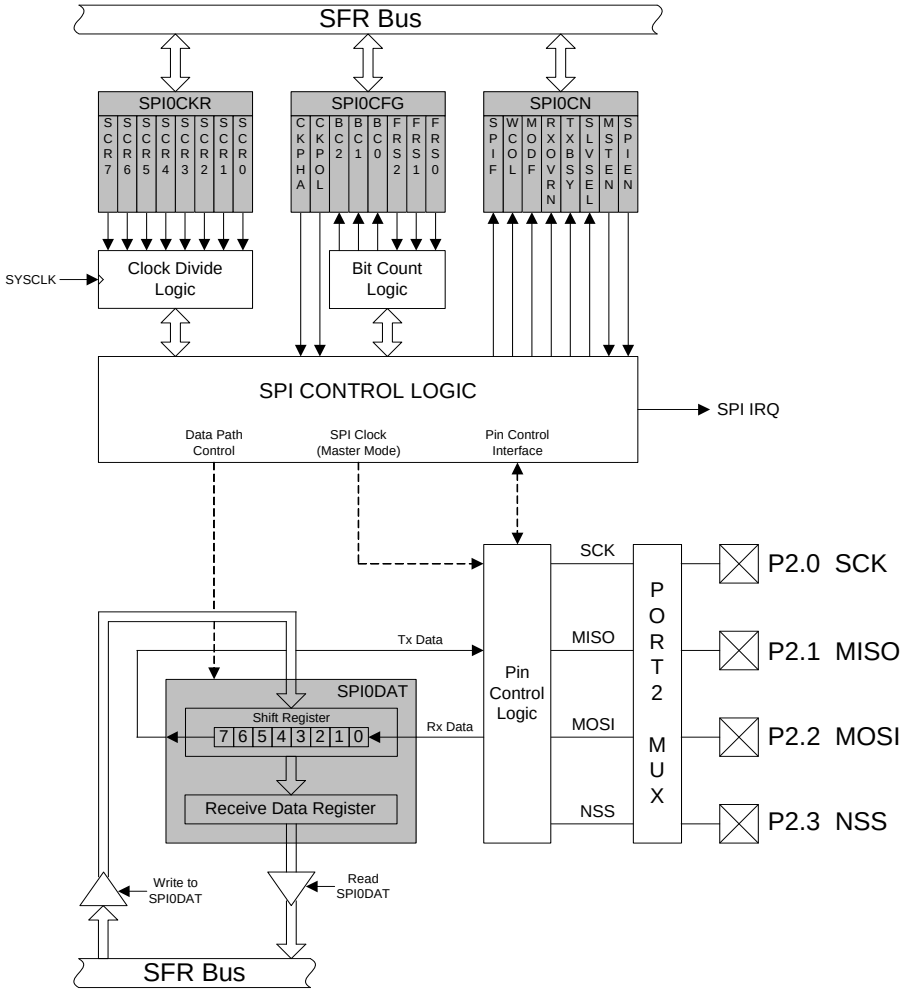


Figure 15.1. SPI Block Diagram

SFR Definition 15.1. SPI0CFG: SPI Configuration

R/W	R/W	R	R	R	R/W	R/W	R/W	Reset Value
CKPHA	CKPOL	BC2	BC1	BC0	SPIFRS2	SPIFRS1	SPIFRS0	00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9A

Bit7: CKPHA: SPI Clock Phase.
This bit controls the SPI clock phase.
0: Data sampled on first edge of SCK period.
1: Data sampled on second edge of SCK period.

Bit6: CKPOL: SPI Clock Polarity.
This bit controls the SPI clock polarity.
0: SCK line low in idle state.
1: SCK line high in idle state.

Bits5–3: BC2–BC0: SPI Bit Count.
Indicates which of the up to 8 bits of the SPI word have been transmitted.

BC2–BC0			Bit Transmitted
0	0	0	Bit 0 (LSB)
0	0	1	Bit 1
0	1	0	Bit 2
0	1	1	Bit 3
1	0	0	Bit 4
1	0	1	Bit 5
1	1	0	Bit 6
1	1	1	Bit 7 (MSB)

Bits2–0: SPIFRS2–SPIFRS0: SPI Frame Size.
These three bits determine the number of bits to shift in/out of the SPI shift register during a data transfer in master mode. They are ignored in slave mode.

SPIFRS			Bits Shifted
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

SFR Definition 15.2. SPI0CN: SPI Control

R/W	R/W	R/W	R/W	R	R	R/W	R/W	Reset Value
SPIF	WCOL	MODF	RXOVRN	TXBSY	SLVSEL	MSTEN	SPIEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF8

Bit7: SPIF: SPI Interrupt Flag.
This bit is set to logic 1 by hardware at the end of a data transfer. If interrupts are enabled, setting this bit causes the CPU to vector to the SPI0 interrupt service routine. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit6: WCOL: Write Collision Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) to indicate a write to the SPI data register was attempted while a data transfer was in progress. It is cleared by software.

Bit5: MODF: Mode Fault Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when a master mode collision is detected (NSS is low and MSTEN = 1). This bit is not automatically cleared by hardware. It must be cleared by software.

Bit4: RXOVRN: Receive Overrun Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when the receive buffer still holds unread data from a previous transfer and the last bit of the current transfer is shifted into the SPI shift register. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit3: TXBSY: Transmit Busy Flag.
This bit is set to logic 1 by hardware while a master mode transfer is in progress. It is cleared by hardware at the end of the transfer.

Bit2: SLVSEL: Slave Selected Flag.
This bit is set to logic 1 whenever the NSS pin is low indicating it is enabled as a slave. It is cleared to logic 0 when NSS is high (slave disabled).

Bit1: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit0: SPIEN: SPI Enable.
This bit enables/disables the SPI.
0: SPI disabled.
1: SPI enabled.

SFR Definition 15.3. SPI0CKR: SPI Clock Rate Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9D

Bits7–0: SCR7–SCR0: SPI Clock Rate
These bits determine the frequency of the SCK output when the SPI module is configured for master mode operation. The SCK clock frequency is a divided down version of the system clock, and is given in the following equations:

fSCK = 0.5 x fSYSCLK / (SPI0CKR + 1), for 0 ≤ SPI0CKR ≤ 255,

SFR Definition 15.4. SPI0DAT: SPI Data Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x9B

Bits7–0: SPI0DAT: SPI0 Transmit and Receive Data.
The SPI0DAT register is used to transmit and receive SPI data. Writing data to SPI0DAT places the data immediately into the shift register and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

16. UART

Description

The CIP-51 includes a serial port (UART) capable of asynchronous transmission. The UART can function in full duplex mode. In all modes, receive data is buffered in a holding register. This allows the UART to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART has an associated Serial Control Register (SCON) and a Serial Data Buffer (SBUF) in the SFRs. The single SBUF location provides access to both transmit and receive registers. Reads access the Receive register and writes access the Transmit register automatically.

The UART is capable of generating interrupts if enabled. The UART has two sources of interrupts: a Transmit Interrupt flag, TI (SCON.1) set when transmission of a data byte is complete, and a Receive Interrupt flag, RI (SCON.0) set when reception of a data byte is complete. The UART interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software. This allows software to determine the cause of the UART interrupt (transmit complete or receive complete).

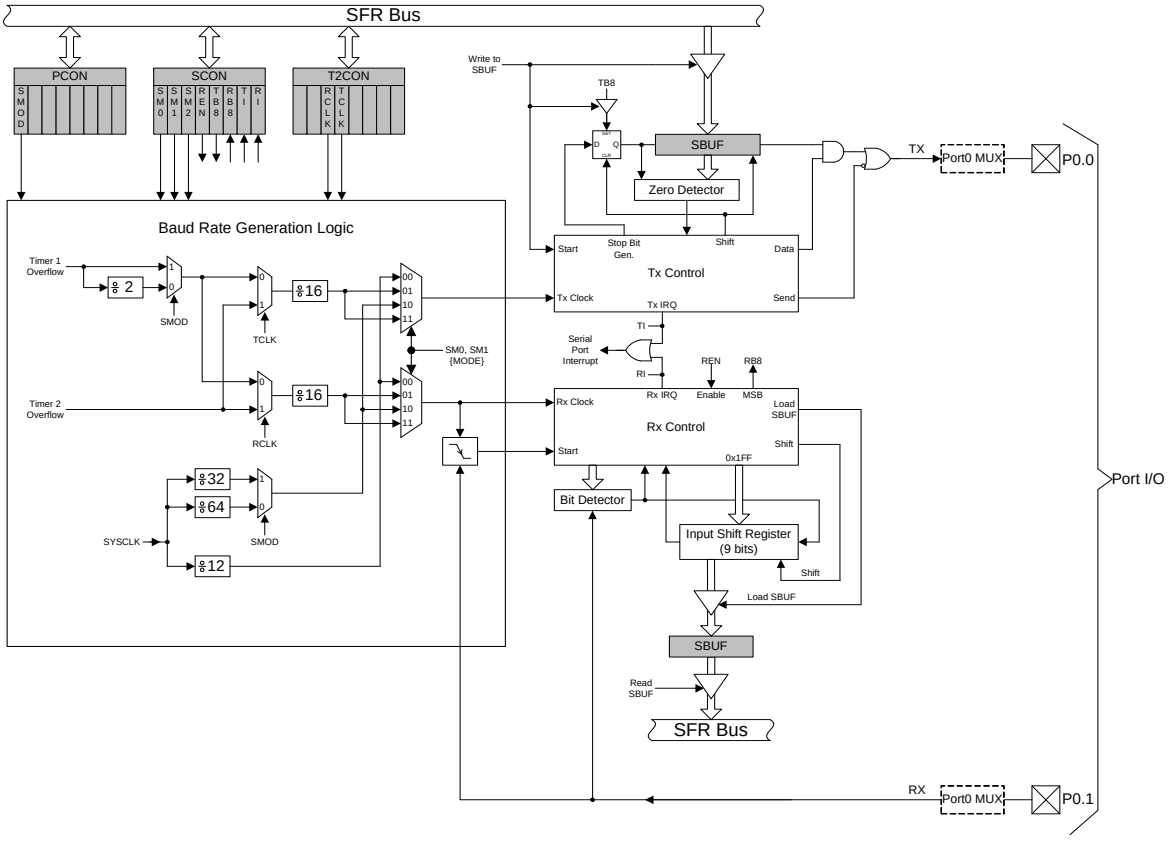


Figure 16.1. UART Block Diagram

SFR Definition 17.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x88

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 input signal's logic level when IT1 = 0.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT1 is level triggered.
1: /INT1 is edge triggered.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 input signal's logic level when IT0 = 0.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT0 is level triggered.
1: /INT0 is edge triggered.

SFR Definition 17.3. CKCON: Clock Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	T2M	T1M	T0M	-	-	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8E

Bits7–6: UNUSED. Read = 00b, Write = don't care.

Bit5: T2M: Timer 2 Clock Select.
This bit controls the division of the system clock supplied to Timer 2. This bit is ignored when the timer is in baud rate generator mode or counter mode (i.e. C/T2 = 1).
0: Timer 2 uses the system clock divided by 12.
1: Timer 2 uses the system clock.

Bit4: T1M: Timer 1 Clock Select.
This bit controls the division of the system clock supplied to Timer 1.
0: Timer 1 uses the system clock divided by 12.
1: Timer 1 uses the system clock.

Bit3: T0M: Timer 0 Clock Select.
This bit controls the division of the system clock supplied to Counter/Timer 0.
0: Counter/Timer uses the system clock divided by 12.
1: Counter/Timer uses the system clock.

Bits2–0: UNUSED. Read = 000b, Write = don't care.

SFR Definition 17.4. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8A

Bits 7–0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 17.5. TL1: Timer 1 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8B

Bits 7–0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 17.6. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8C

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 17.7. TH1: Timer 1 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8D

Bits 7–0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.