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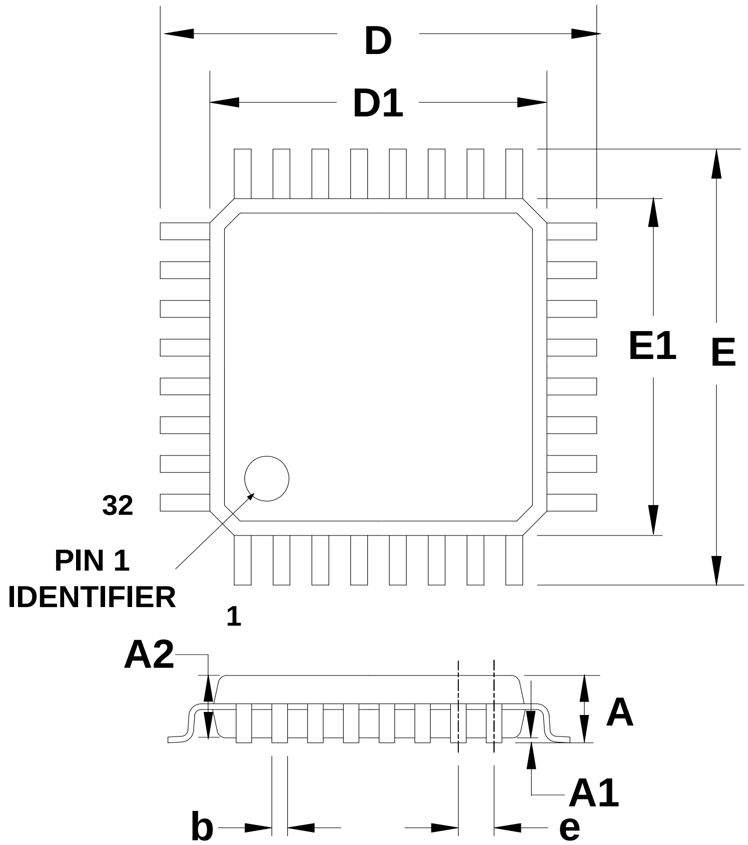
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 32x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f226-gqr

List of Figures and Tables



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
D	-	9.00	-
D1	-	7.00	-
e	-	0.80	-
E	-	9.00	-
E1	-	7.00	-

Figure 4.4. LQFP-32 Package Drawing

SFR Definition 5.4. ADC0H: ADC Data Word (‘F220/1/6 and ‘F206)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
MSB							LSB	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBF

Bits7–0: ADC Data Word Bits

EXAMPLE: ADC Data Word Conversion Map

AIN – GND(Volts)	ADC0H
REF x (255/256)	0xFF
REF x ½	0x80
REF x (127/256)	0x7F
0	0x00

5.3. ADC Programmable Window Detector

The ADC programmable window detector is very useful in many applications. It continuously compares the ADC output to user-programmed limits and notifies the system when an out-of-band condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (ADWINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC Greater-Than and ADC Less-Than registers (ADC0GTH and ADC0LTH).

SFR Definition 5.5. ADC0GTH: ADC Greater-Than Data (‘F220/1/6 and ‘F206)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC5

Bits7–0:
The high byte of the ADC Greater-Than Data Word.

SFR Definition 5.6. ADC0LTH: ADC Less-Than Data Byte (‘F220/1/6 and ‘F206)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC7

Bits7–0:
The high byte of the ADC Less-Than Data Word.

6.2. ADC Modes of Operation

The ADC has a maximum conversion speed of 100 ksps. The ADC conversion clock is derived from the system clock. The ADC conversion clock is derived from a divided version of SYSCLK. Divide ratios of 1, 2, 4, 8, or 16 are supported by setting the ADCSC bits in the ADC0CF Register. This is useful to adjust conversion speed to accommodate different system clock speeds.

A conversion can be initiated in one of two ways, depending on the programmed states of the ADC Start of Conversion Mode bits (ADSTM1, ADSTM0) in ADC0CN. Conversions may be initiated by:

1. Writing a 1 to the ADBUSY bit of ADC0CN;
2. A Timer 2 overflow (i.e. timed continuous conversions).

Writing a 1 to ADBUSY provides software control of the ADC whereby conversions are performed "on-demand". During conversion, the ADBUSY bit is set to 1 and restored to 0 when conversion is complete. The falling edge of ADBUSY triggers an interrupt (when enabled) and sets the ADCINT interrupt flag in the ADC0CN register. Note: When conversions are performed "on-demand", the ADCINT flag, not ADBUSY, should be polled to determine when the conversion has completed. Converted data is available in the ADC data word register, ADC0H.

The ADCTM bit in register ADC0CN controls the ADC track-and-hold mode. In its default state, the ADC input is continuously tracked, except when a conversion is in progress. Setting ADCTM to 1 allows one of two different low power track-and-hold modes to be specified by states of the ADSTM1-0 bits (also in ADC0CN):

1. Tracking begins with a write of 1 to ADBUSY and lasts for 3 SAR clocks;
2. Tracking starts with an overflow of Timer 2 and lasts for 3 SAR clocks.

Tracking can be disabled (shutdown) when the entire chip is in low power standby or sleep modes.

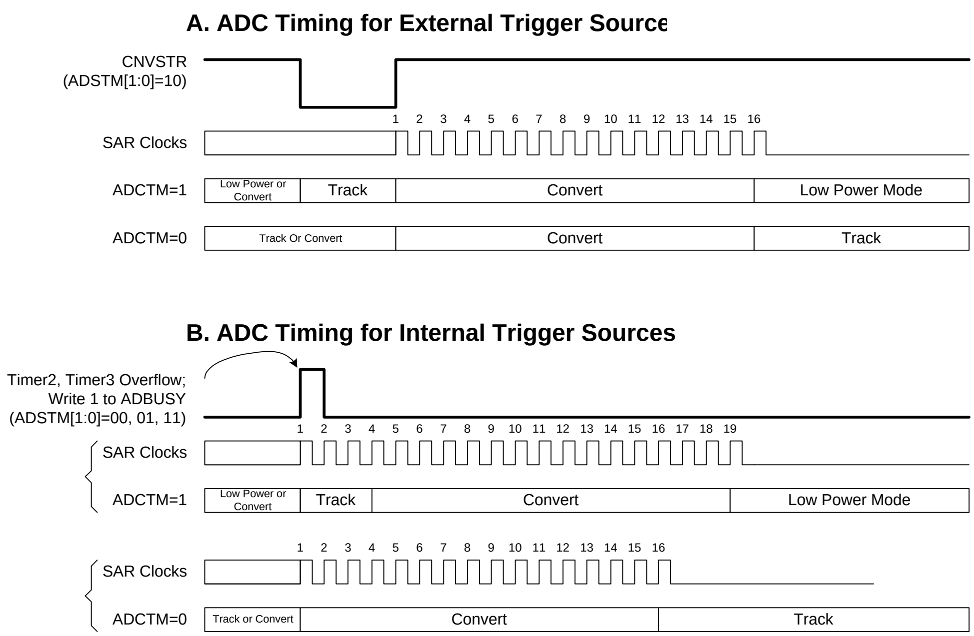


Figure 6.2. 12-Bit ADC Track and Conversion Example Timing

SFR Definition 6.1. AMX0SL: AMUX Channel Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	AMXEN	PRTSL1	PRTSL0	PINSL2	PINSL1	PINSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

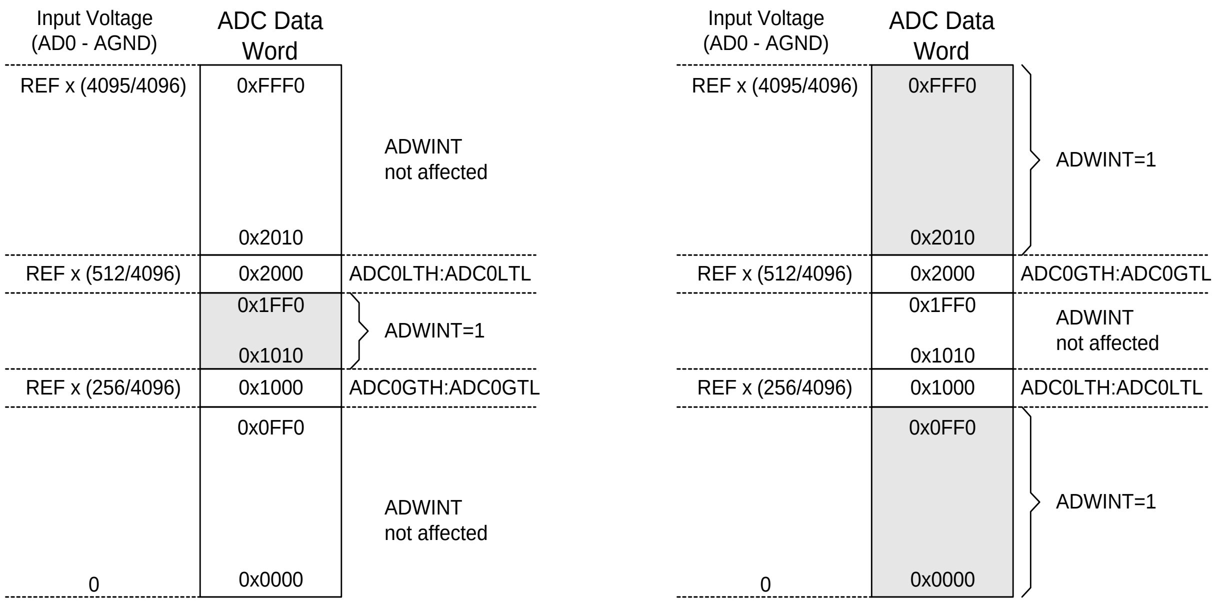
Bits 7–6: UNUSED. Read = 00b; Write = don't care
Bit 5: AMXEN enable
0: AMXEN disabled and port pins are unavailable for analog use.
1: AMXEN enabled to use/select port pins for analog use.
Bits 4–3: PRTSL1–0: Port Select Bits*.
00: Port0 select to configure pin for analog input from this port.
01: Port1 select to configure pin for analog input from this port.
10: Port2 select to configure pin for analog input from this port.
11: Port3 select to configure pin for analog input from this port.
Bits 2–0:PINSL2–0: Pin Select Bits
000: Pin 0 of selected port (above) to be used for analog input.
001: Pin 1 of selected port (above) to be used for analog input.
010: Pin 2 of selected port (above) to be used for analog input.
011: Pin 3 of selected port (above) to be used for analog input.
100: Pin 4 of selected port (above) to be used for analog input.
101: Pin 5 of selected port (above) to be used for analog input.
110: Pin 6 of selected port (above) to be used for analog input.
111: Pin 7 of selected port (above) to be used for analog input.

* Selecting a port for analog input does NOT default all pins of that port as analog input. After selecting a port for analog input, a pin must be selected using pin select bits (PINSL2–0). For example, after setting the AMXEN to '1', setting PRTSL1–0 to "11", and setting PINSL2–0 to "100" P3.4 is configured as analog input. All other Port 3 pins remain as GPIO pins. Also note that in order to use a port pin as analog input, its input mode should be set to *analog*. Please see section 14.2.

SFR Definition 6.2. ADC0CF: ADC Configuration (‘F220/1/6 and ‘F206)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ADCSC2	ADCSC1	ADCSC0	-	-	AMPGN2	AMPGN1	AMPGN0	01100000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBC

Bits7–5: ADCSC2–0: ADC SAR Conversion Clock Period Bits
000: SAR Conversion Clock = 1 System Clock
001: SAR Conversion Clock = 2 System Clocks
010: SAR Conversion Clock = 4 System Clocks
011: SAR Conversion Clock = 8 System Clocks
1xx: SAR Conversion Clock = 16 Systems Clocks
NOTE: SAR conversion clock should be less than or equal to 2MHz.
Bits4–3: UNUSED. Read = 00b; Write = don't care
Bits2–0: AMPGN2–0: ADC Internal Amplifier Gain
000: Gain = 1
001: Gain = 2
010: Gain = 4
011: Gain = 8
10x: Gain = 16
1x: Gain = 0.5



Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1, ADC0LTH:ADC0LTL = 0x2000, ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0x1000.

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1, ADC0LTH:ADC0LTL = 0x1000, ADC0GTH:ADC0GTL = 0x2000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 or > 0x2000.

Figure 6.4. 12-Bit ADC Window Interrupt Examples, Left Justified Data

7. Voltage Reference (C8051F206/220/221/226)

The voltage reference circuit selects between an externally connected reference and the power supply voltage (V_{DD}). (See Figure 7.1).

An external reference can be connected to the VREF pin and selected by setting the REF0CN special function register per Figure 7.1. The external reference supply must be between V_{DD} – 0.3 V and 1 V. V_{DD} may also be selected using REF0CN per SFR Definition 7.1. The electrical specifications for the Voltage Reference are given in Table 7.1.

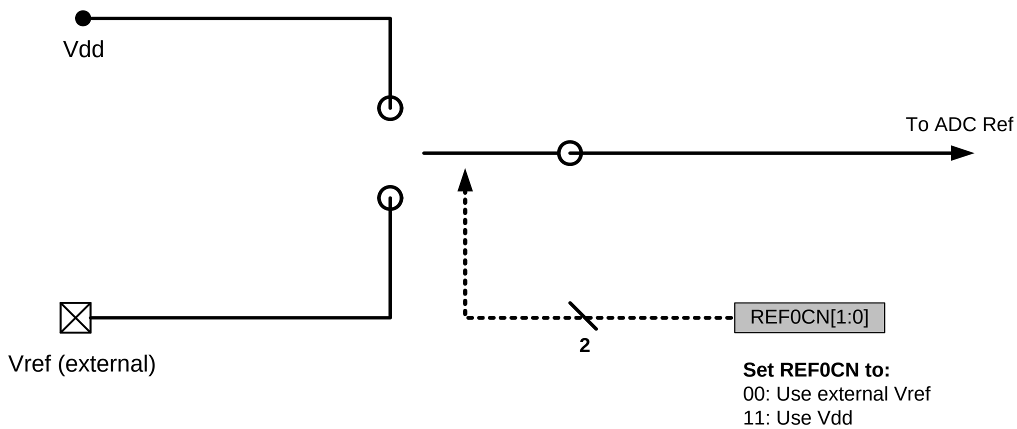


Figure 7.1. Voltage Reference Functional Block Diagram

SFR Definition 7.1. REF0CN: Reference Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	REFSL1	REFSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xD1

Bits7–2: UNUSED. Read = 00000b; Write = don't care

Bit1–0: REFSL1– REFSL0: Voltage reference selection.
Bits control which reference is selected.
00: External VREF source is selected.
01: Reserved.
10: Reserved.
11: V_{DD} selected as VREF source.

Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
MOV A,#data	Move immediate to A	2	2
MOV Rn,A	Move A to register	1	1
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate to register	2	2
MOV direct,A	Move A to direct byte	2	2
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate to direct byte	3	3
MOV @Ri,A	Move A to indirect RAM	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	2	2
MOV @Ri,#data	Move immediate to indirect RAM	2	2
MOV DPTR,#data16	Load data pointer with 16-bit constant	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A,@A+PC	Move code byte relative PC to A	1	3
MOVX A,@Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri,A	Move A to external data (8-bit address)	1	3
MOVX A,@DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR,A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with A	1	1
XCH A,direct	Exchange direct byte with A	2	2
XCH A,@Ri	Exchange indirect RAM with A	1	2
XCHD A,@Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit to carry	2	2
ANL C,/bit	AND complement of direct bit to carry	2	2
ORL C,bit	OR direct bit to carry	2	2
ORL C,/bit	OR complement of direct bit to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
JC rel	Jump if carry is set	2	2/3

Table 9.4. Interrupt Summary (Continued)

Interrupt Source	Interrupt Vector	Priority Order	Interrupt-Pending Flag	Enable
ADC0 End of Conversion	0x007B	15	ADCINT (ADC0CN.5)	EADC0 (EIE2.1)
Software Controlled Interrupt 0	0x0083	16	SCI0 (SWCINT.4)	ESCI0 (EIE2.2)
Software Controlled Interrupt 1	0x008B	17	SCI1 (SWCINT.5)	ESCI1 (EIE2.3)
Software Controlled Interrupt 2	0x0093	18	SCI2 (SWCINT.6)	ESCI2 (EIE2.4)
Software Controlled Interrupt 3	0x009B	19	SCI3 (SWCINT.7)	ESCI3 (EIE2.5)
Unused Interrupt Location	0x00A3	20	None	Reserved (EIE2.6)
External Crystal OSC Ready	0x00AB	21	XTLVLD (OSCXCN.7)	EXVLD (EIE2.7)

9.4.4. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP–EIP2) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate.

9.4.5. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. NOTE: If a Flash write or erase is performed, the MCU is stalled during the operation and interrupts will not be serviced until the operation is complete. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

down all digital peripherals. Each analog peripheral must be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to sleep for longer than the MCD timeout of 100µsec.

SFR Definition 9.14. PCON: Power Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x87

Bit7: SMOD: Serial Port Baud Rate Doubler Enable.
0: Serial Port baud rate is that defined by Serial Port Mode in SCON.
1: Serial Port baud rate is double that defined by Serial Port Mode in SCON.

Bits6–2: GF4–GF0: General Purpose Flags 4–0.
These are general purpose flags for use under software control.

Bit1: STOP: Stop Mode Select.
Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
1: Goes into power down mode. (Turns off internal oscillator).

Bit0: IDLE: Idle Mode Select.
Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.
1: Goes into idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

The Flash Access Limit security feature protects proprietary program code and data from being read by software running on the CIP-51. This feature provides support for OEMs that wish to program the MCU with proprietary value-added firmware before distribution. The value-added firmware can be protected while allowing additional code to be programmed in remaining program memory space later.

The Software Read Limit (SRL) is a 16-bit address that establishes two logical partitions in the program memory space. The first is an upper partition consisting of all the program memory locations at or above the SRL address, and the second is a lower partition consisting of all the program memory locations starting at 0x0000 up to (but excluding) the SRL address. Software in the upper partition can execute code in the lower partition, but is prohibited from reading locations in the lower partition using the MOVC instruction. (Executing a MOVC instruction from the upper partition with a source address in the lower partition will always return a data value of 0x00.) Software running in the lower partition can access locations in both the upper and lower partition without restriction.

The Value-added firmware should be placed in the lower partition. On reset, control is passed to the value-added firmware via the reset vector. Once the value-added firmware completes its initial execution, it branches to a predetermined location in the upper partition. If entry points are published, software running in the upper partition may execute program code in the lower partition, but it cannot read the contents of the lower partition. Parameters may be passed to the program code running in the lower partition either through the typical method of placing them on the stack or in registers before the call or by placing them in prescribed memory locations in the upper partition.

The SRL address is specified using the contents of the Flash Access Register. The 16-bit SRL address is calculated as 0xNN00, where NN is the contents of the SRL Security Register. Thus, the SRL can be located on 256-byte boundaries anywhere in program memory space. However, the 512-byte erase sector size essentially requires that a 512 boundary be used. The contents of a non-initialized SRL security byte is 0x00, thereby setting the SRL address to 0x0000 and allowing read access to all locations in program memory space by default.

SFR Definition 10.1. PSCTL: Program Store RW Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	-	-	PSEE	PSWE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x8F

Bits7–2: UNUSED. Read = 000000b, Write = don't care.

Bit1: PSEE: Program Store Erase Enable.
Setting this bit allows an entire page of the Flash program memory to be erased (provided the PSWE bit is set to '1'). After setting this bit, a write to Flash memory using the MOVX instruction will erase the entire page that contains the location addressed by the MOVX instruction. The value of the data byte written does not matter.
0: Flash program memory erasure disabled.
1: Flash program memory erasure enabled.

Bit0: PSWE: Program Store Write Enable.
Setting this bit allows writing a byte of data to the Flash program memory using the MOVX instruction. The location must be erased before writing data.
0: Write to Flash program memory disabled.
1: Write to Flash program memory enabled.

13.1. External Crystal Example

If a crystal were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 1. For an ECS-110.5-20-4 crystal, the resonate frequency is 11.0592 MHz, the intrinsic capacitance is 7 pF, and the ESR is 60 W. The compensation capacitors should be 33 pF each, and the PWB parasitic capacitance is estimated to be 2 pF. The appropriate External Oscillator Frequency Control value (XFCN) from the Crystal column in the table in SFR Definition 13.2 (OSCXCN Register) should be 111b.

The Crystal Oscillator Valid Flag (XTLVLD in register OSCXCN) is set to logic 1 by hardware when the external oscillator is running and stable. The XTLVLD detection circuit requires a startup time of at least 1ms between enabling the oscillator and checking the XTLVLD flag. Switching to the external oscillator before 1ms can result in unpredictable behavior. The recommend procedure is:

1. Enable the external oscillator
2. Wait 1 ms
3. Poll for XTLVLD '0' ==> '1'
4. Switch to the external oscillator

Switching to the external oscillator before the crystal oscillator has stabilized could result in unpredictable behavior.

NOTE: Crystal oscillator circuits are quite sensitive to PCB layout. The crystal should be placed as close as possible to the XTAL pins on the device, keeping the traces as short as possible and shielded with ground plane from any other traces which could introduce noise or interference.

13.2. External RC Example

If an external RC network were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 2. The capacitor must be no greater than 100 pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kW and C = 50 pF:

f = 1.23(103)/RC = 1.23(103) / [246 x 50] = 0.1 MHz = 100 kHz

XFCN ^{3} log2(f/25 kHz)
XFCN ^{3} log2(100 kHz/25 kHz) = log2(4)
XFCN ^{3} 2, or code 010

13.3. External Capacitor Example

If an external capacitor were used to generate the system clock for the MCU, the circuit would be as shown in Figure 13.1, Option 3. The capacitor must be no greater than 100 pF, but using a very small capacitor will increase the frequency drift due to the PWB parasitic capacitance. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume V_{DD} = 3.0 V and C = 50 pF:

f = KF / (C x V_{DD}) = KF / (50 x 3)
f = KF / 150

If a frequency of roughly 90kHz is desired, select the K Factor from the table in SFR Definition 13.2 as KF = 13:

f = 13 /150 = 0.087 MHz, or 87 kHz

Therefore, the XFCN value to use in this example is 011.

14. Port Input/Output

Description

The C8051F221/231 have three I/O Ports: Port0, Port1, and Port2. The C8051F206, C8051F220/6 and C8051F230/6 have four I/O Ports: Port0, Port1, Port2, and Port3. A wide array of digital resources can be assigned to these ports by the simple configuration of the port's corresponding multiplexer (MUX). Please see Figure 8.1. Additionally, all external port pins are available as analog input.

14.1. Port I/O Initialization

Port I/O initialization is straightforward. Registers PRT0MX, PRT1MX and PRT2MX must be loaded with the appropriate values to select the digital I/O functions required by the design. The output driver characteristics of the I/O pins are defined using the Port Configuration Registers PRT0CF, PRT1CF, PRT2CF and PRT3CF. Each Port Output driver can be configured as either Open Drain or Push-Pull. This is required even for the digital resources selected in the PRTnMX registers, and is not automatic.

Any or all pins may be configured as digital I/O or as analog input. The default mode is digital I/O. The P0MODE, P1MODE, P2MODE, and P3MODE special function registers are used to configure the port pins as digital or analog as defined in this section.

The final step is initializing the individual resources selected using the appropriate setup registers. Initialization procedures for the various digital resources may be found in the detailed explanation of each available function. The reset state of each register is shown in the figures that describe each individual register.

NOTE: The input mode of pins configured for use with Timer 0, 1, or 2 must be manually configured.

1. The output mode of all ports pins must be configured regardless of whether the port pin is either standard general-purpose I/O or controlled by a digital peripheral.
2. For all pins used as Timer inputs (P0.4/T0, P0.5/T1, P0.6/T2, and P0.7/T2EX), the output mode must be "open-drain" (which is the reset state), and "1" must be written to the associated port pin to prevent possible contention for the port pin that could result in an overcurrent condition. For example, to configure a Timer0, set PRT0MX's T0E Timer0 enable bit to '1' to route Timer0 to Port Pin P0.4. Then place P0.4/T0 in open-drain configuration (which is set in PRT0CF by default), and write a '1' to P0.4 to set its output state to high impedance for use as a digital peripheral input (port pins also default to logic high state upon reset). Lastly, ensure P0MODE.4 is '1' for digital input mode. (All pins default to digital input mode upon reset.)

SFR Definition 14.1. PRT0MX: Port I/O MUX Register 0

R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	Reset Value
T2EXE	T2E	T1E	T0E	INT1E	INT0E	-	UARTEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE1

Bit7: T2EXE: T2EX Enable Bit
0: T2EX unavailable at Port pin.
1: T2EX routed to Port Pin.

Bit6: T2E: T2 Enable Bit
0: T2 unavailable at Port pin.
1: T2 routed to Port Pin.

Bit5: T1E: T1 Enable Bit
0: T1 unavailable at Port pin.
1: T1 routed to Port Pin.

Bit4: T0E: T0 Enable Bit
0: T0 unavailable at Port pin.
1: T0 routed to Port Pin.

Bit3: INT1E: /INT1 Enable Bit
0: /INT1 unavailable at Port pin.
1: /INT1 routed to port pin.

Bit2: INT0E: /INT0 Enable Bit
0: /INT0 unavailable at Port pin.
1: /INT0 routed to Port Pin.

Bit1: UNUSED. Read = 0, Write = don't care.

Bit0: UARTEN: UART I/O Enable
0: UART I/O unavailable at port pins.
1: TX, RX routed to pins P0.0 and P0.1, respectively.

SFR Definition 14.9. P1MODE: Port1 Digital/Analog Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF2

Bits7–0: Port1 Digital/Analog Output Mode
0: Corresponding Port1 pin Digital Input disabled. (For analog use, i.e., ADC or comparators).
1: Corresponding Port1 pin Digital Input is enabled.

SFR Definition 14.10. P2: Port2 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	11111111
Bit7	Bit6	Bit	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xA0

Bits7–0: P2.[7:0]
(Write - Output appears on I/O pins per PRT0MX, PRT1MX, and PRT2MX registers)
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding PRT2CF.n bit = 0)
(Read - Regardless of PRT0MX, PRT1MX, and PRT2MX Register settings).
0: P2.n is logic low.
1: P2.n is logic high.

SFR Definition 14.11. PRT2CF: Port2 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA6

Bits7–0: PRT2CF.[7:0]: Output Configuration Bits for P2.7–P2.0 (respectively)
0: Corresponding P2.n Output Mode is Open-Drain.
1: Corresponding P2.n Output Mode is Push-Pull.

SFR Definition 14.15. P3MODE: Port3 Digital/Analog Input Mode*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF4

Bits7–0: Port3 Digital/Analog Output Mode
0: Corresponding Port3 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port3 pin Digital Input is enabled.

* (Available on C8051F206, C8051F220/6 and C8051F230/6)

Table 14.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –10 uA, Port I/O push-pull I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{DD} – 0.1 V_{DD} – 0.7	V_{DD} – 0.8		V
Output Low Voltage	I_{OL} = 10 uA I_{OL} = 8.5 mA I_{OL} = 25 mA		1.0	0.1 0.6	V
Input High Voltage		0.7 x V_{DD}			V
Input Low Voltage				0.3 x V_{DD}	V
Input Leakage Current	DGND < Port Pin < V_{DD}, Pin Tri-state Weak Pull-up Off Weak Pull-up On		30	±1	µA
Capacitive Loading			3		pF

15. Serial Peripheral Interface Bus

The Serial Peripheral Interface (SPI) provides access to a four-wire, full-duplex, serial bus. SPI supports the connection of multiple slave devices to a master device on the same bus. A separate slave-select signal (NSS) is used to select a slave device and enable a data transfer between the master and the selected slave. Multiple masters on the same bus are also supported. Collision detection is provided when two or more masters attempt a data transfer at the same time. The SPI can operate as either a master or a slave. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency.

When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less that 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of ¼ the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the system clock.

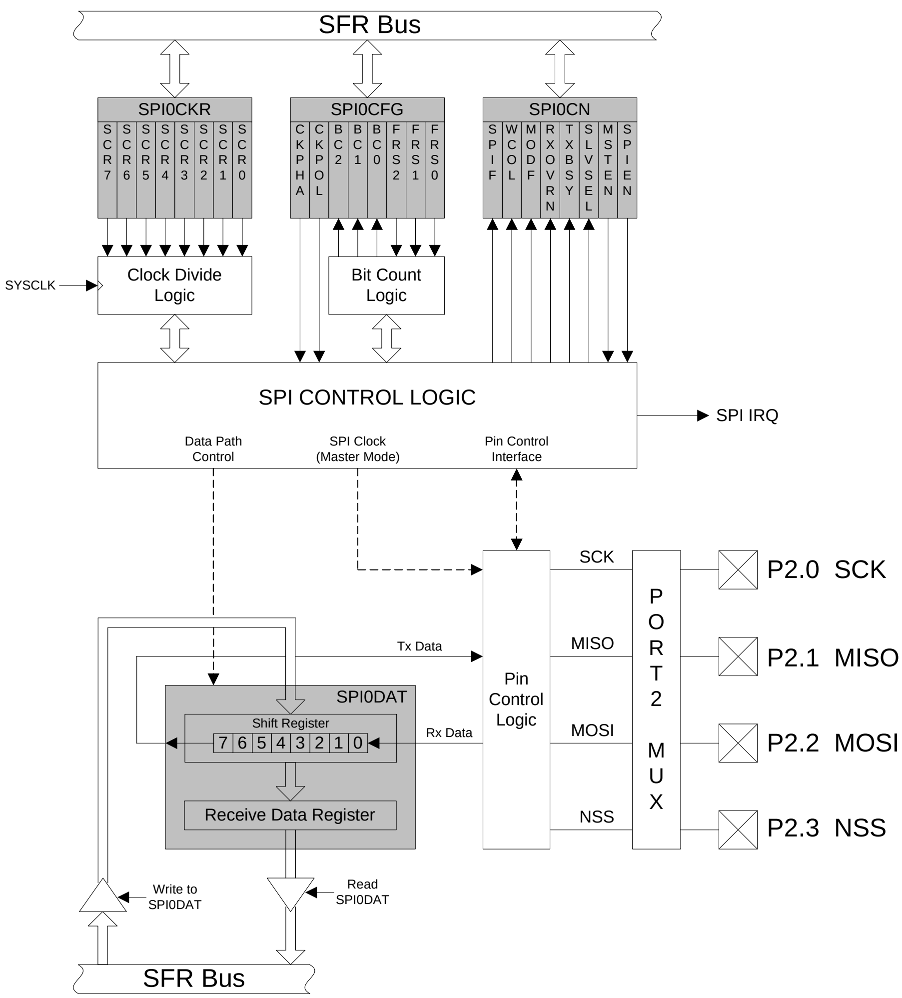


Figure 15.1. SPI Block Diagram

16.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit (see the timing diagram in Figure 16.4). Data are transmitted from the TX pin and received at the RX pin (see the interconnection diagram in Figure 16.5). On receive, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2).

Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: RI must be logic 0, and if SM2 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data are stored in SBUF, the stop bit is stored in RB8, and the RI flag is set. If these conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set. An interrupt will occur if enabled when either TI or RI is set.

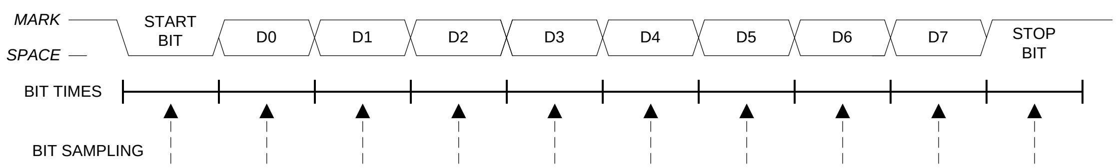


Figure 16.4. UART Mode 1 Timing Diagram

The baud rate generated in Mode 1 is a function of timer overflow. The UART can use Timer 1 operating in 8-bit Counter/Timer with Auto-Reload Mode, or Timer 2 operating in Baud Rate Generator Mode to generate the baud rate (note that the TX and RX clock sources are selected separately). On each timer overflow event (a rollover from all ones (0xFF for Timer 1, 0xFFFF for Timer 2) to zero), a clock is sent to the baud rate logic.

When Timer 1 is selected as a baud rate source, the SMOD bit (PCON.7) selects whether or not to divide the Timer 1 overflow rate by two. On reset, the SMOD bit is logic 0, thus selecting the lower speed baud rate by default. The SMOD bit affects the baud rate generated by Timer 1 as follows:

Mode 1 Baud Rate = (1 / 32) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 0).
Mode 1 Baud Rate = (1 / 16) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 1).

When Timer 2 is selected as a baud rate source, the baud rate generated by Timer 2 is as follows:

Mode 1 Baud Rate = (1 / 16) x T2_OVERFLOWRATE.

The Timer 1 overflow rate is determined by the Timer 1 clock source (T1CLK) and reload value (TH1). The frequency of T1CLK can be selected as SYSCLK, SYSCLK/12, or an external clock source. The Timer 1 overflow rate can be calculated as follows:

T1_OVERFLOWRATE = T1CLK / (256 – TH1).

For example, assume TMOD = 0x20.