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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f236-gqr

1. System Overview

The C8051F2xx is a family of fully integrated, mixed-signal System on a Chip MCU's available with a true 12-bit ('F206) multi-channel ADC, 8-bit multi-channel ADC ('F220/1/6 and 'F206), or without an ADC ('F230/1/6). Each model features an 8051-compatible microcontroller core with 8 kB of Flash memory. There are also UART and SPI serial interfaces implemented in hardware (not "bit-banged" in user software). Products in this family feature 22 or 32 general purpose I/O pins, some of which can be used for assigned digital peripheral interface. Any pins may be configured for use as analog input to the analog-to-digital converter ('F220/1/6 and 'F206 only). (See the Product Selection Guide in Table 1.1 for a quick reference of each MCUs' feature set.)

Other features include an on-board V_{DD} monitor, WDT, and clock oscillator. On-board Flash memory can be reprogrammed in-circuit, and may also be used for non-volatile data storage. Integrated peripherals can also individually shut down any or all of the peripherals to conserve power. All parts have 256 bytes of SRAM. Also, an additional 1024 bytes of RAM is available in the 'F206/226/236.

On-board JTAG debug support allows non-intrusive (uses no on-chip resources), full speed, in-circuit debug using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, run and halt commands. All analog and digital peripherals are fully functional when emulating using JTAG.

Each MCU is specified for 2.7 to 3.6 V operation over the industrial temperature range (–45 to +85 °C) and is available in the 48-pin TFQP and 32-pin LFQP. The Port I/Os are tolerant for input signals up to 5 V.

Table 1.1. Product Selection Guide

	MIPS (Peak)	Flash Memory	RAM	SPI	UART	Timers (16-bit)	Digital Port I/O's	ADC Resolution (bits)	ADC Max Speed (ksps)	ADC Inputs	Voltage Comparators	Package
C8051F206	25	8 k	1280	✓	✓	3	32	12	100	32	2	48TQFP
C8051F220	25	8 k	256	✓	✓	3	32	8	100	32	2	48TQFP
C8051F221	25	8 k	256	✓	✓	3	22	8	100	22	2	32LQFP
C8051F226	25	8 k	1280	✓	✓	3	32	8	100	32	2	48TQFP
C8051F230	25	8 k	256	✓	✓	3	32	—	—	—	2	48TQFP
C8051F231	25	8 k	256	✓	✓	3	22	—	—	—	2	32LQFP
C8051F236	25	8 k	1280	✓	✓	3	32	—	—	—	2	48TQFP

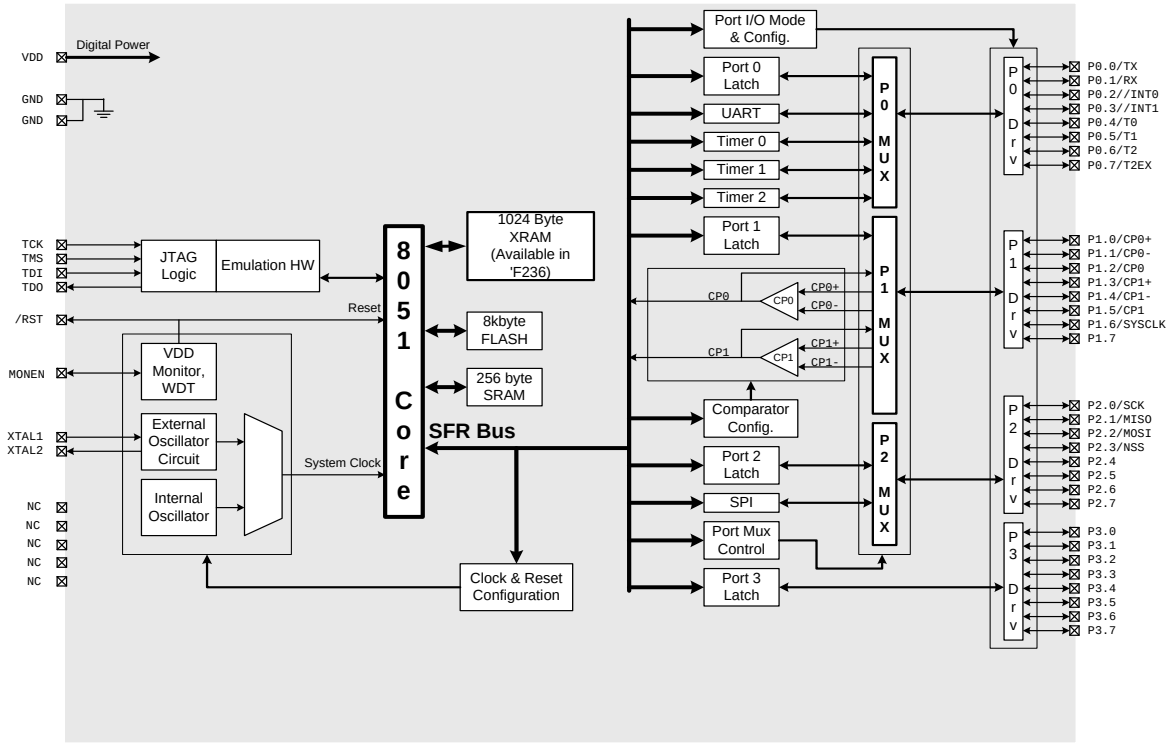


Figure 1.3. C8051F230 and C8051F236 Block Diagram (48 TQFP)

3. Global DC Electrical Characteristics

Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage[1]		2.7	3.0	3.6	V
V_{DD} supply current with ADC and comparators active, and CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	13 1.5 300	—	mA mA µA
V_{DD} supply current with ADC and comparators active, and CPU inactive (Idle Mode)	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	9 1.8 275	—	mA mA µA
V_{DD} supply current with ADC and comparators inactive, and CPU active	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	12.5 1.0 25	—	mA mA µA
Digital Supply Current with CPU inactive (Idle Mode)	Clock = 25 MHz Clock = 1 MHz Clock = 32 kHz	—	8.5 1.4 25	—	mA mA µA
Digital Supply Current (Stop Mode), V_{DD} monitor enabled	Oscillator not running	—	10	—	µA
Digital Supply Current (Stop Mode), V_{DD} monitor disabled	Oscillator not running	—	0.1	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
Specified Operating Temperature Range		–40	—	+85	°C
SYSCLK (system clock frequency)[2]		0	—	25	MHz
Tsysl (SYSCLK low time)		18	—	—	ns
Tsysh (SYSCLK high time)		18	—	—	ns

Notes:
1. Analog Supply AV+ must be greater than 1 V for V_{DD} monitor to operate.
2. SYSCLK must be at least 32 kHz to enable debugging.

SFR Definition 5.1. AMX0SL: AMUX Channel Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	AMXEN	PRTSL1	PRTSL0	PINSL2	PINSL1	PINSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

Bits 7–6: UNUSED. Read = 00b; Write = don't care
Bit 5: AMXEN enable
0: AMXEN disabled and port pins are unavailable for analog use.
1: AMXEN enabled to use/select port pins for analog use.
Bits 4–3: PRTSL1–0: Port Select Bits .
00: Port0 select to configure pin for analog input from this port.
01: Port1 select to configure pin for analog input from this port.
10: Port2 select to configure pin for analog input from this port.
11: Port3 select to configure pin for analog input from this port.
Bits 2–0:PINSL2–0: Pin Select Bits
000: Pin 0 of selected port (above) to be used for analog input.
001: Pin 1 of selected port (above) to be used for analog input.
010: Pin 2 of selected port (above) to be used for analog input.
011: Pin 3 of selected port (above) to be used for analog input.
100: Pin 4 of selected port (above) to be used for analog input.
101: Pin 5 of selected port (above) to be used for analog input.
110: Pin 6 of selected port (above) to be used for analog input.
111: Pin 7 of selected port (above) to be used for analog input.

* Selecting a port for analog input does NOT default all pins of that port as analog input. After selecting a port for analog input, a pin must be selected using pin select bits (PINSL2–0). For example, after setting the AMXEN to ‘1’, setting PRTSL1–0 to “11”, and setting PINSL2–0 to “100” P3.4 is configured as analog input. All other Port 3 pins remain as GPIO pins. Also note that in order to use a port pin as analog input, its input mode should be set to *analog*. Please see section 14.2.

SFR Definition 6.1. AMX0SL: AMUX Channel Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	AMXEN	PRTSL1	PRTSL0	PINSL2	PINSL1	PINSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

Bits 7–6: UNUSED. Read = 00b; Write = don't care

Bit 5: AMXEN enable
0: AMXEN disabled and port pins are unavailable for analog use.
1: AMXEN enabled to use/select port pins for analog use.

Bits 4–3: PRTSL1–0: Port Select Bits*.
00: Port0 select to configure pin for analog input from this port.
01: Port1 select to configure pin for analog input from this port.
10: Port2 select to configure pin for analog input from this port.
11: Port3 select to configure pin for analog input from this port.

Bits 2–0:PINSL2–0: Pin Select Bits
000: Pin 0 of selected port (above) to be used for analog input.
001: Pin 1 of selected port (above) to be used for analog input.
010: Pin 2 of selected port (above) to be used for analog input.
011: Pin 3 of selected port (above) to be used for analog input.
100: Pin 4 of selected port (above) to be used for analog input.
101: Pin 5 of selected port (above) to be used for analog input.
110: Pin 6 of selected port (above) to be used for analog input.
111: Pin 7 of selected port (above) to be used for analog input.

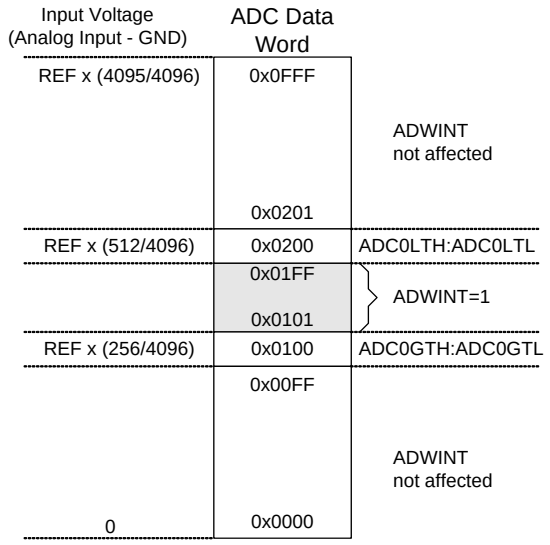
* Selecting a port for analog input does NOT default all pins of that port as analog input. After selecting a port for analog input, a pin must be selected using pin select bits (PINSL2–0). For example, after setting the AMXEN to '1', setting PRTSL1–0 to "11", and setting PINSL2–0 to "100" P3.4 is configured as analog input. All other Port 3 pins remain as GPIO pins. Also note that in order to use a port pin as analog input, its input mode should be set to *analog*. Please see section 14.2.

SFR Definition 6.9. ADC0LTL: ADC Less-Than Data Low Byte (C8051F206)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xC4

Bits7–0:
These bits are the low byte of the ADC Less-Than Data Word.

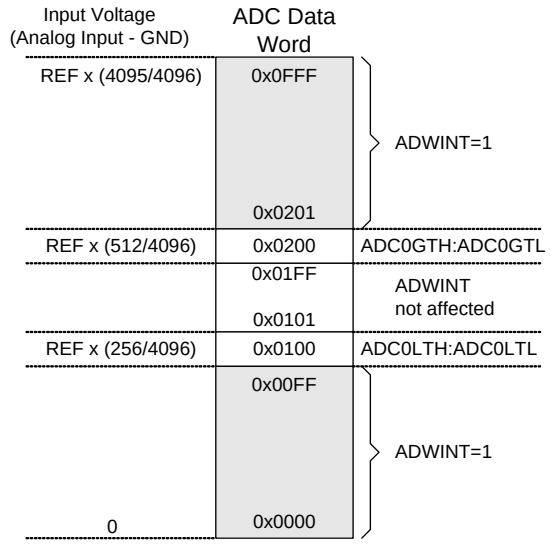
Definition:
ADC Less-Than Data Word = ADC0LTH:ADC0LTL



Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0, ADC0LTH:ADC0LTL = 0x0200, ADC0GTH:ADC0GTL = 0x0100.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0200 and > 0x0100.

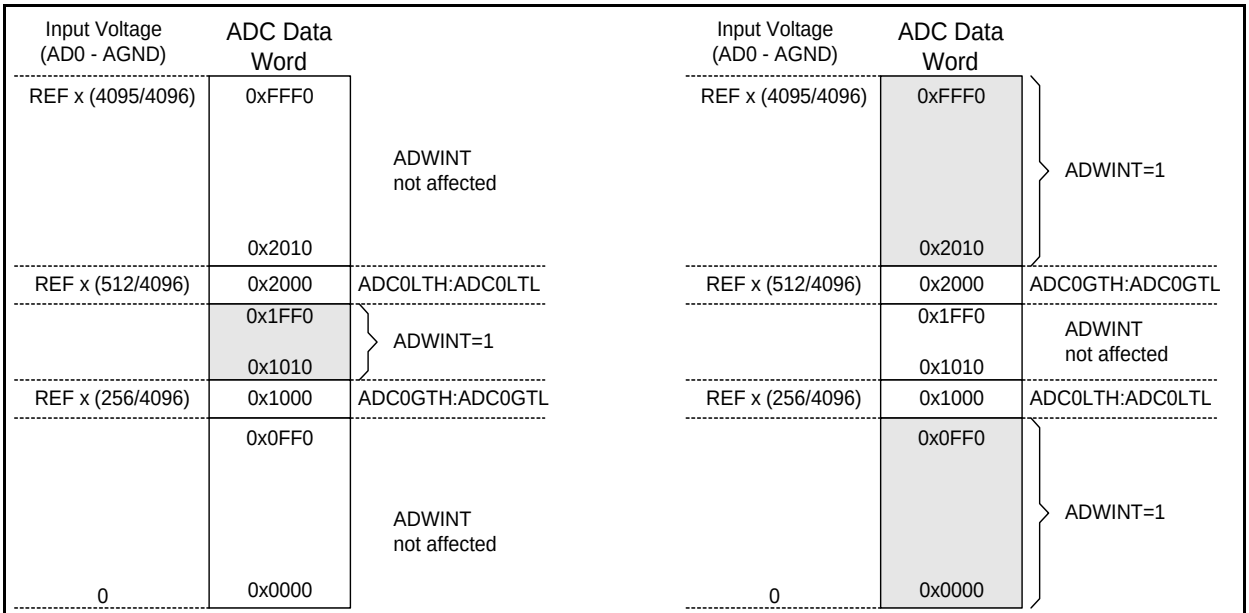


Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 0, ADC0LTH:ADC0LTL = 0x0100, ADC0GTH:ADC0GTL = 0x0200.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x0100 or > 0x0200.

Figure 6.3. 12-Bit ADC Window Interrupt Examples, Right Justified Data



Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1, ADC0LTH:ADC0LTL = 0x2000, ADC0GTH:ADC0GTL = 0x1000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x2000 and > 0x1000.

Given:

AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1, ADC0LTH:ADC0LTL = 0x1000, ADC0GTH:ADC0GTL = 0x2000.

An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x1000 or > 0x2000.

Figure 6.4. 12-Bit ADC Window Interrupt Examples, Left Justified Data

Table 6.1. 12-Bit ADC Electrical Characteristics (C8015F206 only)

V_{DD} = 3.0 V, VREF = 2.40 V (REFBE=0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	±1	±2	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±2	LSB
Offset Error		±20	±5	—	LSB
Full Scale Error	Differential mode	—	—	–20±10	LSB
Offset Temperature Coefficient		—	±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to –1 dB of full scale, 100 ksps)					
Signal-to-Noise Plus Distortion		63	66	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	–60	–72	—	dB
Spurious-Free Dynamic Range		60	76	—	dB
Conversion Rate					
Conversion Time in SAR Clocks		16	—	—	clocks
SAR Clock Frequency		—	—	2.0	MHz
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Voltage Conversion Range		0	—	VREF	V
Input Voltage	Any pin (in Analog Input Mode)	GND	—	V_{DD}	V
Input Capacitance		—	10	—	pF
Power Specifications					
Power Supply Current (V_{DD} supplied to ADC)	Operating Mode, 100 ksps	—	0.45	1.0	mA
Power Supply Rejection		—	±0.3	—	mV/V

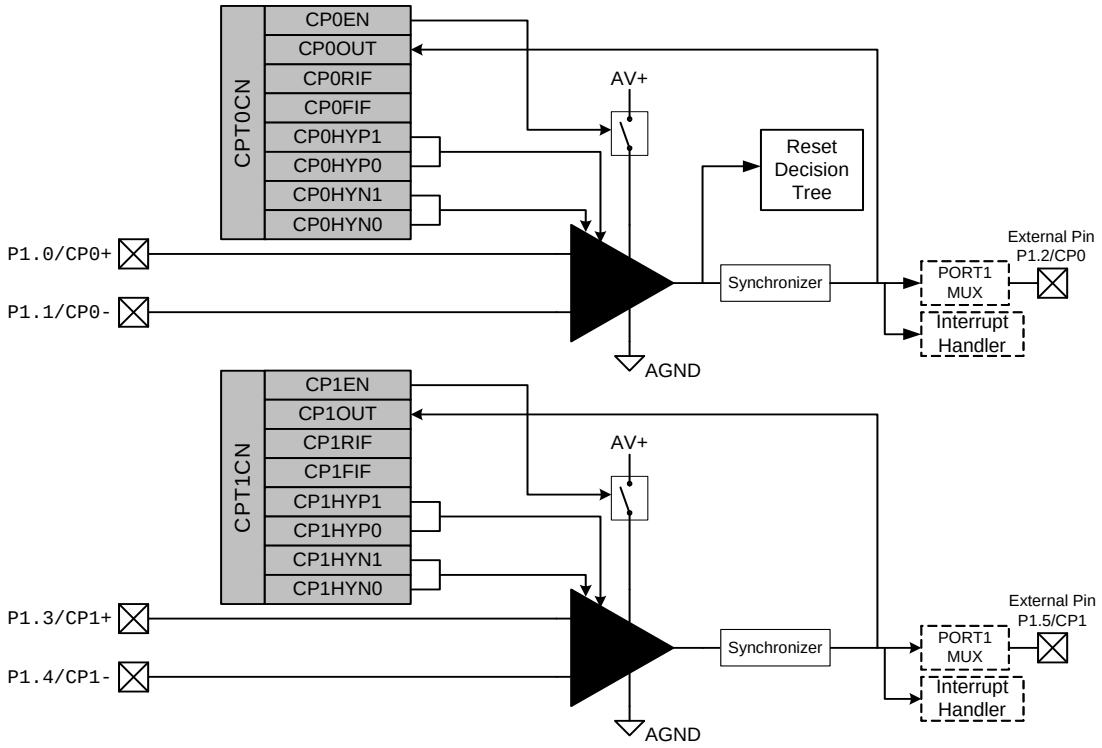


Figure 8.1. Comparator Functional Block Diagram

Performance

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute, and usually have a maximum system clock of 12MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with no instructions taking more than eight system clock cycles.

With the CIP-51's maximum system clock at 25MHz, it has a peak throughput of 25MIPS. The CIP-51 has a total of 109 instructions. The number of instructions versus the system clock cycles required to execute them is as follows:

Instructions	26	50	5	14	7	3	1	2	1
Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8

Programming and Debugging Support

A JTAG-based serial interface is provided for in-system programming of the Flash program memory and communication with on-chip debug support logic. The re-programmable Flash can also be read and changed a single byte at a time by the application software using the MOVC and MOVX instructions. This feature allows program memory to be used for non-volatile data storage as well as updating program code under software control.

The on-chip debug support circuitry facilitates full speed in-circuit debugging, allowing the setting of hardware breakpoints and watchpoints, starting, stopping and single stepping through program execution (including interrupt service routines), examination of the program's call stack, and reading/writing the contents of registers and memory. This method of on-chip debugging is completely non-intrusive and non-invasive, requiring no RAM, Stack, timers, or other on-chip resources.

The CIP-51 is supported by development tools from Silicon Laboratories and third party vendors. Silicon Labs provides an integrated development environment (IDE) including editor, macro assembler, debugger and programmer. The IDE's debugger and programmer interface to the CIP-51 via its JTAG interface to provide fast and efficient in-system device programming and debugging. Third party macro assemblers and C compilers are also available.

Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
MOV A,#data	Move immediate to A	2	2
MOV Rn,A	Move A to register	1	1
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate to register	2	2
MOV direct,A	Move A to direct byte	2	2
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct	3	3
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate to direct byte	3	3
MOV @Ri,A	Move A to indirect RAM	1	2
MOV @Ri,direct	Move direct byte to indirect RAM	2	2
MOV @Ri,#data	Move immediate to indirect RAM	2	2
MOV DPTR,#data16	Load data pointer with 16-bit constant	3	3
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	3
MOVC A,@A+PC	Move code byte relative PC to A	1	3
MOVX A,@Ri	Move external data (8-bit address) to A	1	3
MOVX @Ri,A	Move A to external data (8-bit address)	1	3
MOVX A,@DPTR	Move external data (16-bit address) to A	1	3
MOVX @DPTR,A	Move A to external data (16-bit address)	1	3
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte from stack	2	2
XCH A,Rn	Exchange register with A	1	1
XCH A,direct	Exchange direct byte with A	2	2
XCH A,@Ri	Exchange indirect RAM with A	1	2
XCHD A,@Ri	Exchange low nibble of indirect RAM with A	1	2
Boolean Manipulation			
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	2
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	2
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	2
ANL C,bit	AND direct bit to carry	2	2
ANL C,/bit	AND complement of direct bit to carry	2	2
ORL C,bit	OR direct bit to carry	2	2
ORL C,/bit	OR complement of direct bit to carry	2	2
MOV C,bit	Move direct bit to carry	2	2
MOV bit,C	Move carry to direct bit	2	2
JC rel	Jump if carry is set	2	2/3

9.2. Memory Organization

The memory organization of the CIP-51 System Controller is similar to that of a standard 8051. There are two separate memory spaces: program memory and data memory. Program and data memory share the same address space but are accessed via different instruction types. There are 256 bytes of internal data memory and 8 kB of internal program memory address space implemented within the CIP-51. The CIP-51 memory organization is shown in Figure 9.2.

9.2.1. Program Memory

The CIP-51 has a 8 kB program memory space. The MCU implements 8320 bytes of this program memory space as in-system, reprogrammable Flash memory, organized in a contiguous block from addresses 0x0000 to 0x207F. Note: 512 bytes (0x1E00 – 0x1FFF) of this memory are reserved for factory use and are not available for user program storage.

Program memory is normally assumed to be read-only. However, the CIP-51 can write to program memory by setting the Program Store Write Enable bit (PSCTL.0) and using the MOVX instruction. This feature provides a mechanism for the CIP-51 to update program code and use the program memory space for non-volatile data storage. Refer to Section 10 Flash Memory for further details.

9.2.2. Data Memory

The CIP-51 implements 256 bytes of internal RAM mapped into the data memory space from 0x00 through 0xFF. The lower 128 bytes of data memory are used for general purpose registers and memory. Either direct or indirect addressing may be used to access the lower 128 bytes of data memory. Locations 0x00 through 0x1F are addressable as four banks of general purpose registers, each bank consisting of eight byte-wide registers. The next 16 bytes, locations 0x20 through 0x2F, may either be addressed as bytes or as 128 bit locations accessible with the direct bit addressing mode.

The upper 128 bytes of data memory are accessible only by indirect addressing. This region occupies the same address space as the Special Function Registers (SFR) but is physically separate from the SFR space. The addressing mode used by an instruction when accessing locations above 0x7F determines whether the CPU accesses the upper 128 bytes of data memory space or the SFRs. Instructions that use direct addressing will access the SFR space. Instructions using indirect addressing above 0x7F will access the upper 128 bytes of data memory. Figure 9.2 illustrates the data memory organization of the CIP-51.

Additionally, the C8051F206/226/236 feature 1024 Bytes of RAM mapped in the external data memory space. All address locations may be accessed using the MOVX instruction. (Please see Section 11).

Table 9.3. Special Function Registers (Continued)

SFR's are listed in alphabetical order.

Address	Register	Description	Page No.
0xA4	PRT0CF	Port 0 Configuration	105
0xA5	PRT1CF	Port 1 Configuration	106
0xA6	PRT2CF	Port 2 Configuration	107
0xA7	PRT3CF	Port 3 Configuration	108
0xE1	PRT0MX	Port 0 Multiplexer I/O Configuration	103
0xE2	PRT1MX	Port 1 Multiplexer I/O Configuration	104
0xE3	PRT2MX	Port 2 Multiplexer I/O Configuration	104
0x8F	PSCTL	Program Store RW Control	88
0xD0	PSW	Program Status Word	72
0xCB	RCAP2H	Counter/Timer 2 Capture (High Byte)	138
0xCA	RCAP2L	Counter/Timer 2 Capture (Low Byte)	138
0xD1	REF0CN	Voltage Reference Control Register	50
0xEF	RSTSRC	Reset Source Register	95
0x99	SBUF	Serial Data Buffer (UART)	123
0x98	SCON	Serial Port Control (UART)	124
0x81	SP	Stack Pointer	71
0x9A	SPI0CFG	Serial Peripheral Interface Configuration	114
0x9D	SPI0CKR	SPI Clock Rate	116
0xF8	SPI0CN	SPI Bus Control	115
0x9B	SPI0DAT	SPI Port 1Data	116
0xAD	SWCINT	Software Controlled Interrupt Register	75
0xC8	T2CON	Counter/Timer 2 Control	137
0x88	TCON	Counter/Timer Control	129
0x8C	TH0	Counter/Timer 0 Data Word (High Byte)	132
0x8D	TH1	Counter/Timer 1 Data Word (High Byte)	132
0xCD	TH2	Counter/Timer 2 Data Word (High Byte)	138
0x8A	TL0	Counter/Timer 0 Data Word (Low Byte)	132
0x8B	TL1	Counter/Timer 1 Data Word (Low Byte)	132
0xCC	TL2	Counter/Timer 2 Data Word (Low Byte)	138
0x89	TMOD	Counter/Timer Mode	130
0xFF	WDTCN	Watchdog Timer Control	94
0x84–86, 0x91–97, 0x9C, 0xA1–A3, 0xA9–AC, 0xAE, 0xB3–B5, 0xB9–BA, 0xBD–BE,0xC0–C4, 0xC6,0xCE–CF,0xD2–DF,0xE9–EE,0xF5,0xF9–FE	Reserved		

Notes:

1. C8051F230/1/6 Do not have these registers.
2. C8051F221/231 Does not have this register (32 pin package).
3. On the C8051F206 and C8051F226/236 only.
4. On the C8051F206 only (12-bit ADC)

Table 9.4. Interrupt Summary (Continued)

Interrupt Source	Interrupt Vector	Priority Order	Interrupt-Pending Flag	Enable
ADC0 End of Conversion	0x007B	15	ADCINT (ADC0CN.5)	EADC0 (EIE2.1)
Software Controlled Interrupt 0	0x0083	16	SCI0 (SWCINT.4)	ESCI0 (EIE2.2)
Software Controlled Interrupt 1	0x008B	17	SCI1 (SWCINT.5)	ESCI1 (EIE2.3)
Software Controlled Interrupt 2	0x0093	18	SCI2 (SWCINT.6)	ESCI2 (EIE2.4)
Software Controlled Interrupt 3	0x009B	19	SCI3 (SWCINT.7)	ESCI3 (EIE2.5)
Unused Interrupt Location	0x00A3	20	None	Reserved (EIE2.6)
External Crystal OSC Ready	0x00AB	21	XTLVLD (OSCXCN.7)	EXVLD (EIE2.7)

9.4.4. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. Each interrupt has an associated interrupt priority bit in an SFR (IP–EIP2) used to configure its priority level. Low priority is the default. If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate.

9.4.5. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 5 system clock cycles: 1 clock cycle to detect the interrupt and 4 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 18 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 4 clock cycles to execute the LCALL to the ISR. NOTE: If a Flash write or erase is performed, the MCU is stalled during the operation and interrupts will not be serviced until the operation is complete. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

SFR Definition 14.15. P3MODE: Port3 Digital/Analog Input Mode*

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF4

Bits7–0: Port3 Digital/Analog Output Mode
0: Corresponding Port3 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port3 pin Digital Input is enabled.

* (Available on C8051F206, C8051F220/6 and C8051F230/6)

Table 14.1. Port I/O DC Electrical Characteristics

V_{DD} = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage	I_{OH} = –10 uA, Port I/O push-pull I_{OH} = –3 mA, Port I/O push-pull I_{OH} = –10 mA, Port I/O push-pull	V_{DD} – 0.1 V_{DD} – 0.7	 V_{DD} – 0.8		V
Output Low Voltage	I_{OL} = 10 uA I_{OL} = 8.5 mA I_{OL} = 25 mA		 1.0	0.1 0.6	V
Input High Voltage		0.7 x V_{DD}			V
Input Low Voltage				0.3 x V_{DD}	V
Input Leakage Current	DGND < Port Pin < V_{DD}, Pin Tri-state Weak Pull-up Off Weak Pull-up On		 30	±1	µA
Capacitive Loading			3		pF

SFR Definition 15.2. SPI0CN: SPI Control

R/W	R/W	R/W	R/W	R	R	R/W	R/W	Reset Value
SPIF	WCOL	MODF	RXOVRN	TXBSY	SLVSEL	MSTEN	SPIEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF8

Bit7: SPIF: SPI Interrupt Flag.
This bit is set to logic 1 by hardware at the end of a data transfer. If interrupts are enabled, setting this bit causes the CPU to vector to the SPI0 interrupt service routine. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit6: WCOL: Write Collision Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) to indicate a write to the SPI data register was attempted while a data transfer was in progress. It is cleared by software.

Bit5: MODF: Mode Fault Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when a master mode collision is detected (NSS is low and MSTEN = 1). This bit is not automatically cleared by hardware. It must be cleared by software.

Bit4: RXOVRN: Receive Overrun Flag.
This bit is set to logic 1 by hardware (and generates a SPI interrupt) when the receive buffer still holds unread data from a previous transfer and the last bit of the current transfer is shifted into the SPI shift register. This bit is not automatically cleared by hardware. It must be cleared by software.

Bit3: TXBSY: Transmit Busy Flag.
This bit is set to logic 1 by hardware while a master mode transfer is in progress. It is cleared by hardware at the end of the transfer.

Bit2: SLVSEL: Slave Selected Flag.
This bit is set to logic 1 whenever the NSS pin is low indicating it is enabled as a slave. It is cleared to logic 0 when NSS is high (slave disabled).

Bit1: MSTEN: Master Mode Enable.
0: Disable master mode. Operate in slave mode.
1: Enable master mode. Operate as a master.

Bit0: SPIEN: SPI Enable.
This bit enables/disables the SPI.
0: SPI disabled.
1: SPI enabled.

SFR Definition 17.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x89

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic level one.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin P0.5/T1.

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 Inactive/stopped

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic level one.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin P0.4/T0.

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

18. JTAG

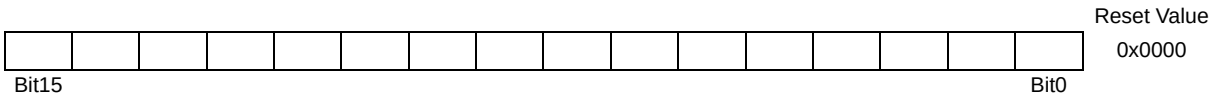
Description

The MCU has an on-chip JTAG interface and logic to support Flash read and write operations and non-intrusive in-circuit debug. The C8051F2xx may be placed in a JTAG test chain in order to maintain only one JTAG interface in a system for boundary scan of other parts, and still utilize the C8051F2xx debug and Flash programming. However, the C8051F2xx does NOT support boundary scan and will act as BYPASS as specified in IEEE 1149.1.

The JTAG interface is implemented via four dedicated pins on the MCU, which are TCK, TMS, TDI, and TDO. These pins are all 5 volt tolerant.

Through the 16-bit JTAG Instruction Register (IR), five instructions shown in JTAG Register Definition 18.1 can be commanded. These commands can either select the device ID code, or select registers for Flash programming operations. BYPASS is shown to illustrate its default setting. There are four Data Registers associated with the Flash read and write operations on the MCU.

JTAG Register Definition 18.1. IR: JTAG Instruction



IR value	Instruction	Description
0x0004	IDCODE	Selects device ID Register
0xFFFF	BYPASS	Selects bypass Data Register and is DEFAULT for the device. Note: The device does NOT support boundary scan. However, it may be placed in a scan chain and bypassed in a system of other devices utilizing boundary scan.
0x0082	Flash Control	Selects FLASHCON Register to control how the interface logic responds to reads and writes to the FLASHDAT Register
0x0083	Flash Data	Selects FLASHDAT Register for reads and writes to the Flash memory
0x0084	Flash Address	Selects FLASHADR Register which holds the address of all Flash read, write, and erase operations
0x0085	Flash Scale	Selects FLASHSCL Register which controls the prescaler used to generate timing signals for Flash operations

18.2. Boundary Scan Bypass and ID Code

The MCU does not support boundary scan (IEEE 1149.1), however, it does support the bypass and ID code functions. Because the MCU utilizes JTAG for Flash memory programming and debug support, and other devices in a system may use JTAG boundary scan, the MCU supports being placed in BYPASS so the user may maintain a single JTAG port for a system. Additionally, the MCU supports an ID code.

18.2.1. BYPASS Instruction

The BYPASS instruction is accessed via the IR. It provides access to the standard 1-bit JTAG Bypass data register.

18.2.2. IDCODE Instruction

The IDCODE instruction is accessed via the IR. It provides access to the 32-bit Device ID register.

JTAG Register Definition 18.6. DEVICEID: JTAG Device ID

Version	Part Number	Manufacturer ID	1	Reset Value
Bit31 Bit28	Bit27 Bit12	Bit11 Bit1	Bit0	0xn0000243

Version = 0000b (Revision A)
= 0001b (Revision B)

Part Number = 0000 0000 0000 0001b (C8051F206/220/1/6, C8051F230/1/6)

Manufacturer ID = 0010 0100 001b (Silicon Laboratories)

18.3. Debug Support

The MCU has on-chip JTAG and debug circuitry that provide non-intrusive, full speed, in-circuit debug using the production part installed in the end application using the four pin JTAG I/F. Silicon Labs' debug system supports inspection and modification of memory and registers, breakpoints, stack tracing, and single stepping. No additional target RAM, program memory, or communications channels are required. All the digital and analog peripherals are functional and work correctly (remain in sync) while emulating. The WDT is disabled when the MCU is halted during single stepping or at a breakpoint.

The C8051F2xxDK is a development kit with all the hardware and software necessary to develop application code and perform in-circuit debugging with the C8061F206, C8051F220/1/6 and C8051F230/1/6. The kit includes an Integrated Development Environment (IDE) which has a debugger and integrated 8051 assembler. It has an RS-232 to JTAG interface module referred to as the EC. The kit also includes RS-232 and JTAG cables, and wall-mount power supply.

DOCUMENT CHANGE LIST

Revision 1.5 to Revision 1.6

- Table 3.1 on page 24 corrected to show 32 kHz instead of 32 MHz.