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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f236r

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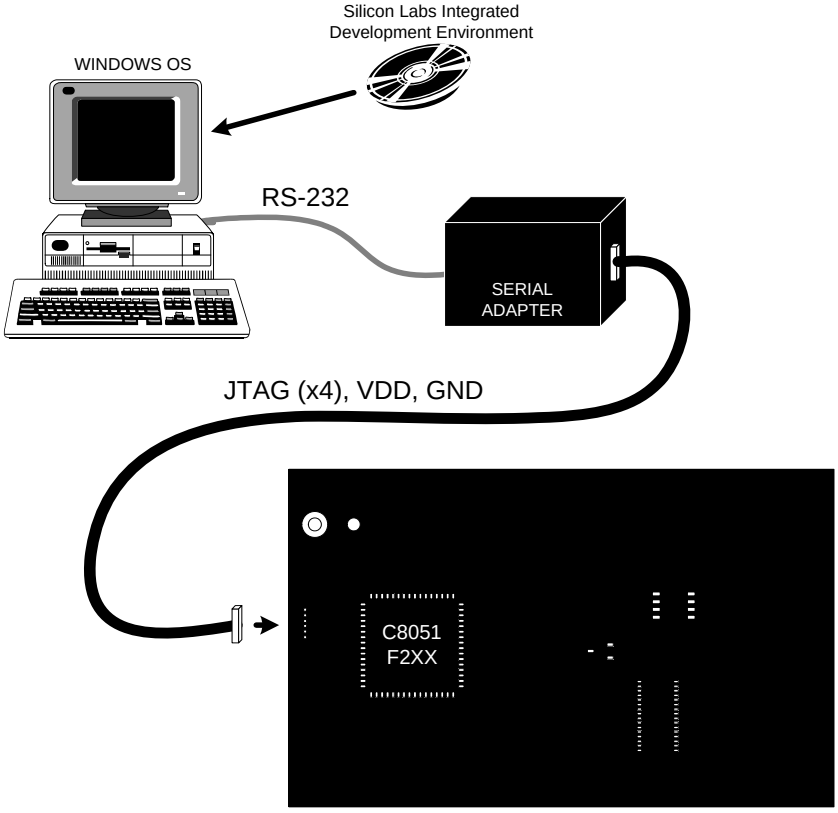

Figure 1.8. Degub Environment Diagram

1.4. Digital/Analog Configurable I/O

The standard 8051 Ports (0, 1, 2, and 3) are available on the device. The ports behave like standard 8051 ports with a few enhancements.

Each port pin can be configured as either a push-pull or open-drain output. Any input that is configured as an analog input will have its corresponding weak pull-up turned off.

Digital resources (timers, SPI, UART, system clock, and comparators) are routed to corresponding I/O pins by configuring the port multiplexer. Port multiplexers are programmed by setting bits in SFR's (please see Section 14). Any of the 32 external port pins may be configured as either analog inputs or digital I/O (See Figure 1.9), so effectively, all port pins are dual function.

SFR Definition 5.1. AMX0SL: AMUX Channel Select

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	AMXEN	PRTSL1	PRTSL0	PINSL2	PINSL1	PINSL0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xBB

Bits 7–6: UNUSED. Read = 00b; Write = don't care
Bit 5: AMXEN enable
0: AMXEN disabled and port pins are unavailable for analog use.
1: AMXEN enabled to use/select port pins for analog use.
Bits 4–3: PRTSL1–0: Port Select Bits .
00: Port0 select to configure pin for analog input from this port.
01: Port1 select to configure pin for analog input from this port.
10: Port2 select to configure pin for analog input from this port.
11: Port3 select to configure pin for analog input from this port.
Bits 2–0:PINSL2–0: Pin Select Bits
000: Pin 0 of selected port (above) to be used for analog input.
001: Pin 1 of selected port (above) to be used for analog input.
010: Pin 2 of selected port (above) to be used for analog input.
011: Pin 3 of selected port (above) to be used for analog input.
100: Pin 4 of selected port (above) to be used for analog input.
101: Pin 5 of selected port (above) to be used for analog input.
110: Pin 6 of selected port (above) to be used for analog input.
111: Pin 7 of selected port (above) to be used for analog input.

* Selecting a port for analog input does NOT default all pins of that port as analog input. After selecting a port for analog input, a pin must be selected using pin select bits (PINSL2–0). For example, after setting the AMXEN to ‘1’, setting PRTSL1–0 to “11”, and setting PINSL2–0 to “100” P3.4 is configured as analog input. All other Port 3 pins remain as GPIO pins. Also note that in order to use a port pin as analog input, its input mode should be set to *analog*. Please see section 14.2.

6.2. ADC Modes of Operation

The ADC has a maximum conversion speed of 100 ksps. The ADC conversion clock is derived from the system clock. The ADC conversion clock is derived from a divided version of SYSCLK. Divide ratios of 1, 2, 4, 8, or 16 are supported by setting the ADCSC bits in the ADC0CF Register. This is useful to adjust conversion speed to accommodate different system clock speeds.

A conversion can be initiated in one of two ways, depending on the programmed states of the ADC Start of Conversion Mode bits (ADSTM1, ADSTM0) in ADC0CN. Conversions may be initiated by:

1. Writing a 1 to the ADBUSY bit of ADC0CN;
2. A Timer 2 overflow (i.e. timed continuous conversions).

Writing a 1 to ADBUSY provides software control of the ADC whereby conversions are performed "on-demand". During conversion, the ADBUSY bit is set to 1 and restored to 0 when conversion is complete. The falling edge of ADBUSY triggers an interrupt (when enabled) and sets the ADCINT interrupt flag in the ADC0CN register. Note: When conversions are performed "on-demand", the ADCINT flag, not ADBUSY, should be polled to determine when the conversion has completed. Converted data is available in the ADC data word register, ADC0H.

The ADCTM bit in register ADC0CN controls the ADC track-and-hold mode. In its default state, the ADC input is continuously tracked, except when a conversion is in progress. Setting ADCTM to 1 allows one of two different low power track-and-hold modes to be specified by states of the ADSTM1-0 bits (also in ADC0CN):

1. Tracking begins with a write of 1 to ADBUSY and lasts for 3 SAR clocks;
2. Tracking starts with an overflow of Timer 2 and lasts for 3 SAR clocks.

Tracking can be disabled (shutdown) when the entire chip is in low power standby or sleep modes.

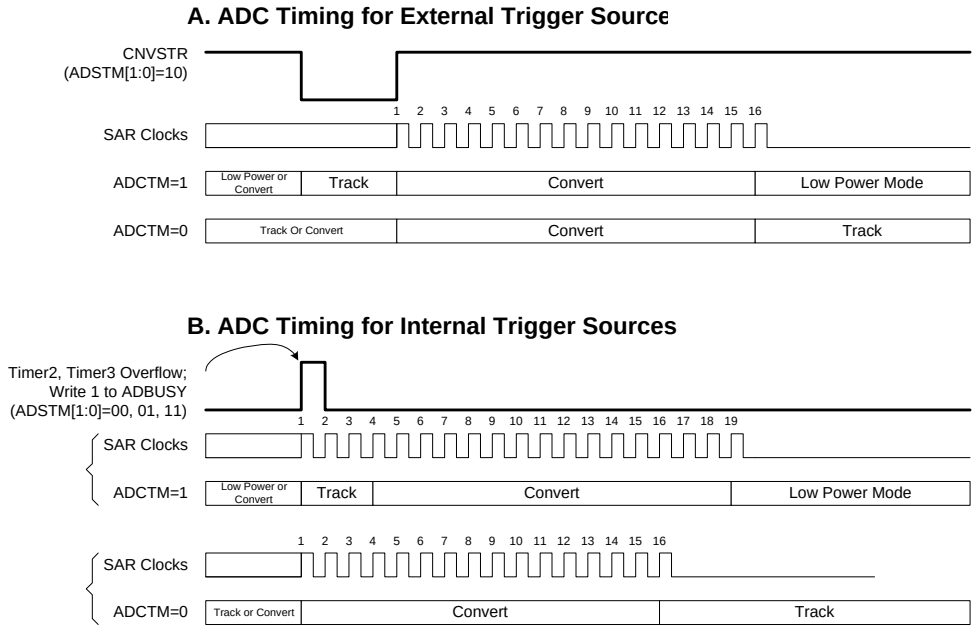

Figure 6.2. 12-Bit ADC Track and Conversion Example Timing

Table 9.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
JNC rel	Jump if carry not set	2	2/3
JB bit,rel	Jump if direct bit is set	3	3/4
JNB bit,rel	Jump if direct bit is not set	3	3/4
JBC bit,rel	Jump if direct bit is set and clear bit	3	3/4
Program Branching			
ACALL addr11	Absolute subroutine call	2	3
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	5
RETI	Return from interrupt	1	5
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A+DPTR	Jump indirect relative to DPTR	1	3
JZ rel	Jump if A equals zero	2	2/3
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A,direct,rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A,#data,rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn,#data,rel	Compare immediate to register and jump if not equal	3	3/4
CJNE @Ri,#data,rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn,rel	Decrement register and jump if not zero	2	2/3
DJNZ direct,rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:
Rn - Register R0–R7 of the currently selected register bank. **@Ri -** Data RAM location addressed indirectly through register R0–R1 **rel -** 8-bit, signed (two's compliment) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps. **direct -** 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00–0x7F) or an SFR (0x80–0xFF). **#data -** 8-bit constant **#data 16 -** 16-bit constant **bit -** Direct-addressed bit in Data RAM or SFR. **addr 11 -** 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2 kB page of program memory as the first byte of the following instruction. **addr 16 -** 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 8 kB program memory space. There is one unused opcode (0xA5) that performs the same function as NOP. All mnemonics copyrighted © Intel Corporation 1980.

Table 9.3. Special Function Registers

SFR's are listed in alphabetical order.

Address	Register	Description	Page No.
0xE0	ACC	Accumulator	73
0xBC	ADC0CF	ADC Configuration	35
0xE8	ADC0CN	ADC Control	36
0xC5	ADC0GTH[1]	ADC Greater-Than Data Word (High Byte)	37
0xC4	ADC0GTL[4]	ADC Greater-Than Data Word (Low Byte)	46
0xBF	ADC0H[1]	ADC Data Word (High Byte)	37
0xBE	ADC0L[4]	ADC Data Word (Low Byte)	45
0xC7	ADC0LTH[1]	ADC Less-Than Data Word (High Byte)	46
0xCE	ADC0LTL[4]	ADC Less-Than Data Word (Low Byte)	47
0xBB	AMX0SL	ADC MUX Channel Selection	34
0xF0	B	B Register	73
0x8E	CKCON	Clock Control	131
0x9E	CPT0CN	Comparator 0 Control	55
0x9F	CPT1CN	Comparator 1 Control	56
0x83	DPH	Data Pointer (High Byte)	71
0x82	DPL	Data Pointer (Low Byte)	71
0xE6	EIE1	Extended Interrupt Enable 1	79
0xE7	EIE2	Extended Interrupt Enable 2	80
0xF6	EIP1	External Interrupt Priority 1	81
0xF7	EIP2	External Interrupt Priority 2	82
0xAF	EMI0CN[3]	External Memory Interface Control	90
0xB7	FLACL	Flash Memory Read Limit	89
0xB6	FLSCL	Flash Memory Timing Prescaler	89
0xA8	IE	Interrupt Enable	77
0xB8	IP	Interrupt Priority Control	78
0xB2	OSCICN	Internal Oscillator Control	98
0xB1	OSCXCN	External Oscillator Control	99
0x80	P0	Port 0 Latch	105
0x90	P1	Port 1 Latch	106
0xA0	P2	Port 2 Latch	107
0xB0	P3	Port 3 Latch	108
0xF1	P0MODE	Port0 Digital/Analog Output Mode	106
0xF2	P1MODE	Port1 Digital/Analog Output Mode	107
0xF3	P2MODE	Port2 Digital/Analog Output Mode	108
0xF4	P3MODE[2]	Port3 Digital/Analog Output Mode	109
0x87	PCON	Power Control	84

SFR Definition 9.4. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0xD0

Bit7: CY: Carry Flag.
This bit is set when the last arithmetic operation results in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: AC: Auxiliary Carry Flag.
This bit is set when the last arithmetic operation results in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: F0: User Flag 0.
This is a bit-addressable, general-purpose flag for use under software control.

Bits4–3: RS1–RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00–0x07
0	1	1	0x08–0x0F
1	0	2	0x10–0x17
1	1	3	0x18–0x1F

Note: Any instruction which changes the RS1–RS0 bits must not be immediately followed by the “MOV Rn, A” instruction.

Bit2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:
•An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
•A MUL instruction results in an overflow (result is greater than 255).
•A DIV instruction causes a divide-by-zero condition.
The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: PARITY: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

SFR Definition 9.10. EIE1: Extended Interrupt Enable 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ECP1R	ECP1F	ECP0R	ECP0F	-	EWADC0	-	ESPI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xE6

Bit7: ECP1R: Enable Comparator 1 (CP1) Rising Edge Interrupt.
This bit sets the masking of the CP1 interrupt.
0: Disable CP1 Rising Edge interrupt.
1: Enable interrupt requests generated by the CP1RIF flag (CPT1CN.3).

Bit6: ECP1F: Enable Comparator 1 (CP1) Falling Edge Interrupt.
This bit sets the masking of the CP1 interrupt.
0: Disable CP1 Falling Edge interrupt.
1: Enable interrupt requests generated by the CP1FIF flag (CPT1CN.4).

Bit5: ECP0R: Enable Comparator 0 (CP0) Rising Edge Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 Rising Edge interrupt.
1: Enable interrupt requests generated by the CP0RIF flag (CPT0CN.3).

Bit4: ECP0F: Enable Comparator 0 (CP0) Falling Edge Interrupt.
This bit sets the masking of the CP0 interrupt.
0: Disable CP0 Falling Edge interrupt.
1: Enable interrupt requests generated by the CP0FIF flag (CPT0CN.4).

Bit3: Reserved. Read = 0, Write = don't care.

Bit2: EWADC0: Enable Window Comparison ADC0 Interrupt.
This bit sets the masking of ADC0 window compare interrupt.
0: Disable ADC0 Window Comparison Interrupt.
1: Enable Interrupt requests generated by ADC0 Window Comparisons.

Bit1: Reserved. Read = 0, Write = don't care.

Bit0: ESPI0: Enable Serial Peripheral Interface 0 Interrupt.
This bit sets the masking of SPI0 interrupt.
0: Disable all SPI0 interrupts.
1: Enable Interrupt requests generated by SPI0.

SFR Definition 9.13. EIP2: Extended Interrupt Priority 2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PXVLD	-	PSCI3	PSCI2	PSCI1	PSCI0	PADC0	-	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF7

Bit7: PXVLD: External Clock Source Valid (XTLVLD) Interrupt Priority Control.
This bit sets the priority of the XTLVLD interrupt.
0: XTLVLD interrupt set to low priority level.
1: XTLVLD interrupt set to high priority level.

Bit6: Reserved. Must write 0. Reads 0.

Bit5: PSCI3: Software Controlled Interrupt 3 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 3.
0: External Interrupt 7 set to low priority level.
1: External Interrupt 7 set to high priority level.

Bit4: PSCI2: Software Controlled Interrupt 2 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 2.
0: Software Controlled Interrupt 2 set to low priority level.
1: Software Controlled Interrupt 2 set to high priority level.

Bit3: PSCI1: Software Controlled Interrupt 1 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 1.
0: Software Controlled Interrupt 1 set to low priority level.
1: Software Controlled Interrupt 1 set to high priority level.

Bit2: PSCI0: Software Controlled Interrupt 0 Priority Control.
This bit sets the priority of the Software Controlled Interrupt 0.
0: Software Controlled Interrupt 0 set to low priority level.
1: Software Controlled Interrupt 0 set to high priority level.

Bit1: PADC0: ADC End of Conversion Interrupt Priority Control.
This bit sets the priority of the ADC0 End of Conversion Interrupt.
0: ADC0 End of Conversion interrupt set to low priority level.
1: ADC0 End of Conversion interrupt set to high priority level.

Bit0: Reserved. Read = 0, Write = don't care.

down all digital peripherals. Each analog peripheral must be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to sleep for longer than the MCD timeout of 100µsec.

SFR Definition 9.14. PCON: Power Control Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SMOD	GF4	GF3	GF2	GF1	GF0	STOP	IDLE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x87

Bit7: SMOD: Serial Port Baud Rate Doubler Enable.
0: Serial Port baud rate is that defined by Serial Port Mode in SCON.
1: Serial Port baud rate is double that defined by Serial Port Mode in SCON.

Bits6–2: GF4–GF0: General Purpose Flags 4–0.
These are general purpose flags for use under software control.

Bit1: STOP: Stop Mode Select.
Setting this bit will place the CIP-51 in Stop mode. This bit will always be read as 0.
1: Goes into power down mode. (Turns off internal oscillator).

Bit0: IDLE: Idle Mode Select.
Setting this bit will place the CIP-51 in Idle mode. This bit will always be read as 0.
1: Goes into idle mode. (Shuts off clock to CPU, but clock to Timers, Interrupts, Serial Ports, and Analog Peripherals are still active.)

10. Flash Memory

This MCU includes 8 k + 128 bytes of on-chip, re-programmable Flash memory for program code and non-volatile data storage. The Flash memory can be programmed in-system, a single byte at a time, through the JTAG interface or by software using the MOVX instruction. Once cleared to 0, a Flash bit must be erased to set it back to 1. The bytes would typically be erased (set to 0xFF) before being reprogrammed. The write and erase operations are automatically timed by hardware for proper execution. Data polling to determine the end of the write/erase operation is not required. The Flash memory is designed to withstand at least 20,000 write/erase cycles. Refer to Table 10.1 for the electrical characteristics of the Flash memory.

10.1. Programming The Flash Memory

The simplest means of programming the Flash memory is through the JTAG interface using programming tools provided by Silicon Labs or a third party vendor. This is the only means for programming a non-initialized device. For details on the JTAG commands to program Flash memory, see Section 18.1.

The Flash memory can be programmed by software using the MOVX instruction with the address and data byte to be programmed provided as normal operands. Before writing to Flash memory using MOVX, flash write operations must be enabled by setting the PSWE Program Store Write Enable bit (PSCTL.0) to logic 1. Writing to Flash remains enabled until the PSWE bit is cleared by software.

To ensure the contents of the Flash contents, it is strongly recommended that the on-chip V_{DD} monitor be enabled (by tieing the MONEN pin 'high') in any application that writes and/or erases Flash memory from software.

Writes to Flash memory can clear bits but cannot set them. Only an erase operation can set bits in Flash. The byte location to be programmed must be erased before a new value can be written. The 8kbyte Flash memory is organized in 512-byte sectors. The erase operation applies to an entire sector (setting all bytes in the sector to 0xFF). Setting the PSEE Program Store Erase Enable bit (PSCTL.1) and PSWE Program Store Write Enable bit (PSCTL.0) to logic 1 and then using the MOVX command to write a data byte to any byte location within the sector will erase an entire 512-byte sector. The data byte written can be of any value because it is not actually written to the Flash. Flash erasure remains enabled until the PSEE bit is cleared by software. The following sequence illustrates the algorithm for programming the Flash memory by software:

1. Disable interrupts.
2. Enable Flash Memory write/erase in FLSCL Register using FLASCL bits.
3. Set PSEE (PSCTL.1) to enable Flash sector erase.
4. Set PSWE (PSCTL.0) to enable Flash writes.
5. Use MOVX to write a data byte to any location within the 512-byte sector to be erased.
6. Clear PSEE to disable Flash sector erase.
7. Use MOVX to write a data byte to the desired byte location within the erased 512-byte sector. Repeat until finished. (Any number of bytes can be written from a single byte to and entire sector.)
8. Clear the PSWE bit to disable Flash writes.

Write/Erase timing is automatically controlled by hardware based on the prescaler value held in the Flash Memory Timing Prescaler register (FLSCL). The 4-bit prescaler value FLASCL determines the time interval for write/erase operations. The FLASCL value required for a given system clock is shown in SFR Definition 10.2, along with the formula used to derive the FLASCL values. When FLASCL is set to 1111b, the

14.2. General Purpose Port I/O

Each I/O port is accessed through a corresponding special function register (SFR) that is both byte addressable and bit addressable. When writing to a port, the value written to the SFR is latched to maintain the output data value at each pin. When reading, the logic levels of the port's input pins are returned regardless of the PRTnMX settings (i.e., even when the pin is assigned to another signal by the MUX, the Port Register can always still read its corresponding Port I/O pin), provided its pin is configured for digital input mode. The exception to this is the execution of the *read-modify-write* instructions. The *read-modify-write* instructions when operating on a port SFR are the following: ANL, ORL, XRL, JBC, CPL, INC, DEC, DJNZ and MOV, CLR or SETB, when the destination is an individual bit in a port SFR. For these instructions, the value of the register (not the pin) is read, modified, and written back to the SFR.

SFR Definition 14.4. P0: Port0 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0x80

Bits7–0: P0.[7:0]
(Write - Output appears on I/O pins per PRT0MX, PRT1MX, and PRT2MX Registers)
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding PRT0CF.n bit = 0)
(Read - Regardless of PRT0MX, PRT1MX, and PRT2MX Register settings).
0: P0.n pin is logic low.
1: P0.n pin is logic high.

SFR Definition 14.5. PRT0CF: Port0 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA4

Bits7–0: PRT0CF.[7:0]: Output Configuration Bits for P0.7–P0.0 (respectively)
0: Corresponding P0.n Output mode is Open-Drain.
1: Corresponding P0.n Output mode is Push-Pull.

SFR Definition 14.6. P0MODE: Port0 Digital/Analog Input Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xF1

Bits7–0: Port0 Digital/Analog Input Mode
0: Corresponding Port0 pin Digital Input disabled. (For analog use, i.e., ADC).
1: Corresponding Port0 pin Digital Input is enabled.

SFR Definition 14.7. P1: Port1 Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0 (bit addressable)	SFR Address: 0x90

Bits7–0: P1.[7:0]
(Write - Output appears on I/O pins per PRT0MX, PRT1MX, and PRT2MX registers)
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding PRT1CF.n bit = 0)
(Read - Regardless of PRT0MX, PRT1MX, and PRT2MX Register settings).
0: P1.n pin is logic low.
1: P1.n pin is logic high.

SFR Definition 14.8. PRT1CF: Port1 Configuration Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0xA5

Bits7–0: PRT1CF.[7:0]: Output Configuration Bits for P1.7–P1.0 (respectively)
0: Corresponding P1.n Output Mode is Open-Drain.
1: Corresponding P1.n Output Mode is Push-Pull.

16.1.2. Mode 1: 8-Bit UART, Variable Baud Rate

Mode 1 provides standard asynchronous, full duplex communication using a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit (see the timing diagram in Figure 16.4). Data are transmitted from the TX pin and received at the RX pin (see the interconnection diagram in Figure 16.5). On receive, the eight data bits are stored in SBUF and the stop bit goes into RB8 (SCON.2).

Data transmission begins when an instruction writes a data byte to the SBUF register. The TI Transmit Interrupt Flag (SCON.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN Receive Enable bit (SCON.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF receive register if the following conditions are met: RI must be logic 0, and if SM2 is logic 1, the stop bit must be logic 1.

If these conditions are met, the eight bits of data are stored in SBUF, the stop bit is stored in RB8, and the RI flag is set. If these conditions are not met, SBUF and RB8 will not be loaded and the RI flag will not be set. An interrupt will occur if enabled when either TI or RI is set.

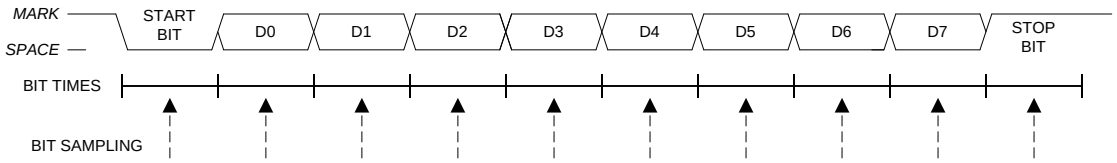

Figure 16.4. UART Mode 1 Timing Diagram

The baud rate generated in Mode 1 is a function of timer overflow. The UART can use Timer 1 operating in 8-bit Counter/Timer with Auto-Reload Mode, or Timer 2 operating in Baud Rate Generator Mode to generate the baud rate (note that the TX and RX clock sources are selected separately). On each timer overflow event (a rollover from all ones (0xFF for Timer 1, 0xFFFF for Timer 2) to zero), a clock is sent to the baud rate logic.

When Timer 1 is selected as a baud rate source, the SMOD bit (PCON.7) selects whether or not to divide the Timer 1 overflow rate by two. On reset, the SMOD bit is logic 0, thus selecting the lower speed baud rate by default. The SMOD bit affects the baud rate generated by Timer 1 as follows:

Mode 1 Baud Rate = (1 / 32) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 0).
Mode 1 Baud Rate = (1 / 16) x T1_OVERFLOWRATE (when the SMOD bit is set to logic 1).

When Timer 2 is selected as a baud rate source, the baud rate generated by Timer 2 is as follows:

Mode 1 Baud Rate = (1 / 16) x T2_OVERFLOWRATE.

The Timer 1 overflow rate is determined by the Timer 1 clock source (T1CLK) and reload value (TH1). The frequency of T1CLK can be selected as SYSCLK, SYSCLK/12, or an external clock source. The Timer 1 overflow rate can be calculated as follows:

T1_OVERFLOWRATE = T1CLK / (256 – TH1).

For example, assume TMOD = 0x20.

17.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. The TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0. Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0.

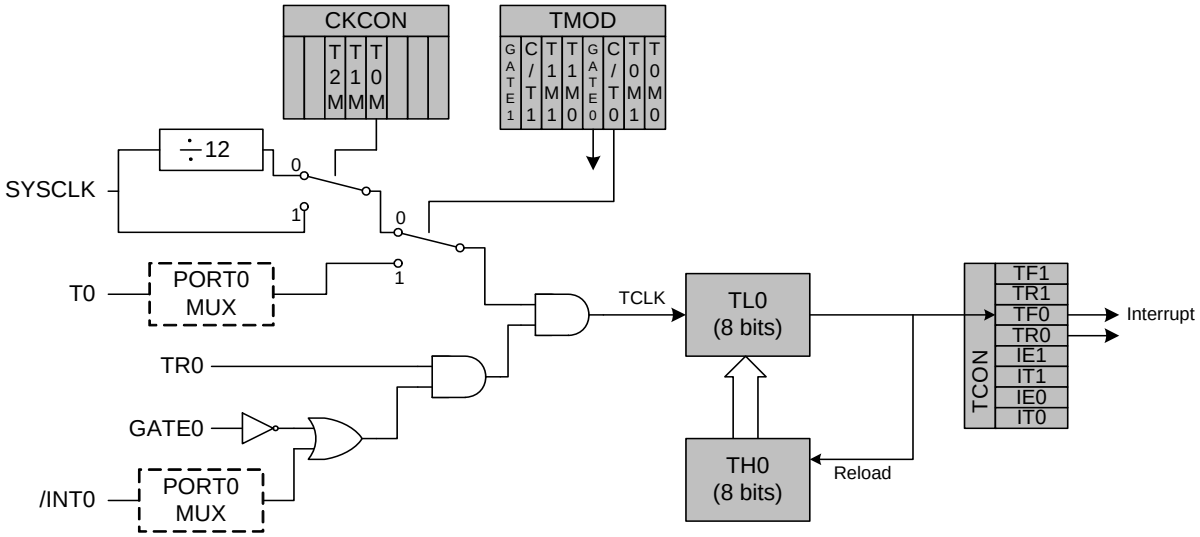

Figure 17.2. T0 Mode 2 Block Diagram

SFR Definition 17.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address: 0x88

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 input signal's logic level when IT1 = 0.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT1 is level triggered.
1: /INT1 is edge triggered.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 input signal's logic level when IT0 = 0.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 signal will detect falling edge or active-low level-sensitive interrupts.
0: /INT0 is level triggered.
1: /INT0 is edge triggered.

17.2.1. Mode 0: 16-bit Counter/Timer with Capture

In this mode, Timer 2 operates as a 16-bit counter/timer with capture facility. A high-to-low transition on the T2EX input pin causes the 16-bit value in Timer 2 (TH2, TL2) to be loaded into the capture registers (RCAP2H, RCAP2L).

Timer 2 can use either SYSCLK, SYSCLK divided by 12, or high-to-low transitions on the external T2 input pin as its clock source when operating in Counter/Timer with Capture mode. Clearing the C/T2 bit (T2CON.1) selects the system clock as the input for the timer (divided by one or twelve as specified by the Timer Clock Select bit T2M in CKCON). When C/T2 is set to logic 1, a high-to-low transition at the T2 input pin increments the counter/timer register. As the 16-bit counter/timer register increments and overflows from 0xFFFF to 0x0000, the TF2 timer overflow flag (T2CON.7) is set and an interrupt will occur if the interrupt is enabled.

Counter/Timer with Capture mode is selected by setting the Capture/Reload Select bit CP/RL2 (T2CON.0) and the Timer 2 Run Control bit TR2 (T2CON.2) to logic 1. The Timer 2 External Enable EXEN2 (T2CON.3) must also be set to logic 1 to enable a capture. If EXEN2 is cleared, transitions on T2EX will be ignored.

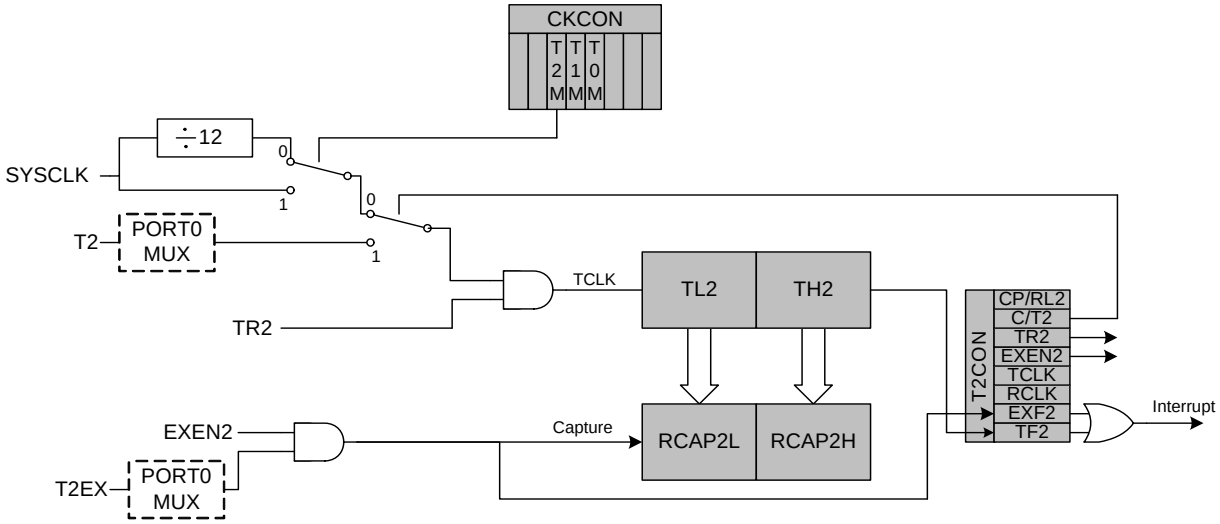

Figure 17.4. T2 Mode 0 Block Diagram