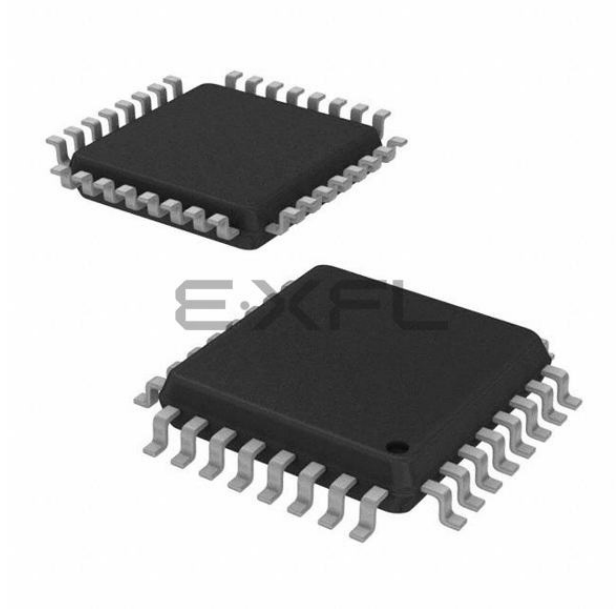


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f866kpmc-g-sne2

5.2 MB95860K Series

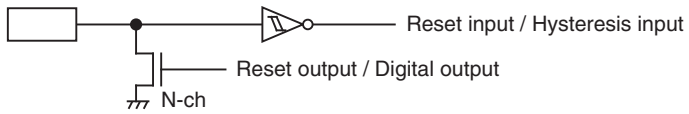
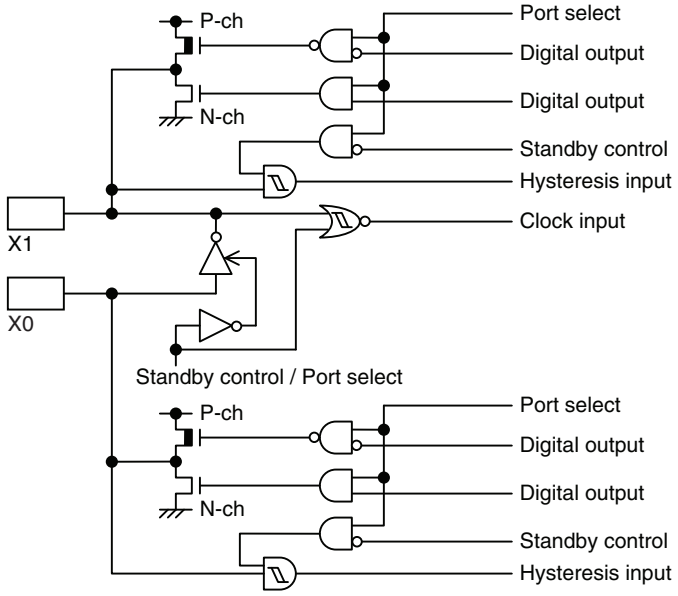
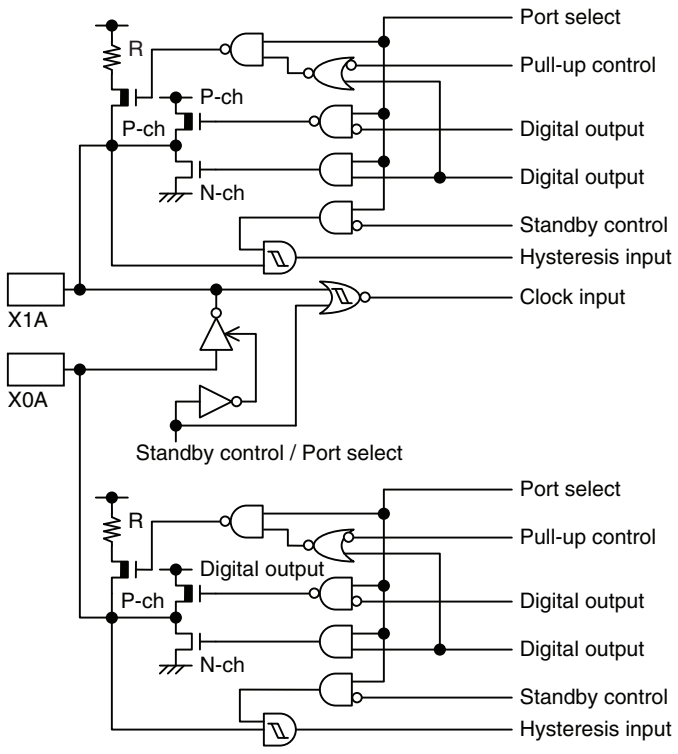
Pin no.	Pin name	I/O circuit type[4]	Function	I/O type			
				Input	Output	OD[5]	PU[6]
1	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X1		Main clock I/O oscillation pin				
2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
	X0		Main clock input oscillation pin				
3	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	V_{CC}	—	Power supply pin	—	—	—	—
5	P73	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S07		TS touch ch. 7 input pin				
6	P72	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S06		TS touch ch. 6 input pin				
7	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S05		TS touch ch. 5 input pin				
8	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S04		TS touch ch. 4 input pin				
9	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S03		TS touch ch. 3 input pin				
10	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S02		TS touch ch. 2 input pin				
11	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S01		TS touch ch. 1 input pin				
12	P64	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	S00		TS touch ch. 0 input pin				
13	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
	AREF		TS reference impedance input pin				
14	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
	RST		Reset pin				
15	P60	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	EC1		8/16-bit composite timer ch. 1 clock input pin				
	DIO00		TS direct output ch. 0 pin				
16	P15	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT00		External interrupt input pin				
	UCK0		UART/SIO ch. 0 clock I/O pin				
17	P14	G	General-purpose I/O port	Hysteresis	CMOS	—	O
	INT01		External interrupt input pin				
	UO0		UART/SIO ch. 0 data output pin				

Pin no.	Pin name	I/O circuit type[4]	Function	I/O type			
				Input	Output	OD[5]	PU[6]
28	P45	K	General-purpose I/O port High-current pin	Hysteresis/ analog	CMOS	—	O
	AN07		8/10-bit A/D converter analog input pin				
	TO01		8/16-bit composite timer ch. 0 output pin				
	DIO04		TS direct output ch. 4 pin				
	PPG11		8/16-bit PPG ch. 1 output pin				
29	P10	H	General-purpose I/O port	Hysteresis	CMOS	O	—
	DBG		DBG input pin				
	EC0		8/16-bit composite timer ch. 0 clock input pin				
30	PG2	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X1A		Subclock I/O oscillation pin				
	DIO03		TS direct output ch. 3 pin				
31	PG1	C	General-purpose I/O port	Hysteresis	CMOS	—	O
	X0A		Subclock input oscillation pin				
	DIO04		TS direct output ch. 4 pin				
32	C	—	Decoupling capacitor connection pin	—	—	—	—

O: Available

Notes
4. For the I/O circuit types, see I/O Circuit Type.
5. N-ch open drain
6. Pull-up

6. I/O Circuit Type

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx. 5 MΩ CMOS output • Hysteresis input • Pull-up control

13. I/O Maps

13.1 MB95850K Series

Address	Register abbreviation	Register name	R/W	Initial value
0x0000	PDR0	Port 0 data register	R/W	0b00000000
0x0001	DDR0	Port 0 direction register	R/W	0b00000000
0x0002	PDR1	Port 1 data register	R/W	0b00000000
0x0003	DDR1	Port 1 direction register	R/W	0b00000000
0x0004	—	(Disabled)	—	—
0x0005	WATR	Oscillation stabilization wait time setting register	R/W	0b11111111
0x0006	PLLC	PLL control register	R/W	0b000X0000
0x0007	SYCC	System clock control register	R/W	0bXXX11011
0x0008	STBC	Standby control register	R/W	0b00000000
0x0009	RSRR	Reset source register	R/W	0b000XXXXX
0x000A	TBTC	Time-base timer control register	R/W	0b00000000
0x000B	WPCR	Watch prescaler control register	R/W	0b00000000
0x000C	WDTC	Watchdog timer control register	R/W	0b00XX0000
0x000D	SYCC2	System clock control register 2	R/W	0bXXXX0011
0x000E to 0x0011	—	(Disabled)	—	—
0x0012	PDR4	Port 4 data register	R/W	0b00000000
0x0013	DDR4	Port 4 direction register	R/W	0b00000000
0x0014, 0x0015	—	(Disabled)	—	—
0x0016	PDR6	Port 6 data register	R/W	0b00000000
0x0017	DDR6	Port 6 direction register	R/W	0b00000000
0x0018	PDR7	Port 7 data register	R/W	0b00000000
0x0019	DDR7	Port 7 direction register	R/W	0b00000000
0x001A, 0x001B	—	(Disabled)	—	—
0x001C	STBC2	Standby control register 2	R/W	0b00000000
0x001D to 0x0027	—	(Disabled)	—	—
0x0028	PDRF	Port F data register	R/W	0b00000000
0x0029	DDRF	Port F direction register	R/W	0b00000000
0x002A	PDRG	Port G data register	R/W	0b00000000
0x002B	DDRG	Port G direction register	R/W	0b00000000
0x002C	PUL0	Port 0 pull-up register	R/W	0b00000000
0x002D	PUL1	Port 1 pull-up register	R/W	0b00000000
0x002E to 0x0031	—	(Disabled)	—	—
0x0032	PUL7	Port 7 pull-up register	R/W	0b00000000
0x0033	PUL6	Port 6 pull-up register	R/W	0b00000000
0x0034	—	(Disabled)	—	—
0x0035	PULG	Port G pull-up register	R/W	0b00000000
0x0036	T01CR1	8/16-bit composite timer 01 status control register 1	R/W	0b00000000
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038, 0x0039	—	(Disabled)	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0E10	BPFREQ	Beep output frequency register	R/W	0b00000000
0x0E11	TER0	TS touch channel enable register 0	R/W	0b00000000
0x0E12	TER1	TS touch channel enable register 1	R/W	0b00000000
0x0E13	PSC	TS prescaler control register	R/W	0b00100000
0x0E14	WRESET	TS warm reset register	R/W	0b00000000
0x0E15	RSEL0	TS sensitivity select register 0	R/W	0b00000010
0x0E16	RSEL1	TS sensitivity select register 1	R/W	0b00010010
0x0E17	RSEL2	TS sensitivity select register 2	R/W	0b00010010
0x0E18	RSEL3	TS sensitivity select register 3	R/W	0b00010010
0x0E19 to 0x0E1B	—	(Disabled)	—	—
0x0E1C	BPDUR	TS beep duration setting register	R/W	0b00000000
0x0E1D	DIOR1	TS direct output control register 1	R/W	0b00000000
0x0E1E	DIOR2	TS direct output control register 2	R/W	0b00000000
0x0E1F	DIOR3	TS direct output control register 3	R/W	0b00000000
0x0E20	FTSEL	TS feature select register	R/W	0b00000100
0x0E21	AICWAT	TS AIC wait time setting register	R/W	0b00100111
0x0E22	CALITV	TS calibration interval setting register	R/W	0b00110000
0x0E23	ITGTM	TS integration time setting register	R/W	0b00001111
0x0E24	IDLETM	TS idle time setting register	R/W	0b00001111
0x0E25	CONTROL	TS control register	R/W	0b00000000
0x0E26	INTMR	TS interrupt mask register	R/W	0b00011000
0x0E27	INTCR	TS interrupt clear register	R/W	0b00000000
0x0E28	FLTP	TS filter period setting register	R/W	0b00000000
0x0E29	FLTTH	TS filter threshold setting register	R/W	0b00000000
0x0E2A	REFDLY	TS reference delay setting register	R/W	0b00000000
0x0E2B to 0x0E30	—	(Disabled)	—	—
0x0E31	ALPH1	TS alpha value setting register ch. 1	R/W	0b00001000
0x0E32	ALPH2	TS alpha value setting register ch. 2	R/W	0b00001000
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36 to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E50	—	(Disabled)	—	—
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001

Address	Register abbreviation	Register name	R/W	Initial value
0x0F9C	PPS01	8/16-bit PPG01 cycle setting buffer register	R/W	0b11111111
0x0F9D	PPS00	8/16-bit PPG00 cycle setting buffer register	R/W	0b11111111
0x0F9E	PDS01	8/16-bit PPG01 duty setting buffer register	R/W	0b11111111
0x0F9F	PDS00	8/16-bit PPG00 duty setting buffer register	R/W	0b11111111
0x0FA0 to 0x0FA3	—	(Disabled)	—	—
0x0FA4	PPGS	8/16-bit PPG start register	R/W	0b00000000
0x0FA5	REVC	8/16-bit PPG output inversion register	R/W	0b00000000
0x0FA6 to 0x0FBD	—	(Disabled)	—	—
0x0FBE	PSSR0	UART/SIO dedicated baud rate generator prescaler select register ch. 0	R/W	0b00000000
0x0FBF	BRSR0	UART/SIO dedicated baud rate generator baud rate setting register ch. 0	R/W	0b00000000
0x0FC0	TIDR0	Touch input disable register 0	R/W	0b00000000
0x0FC1	TIDR1	Touch input disable register 1	R/W	0b00000000
0x0FC2	—	(Disabled)	—	—
0x0FC3	AIDRL	A/D input disable register (lower)	R/W	0b00000000
0x0FC4	LVDPW	LVD reset circuit password register	R/W	0b00000000
0x0FC5 to 0x0FE2	—	(Disabled)	—	—
0x0FE3	WCDR	Watch counter data register	R/W	0b00111111
0x0FE4	CRTH	Main CR clock trimming register (upper)	R/W	0b000XXXXX
0x0FE5	CRTL	Main CR clock trimming register (lower)	R/W	0b000XXXXX
0x0FE6	—	(Disabled)	—	—
0x0FE7	CRTDA	Main CR clock temperature dependent adjustment register	R/W	0b000XXXXX
0x0FE8	SYSC	System configuration register	R/W	0b11000011
0x0FE9	CMCR	Clock monitoring control register	R/W	0b00000000
0x0FEA	CMDR	Clock monitoring data register	R	0b00000000
0x0FEB	WDTH	Watchdog timer selection ID register (upper)	R	0bXXXXXXXX
0x0FEC	WDTL	Watchdog timer selection ID register (lower)	R	0bXXXXXXXX
0x0FED, 0x0FEE	—	(Disabled)	—	—
0x0FEF	WICR	Interrupt pin selection circuit control register	R/W	0b01000000
0x0FF0 to 0x0FFF	—	(Disabled)	—	—

■ R/W access symbols
R/W : Readable/Writable
R : Read only

■ Initial value symbols
0 : The initial value of this bit is “0”.
1 : The initial value of this bit is “1”.
X : The initial value of this bit is undefined.

Note: Do not write to an address that is “(Disabled)”. If a “(Disabled)” address is read, an indeterminate value is returned.

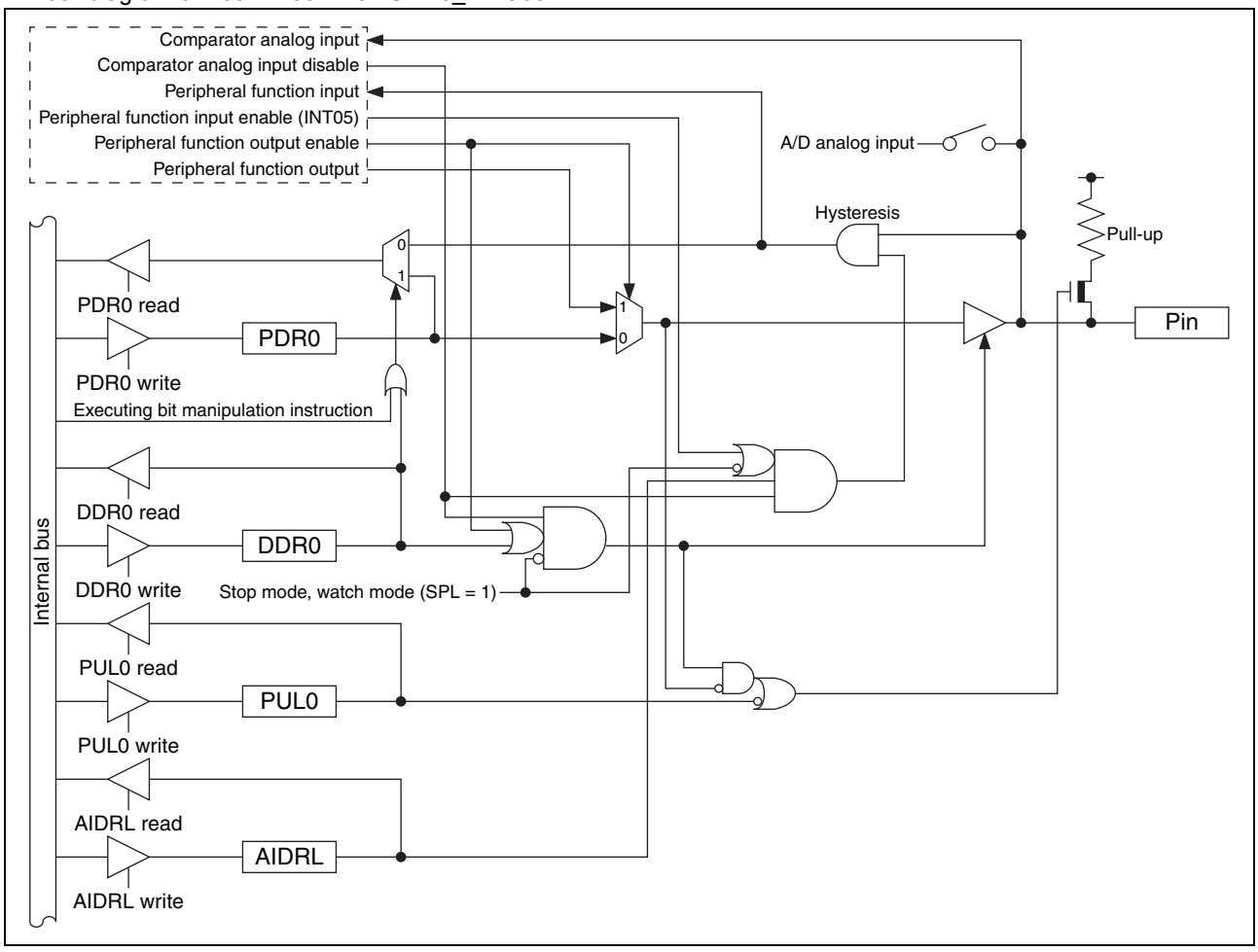
Address	Register abbreviation	Register name	R/W	Initial value
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	PC21	8/16-bit PPG timer 21 control register	R/W	0b00000000
0x003F	PC20	8/16-bit PPG timer 20 control register	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C	EIC01	External interrupt circuit control register ch. 8/ch. 9	R/W	0b00000000
0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x005C to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066 to 0x006B	—	(Disabled)	—	—
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000

■ P05/INT05/AN01/CMP0_N/TO00 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT05)
- ❒ 8/10-bit A/D converter analog input pin (AN01)
- ❒ Comparator ch. 0 inverting analog input (negative input) pin (CMP0_N)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO00)

■ Block diagram of P05/INT05/AN01/CMP0_N/TO00



■ P07/AN03/CMP0_P/PPG01 pin

This pin has the following peripheral functions:

- ❒ 8/10-bit A/D converter analog input pin (AN03)
- ❒ Comparator ch. 0 non-inverting analog input (positive input) pin (CMP0_P)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG01)

3. Port 0 registers

■ Port 0 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR0	0	Pin state is “L” level.	PDR0 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR0 value is “1”.	As output port, outputs “H” level.
DDR0	0	Port input enabled		
	1	Port output enabled		
PUL0	0	Pull-up disabled		
	1	Pull-up enabled		
AIDRL	0	Analog input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 0

Pin name	Correspondence between related register bits and pins							
	P07	P06	P05	P04	-	-	-	-
PDR0	bit7	bit6	bit5	bit4	-	-	-	-
DDR0								
PUL0								
AIDRL	bit5	bit4	bit1	bit0				

14.1.2 Port 1

Port 1 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 1 configuration

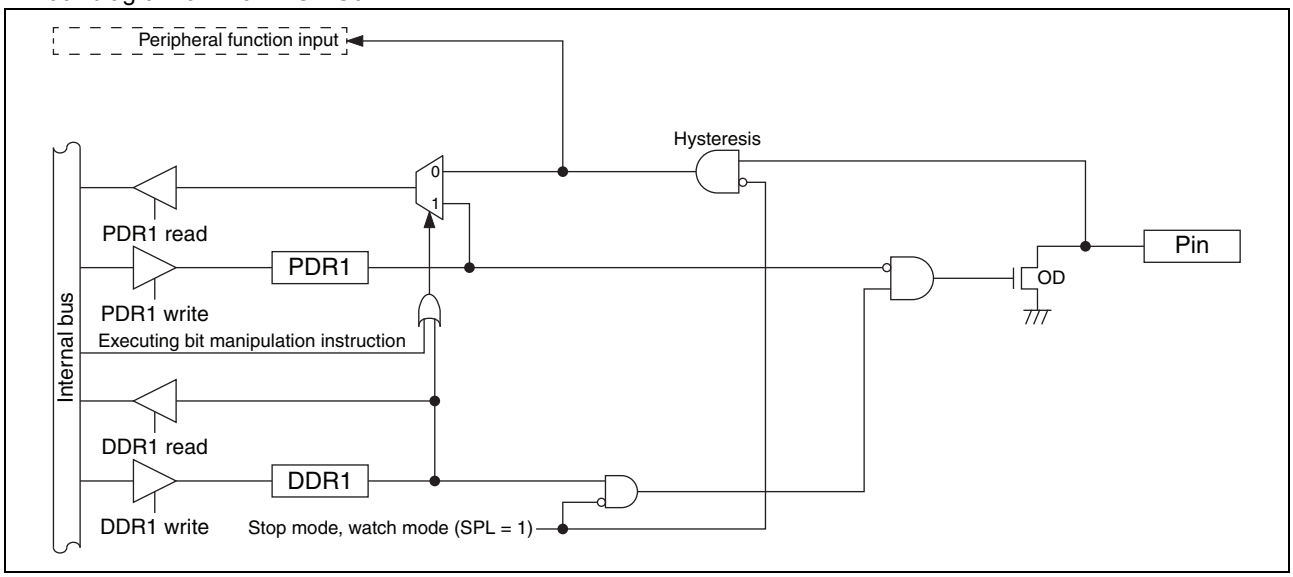
■ Port 1 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 1 data register (PDR1)
- ❒ Port 1 direction register (DDR1)
- ❒ Port 1 pull-up register (PUL1)

2. Block diagrams of port 1

■ P10/DBG/EC0 pin

This pin has the following peripheral functions:
- ❒ DBG input pin (DBG)
- ❒ 8/16-bit composite timer ch. 0 clock input pin (EC0)

■ Block diagram of P10/DBG/EC0



■ P13/INT04/UI0/DIO02 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT04)
- ❒ UART/SIO ch. 0 data input pin (UI0)
- ❒ TS direct output ch. 2 pin (DIO02)

14.1.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

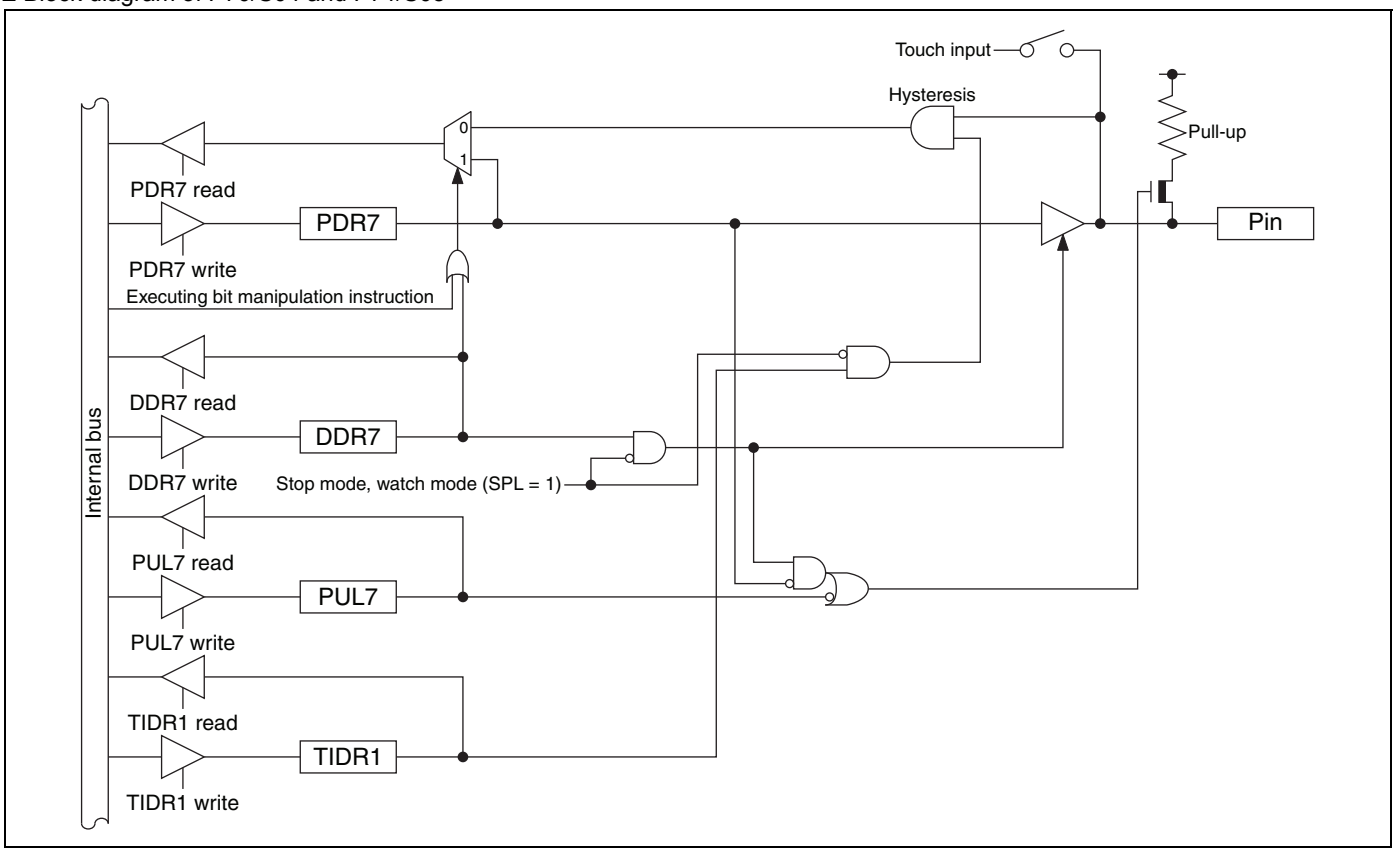
■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

■ Block diagram of P70/S04 and P71/S05



14.2.1 Port 0

Port 0 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 0 configuration

■ Port 0 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 0 data register (PDR0)
- ❒ Port 0 direction register (DDR0)
- ❒ Port 0 pull-up register (PUL0)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 0

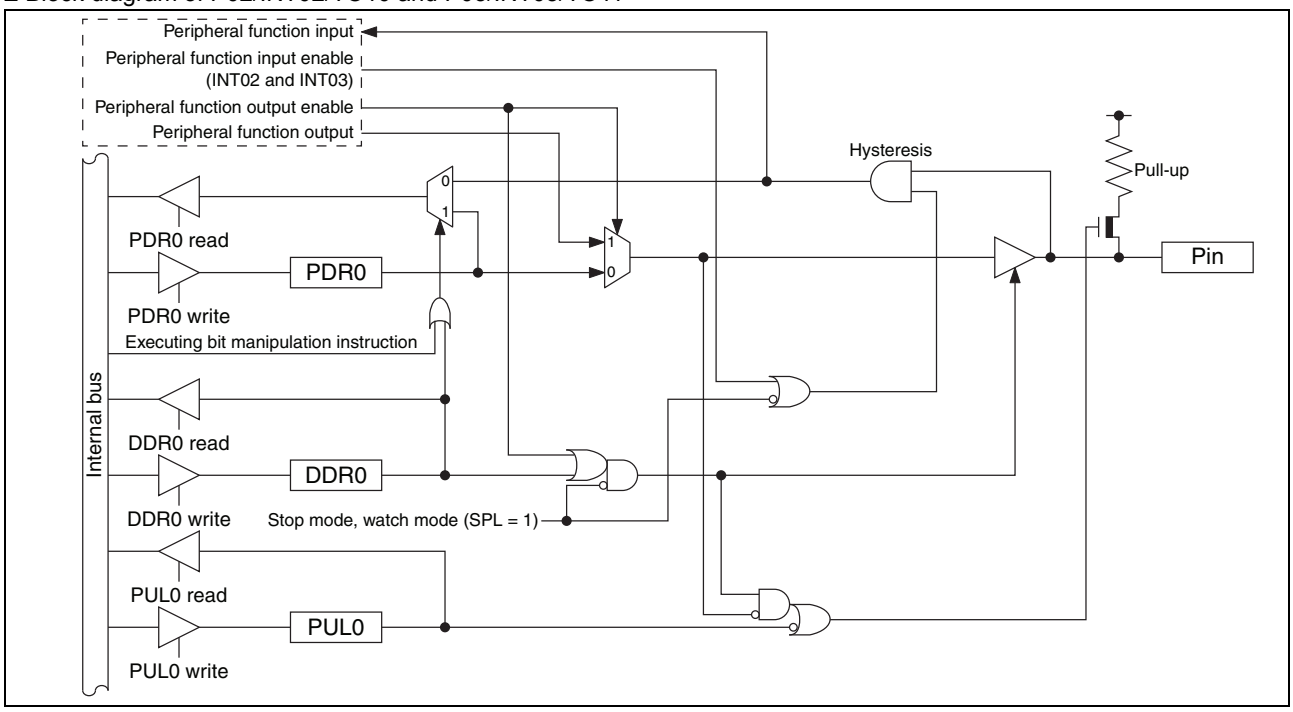
■ P02/INT02/TO10 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT02)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO10)

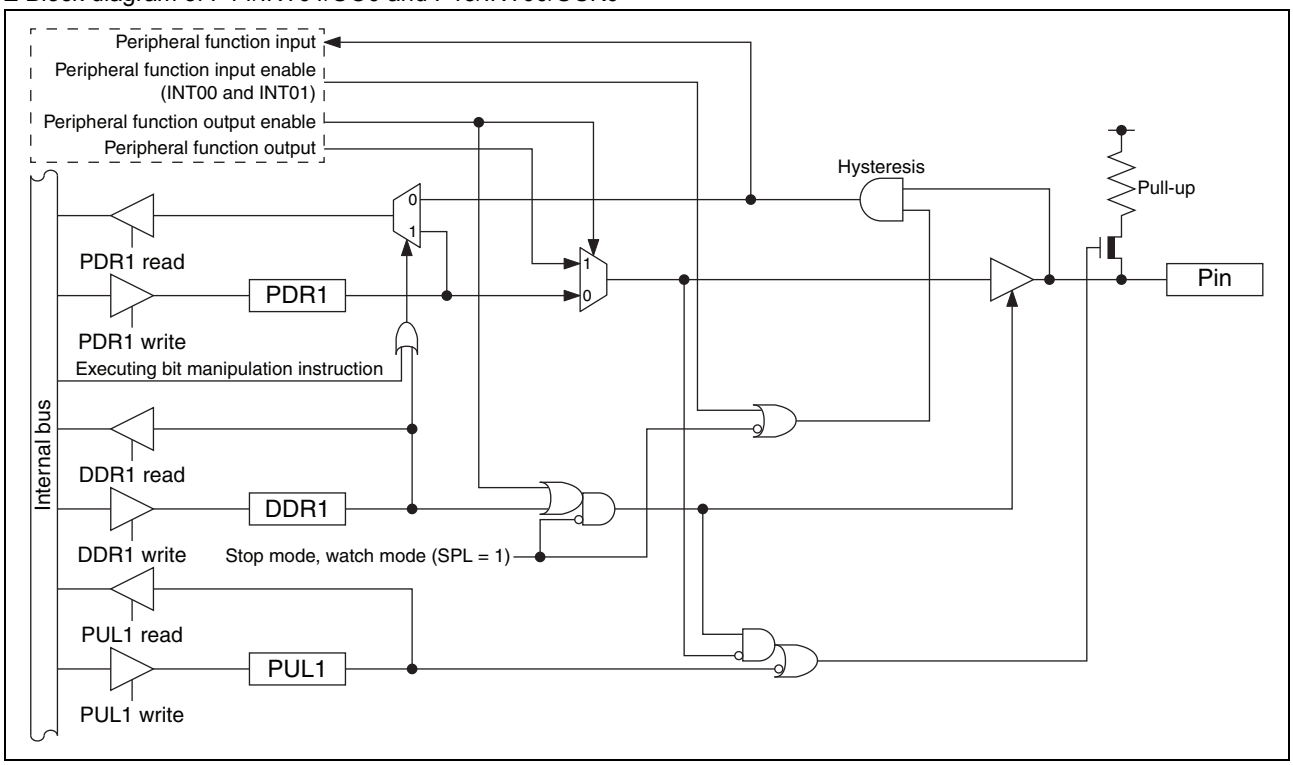
■ P03/INT03/TO11 pin

This pin has the following peripheral functions:
- ❒ External interrupt input pin (INT03)
- ❒ 8/16-bit composite timer ch. 1 output pin (TO11)

■ Block diagram of P02/INT02/TO10 and P03/INT03/TO11



■ Block diagram of P14/INT01/UO0 and P15/INT00/UCK0



3. Port 1 registers

■ Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 1

Pin name	Correspondence between related register bits and pins							
	-	-	P15	P14	P13	-	-	P10
PDR1	-	-	bit5	bit4	bit3	-	-	bit0*
DDR1								
PUL1								

*: Though P10 has no pull-up function, bit0 in the PUL1 register can still be accessed. The operation of P10 is not affected by the setting of bit0 in the PUL1 register.

14.2.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

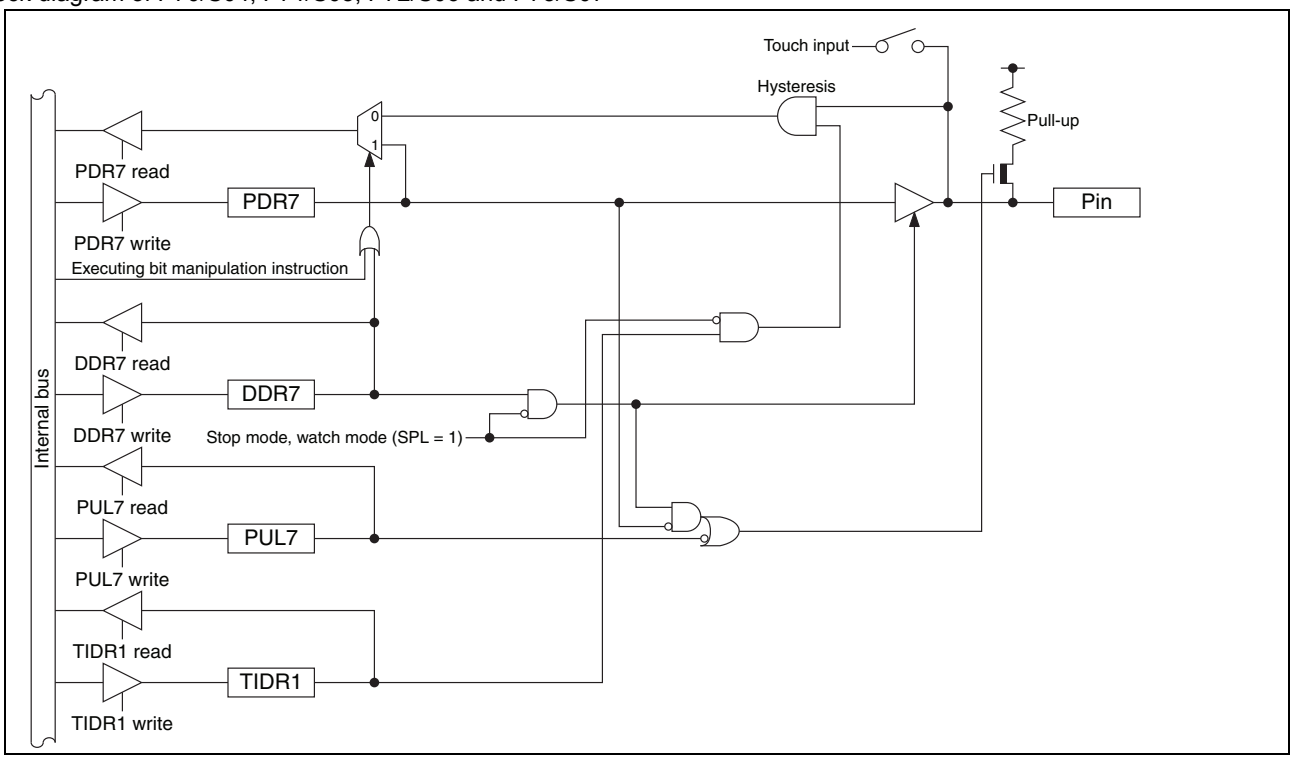
■ P72/S06 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 6 input pin (S06)

■ P73/S07 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 7 input pin (S07)

■ Block diagram of P70/S04, P71/S05, P72/S06 and P73/S07



14.3.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

- Port 7 is made up of the following elements.
  - General-purpose I/O pins/peripheral function I/O pins
  - Port 7 data register (PDR7)
  - Port 7 direction register (DDR7)
  - Port 7 pull-up register (PUL7)
  - Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

- P70/S04 pin

This pin has the following peripheral function:
  - TS touch ch. 4 input pin (S04)

- P71/S05 pin

This pin has the following peripheral function:
  - TS touch ch. 5 input pin (S05)

- P72/S06 pin

This pin has the following peripheral function:
  - TS touch ch. 6 input pin (S06)

- P73/S07 pin

This pin has the following peripheral function:
  - TS touch ch. 7 input pin (S07)

- P74/S08 pin

This pin has the following peripheral function:
  - TS touch ch. 8 input pin (S08)

- P75/S09 pin

This pin has the following peripheral function:
  - TS touch ch. 9 input pin (S09)

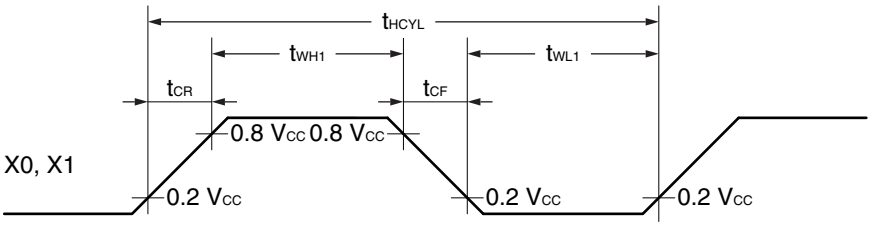
- P76/S10 pin

This pin has the following peripheral function:
  - TS touch ch. 10 input pin (S10)

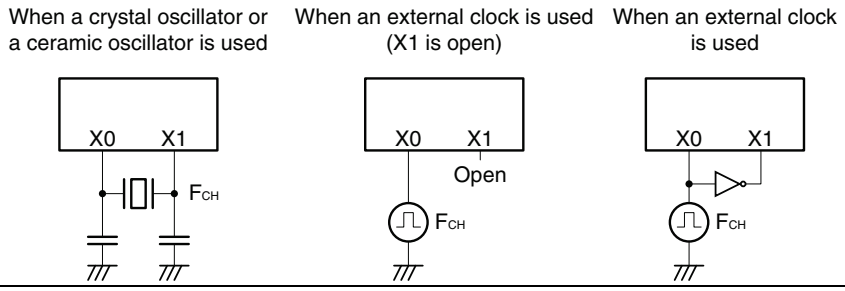
- P77/S11 pin

This pin has the following peripheral function:
  - TS touch ch. 11 input pin (S11)

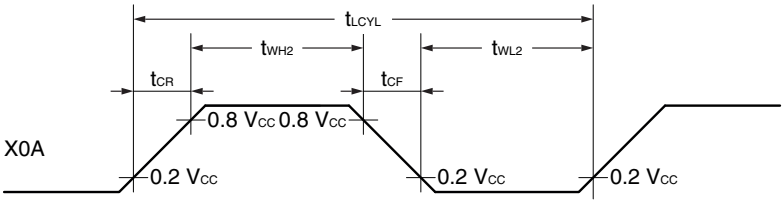
■ Input waveform generated when an external clock (main clock) is used



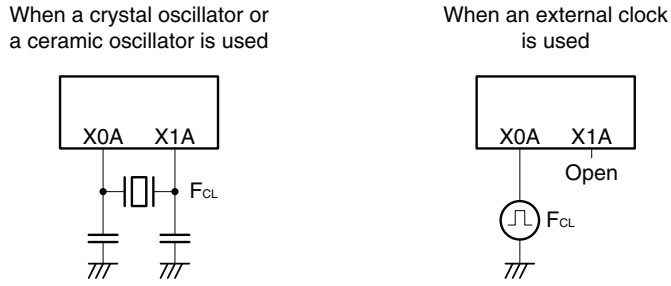
■ Figure of main clock input port external connection



■ Input waveform generated when an external clock (subclock) is used



■ Figure of subclock input port external connection



17.4.6 Low-voltage Detection

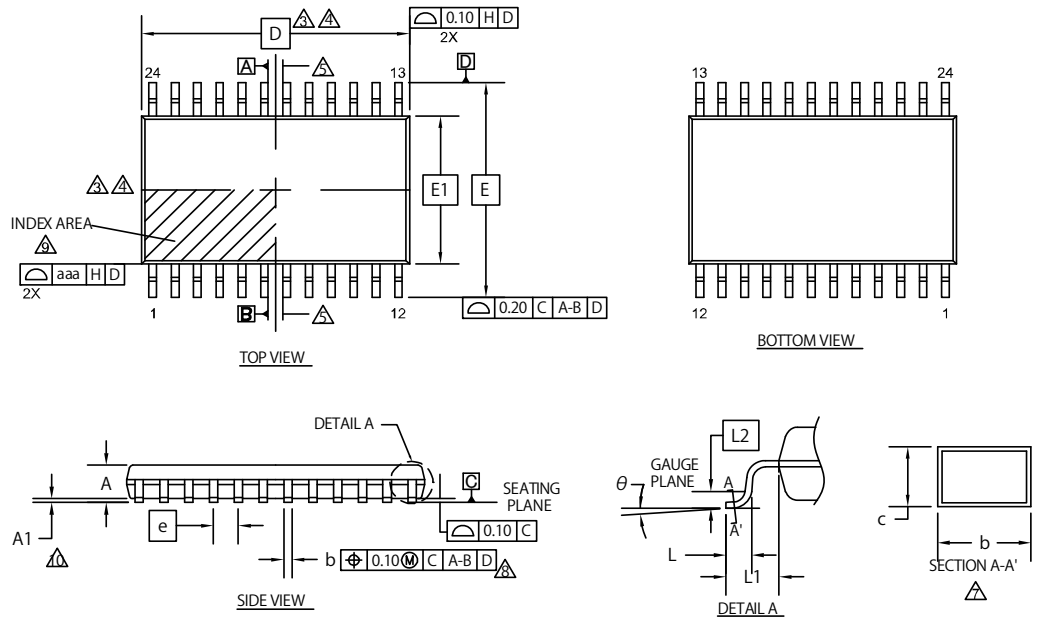
(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Release voltage*	V_{DL+}	2.52	2.7	2.88	V	At power supply rise
		2.61	2.8	2.99	V	
		2.89	3.1	3.31	V	
		3.08	3.3	3.52	V	
Detection voltage*	V_{DL-}	2.43	2.6	2.77	V	At power supply fall
		2.52	2.7	2.88	V	
		2.80	3	3.20	V	
		2.99	3.2	3.41	V	
Hysteresis width	V_{HYS}	—	—	100	mV	
Power supply start voltage	V_{off}	—	—	2.3	V	
Power supply end voltage	V_{on}	4.9	—	—	V	
Power supply voltage change time (at power supply rise)	t_r	650	—	—	µs	Slope of power supply that the reset release signal generates within the rating (V_{DL+})
Power supply voltage change time (at power supply fall)	t_f	650	—	—	µs	Slope of power supply that the reset detection signal generates within the rating (V_{DL-})
Reset release delay time	t_{d1}	—	—	30	µs	
Reset detection delay time	t_{d2}	—	—	30	µs	
LVD reset threshold voltage transition stabilization time	t_{stb}	10	—	—	µs	

*: After the LVD reset is enabled by the LVD reset circuit control register (LVDCC), the release voltage and the detection voltage can be selected by using the LVD reset voltage selection ID register (LVDR) in the low-voltage detection reset circuit. For details of the LVDCC register and the LVDR register, refer to “CHAPTER 16 LOW-VOLTAGE DETECTION RESET CIRCUIT” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

19. Package Dimension

Package Type	Package Code
TSSOP 24	STI024



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	7.80 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.20	0.22	0.29
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

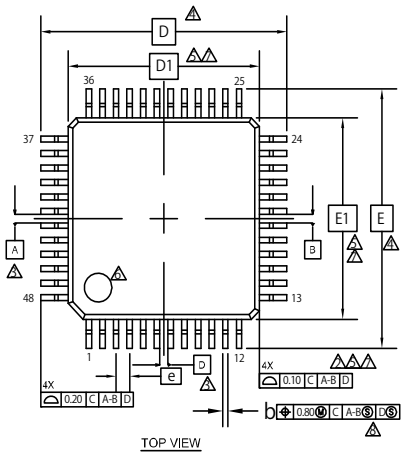
NOTES

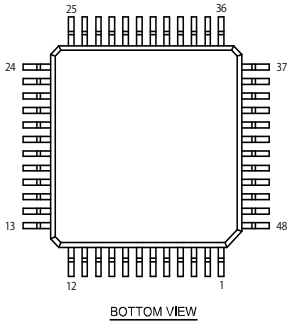
1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.

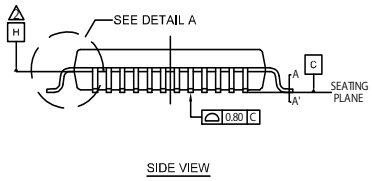
002-14046 **

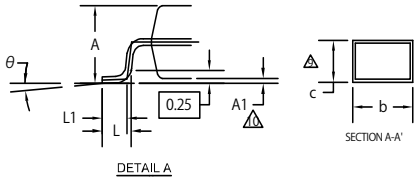
PACKAGE OUTLINE, 24 LEAD TSSOP
4.4X7.8X1.2 MM STI024 REV**

Package Type	Package Code
LQFP 48	LQA048









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Document History Page

Document Title: MB95F856K, MB95F866K, MB95F876K New 8FX MB95850K/860K/870K Series Datasheet Document Number: 002-09305				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	YSKA	08/02/2012	Migrated to Cypress and assigned document number 002-09305. No change to document contents or format.
*A	5560459	YSKA	12/20/2016	Migrated to Cypress datasheet template
*B	5844036	YSAT	08/04/2017	Adapted new Cypress logo
*C	6038234	YSAT	01/22/2018	Corrected the package codes as bellow FPT-24P-M10 → STI024 FPT-24P-M34 → SOL024 FPT-32P-M30 → LQB032 FPT-48P-M49 → LQA048 FPT-52P-M02 → LQC052 Updated “19. Package Dimension” Updated Arm trademark and the last page