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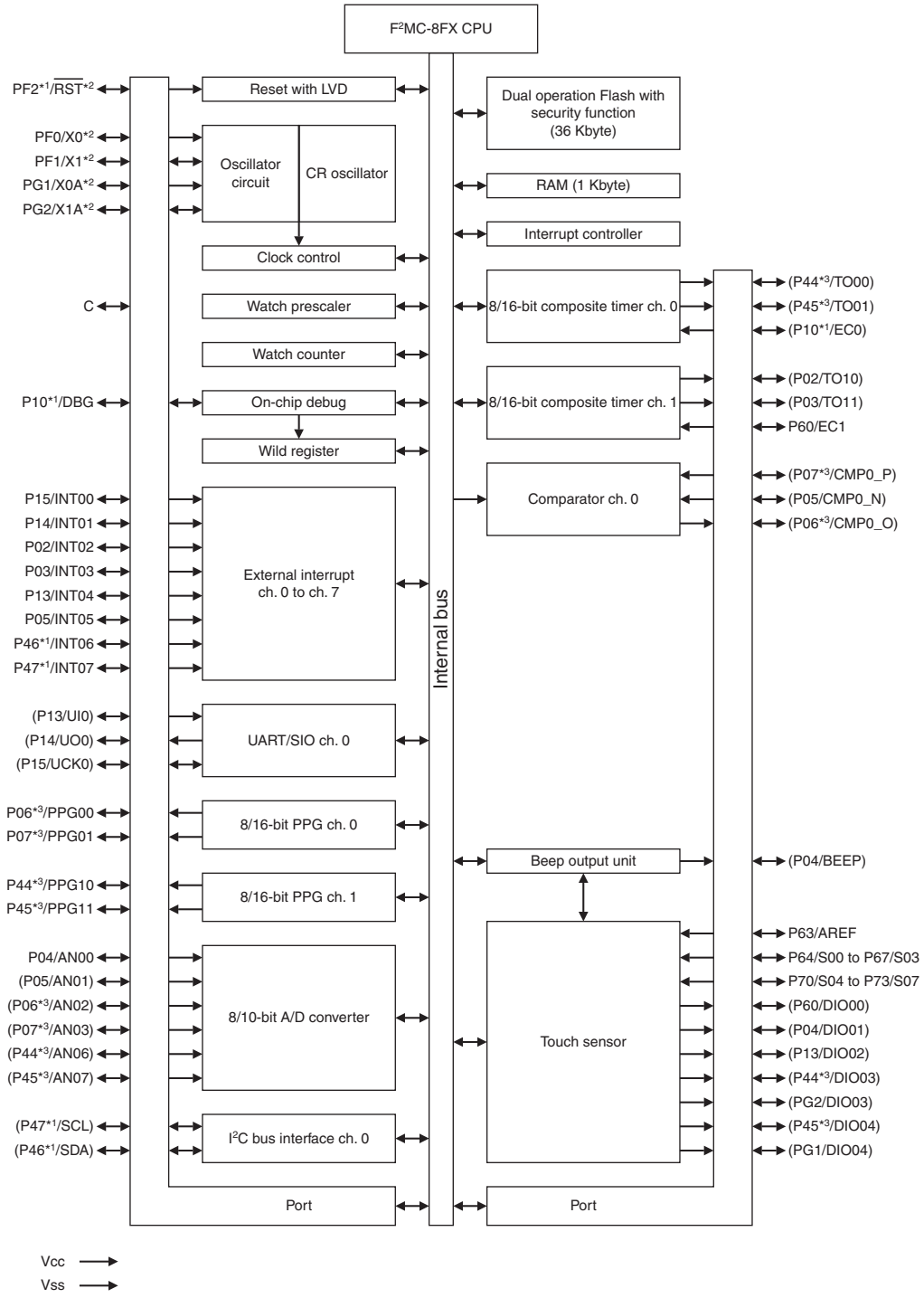
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f876kpmc-g-sne2

Block Diagram (MB95860K Series)



*1: P10, P46, P47 and PF2 are N-ch open drain pins.

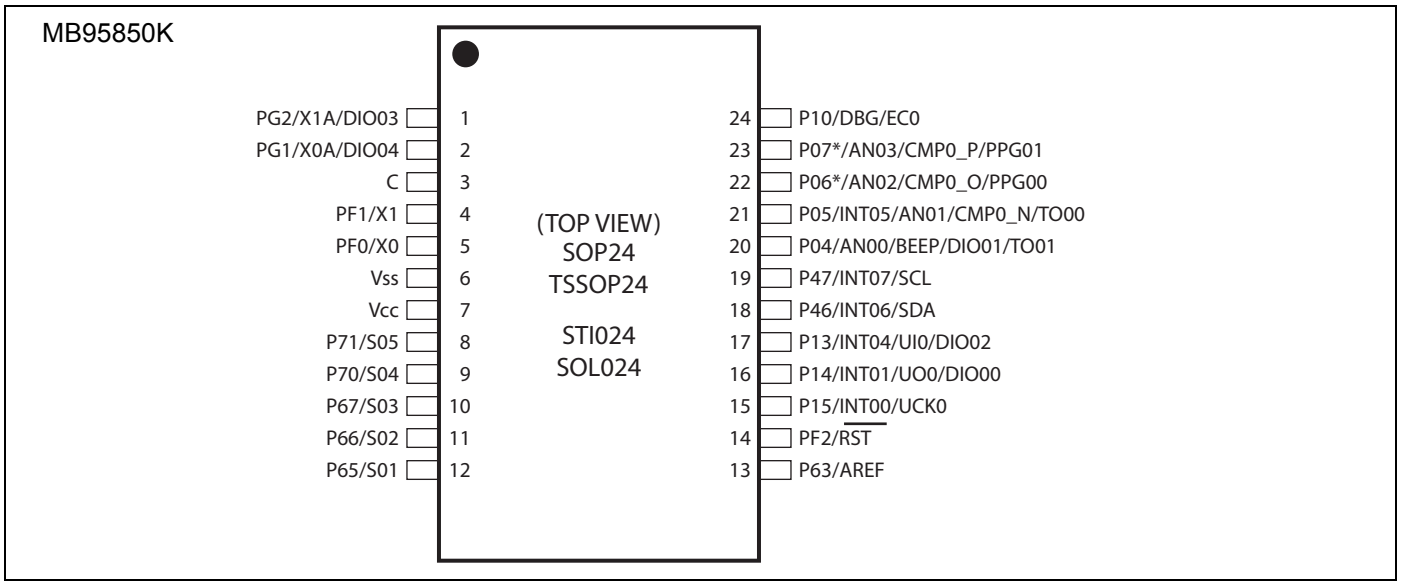
*2: Software select

*3: P06, P07, P44 and P45 are high-current pins.

Note: Pins in parentheses indicate that those pins are shared among different peripheral functions.

Contents

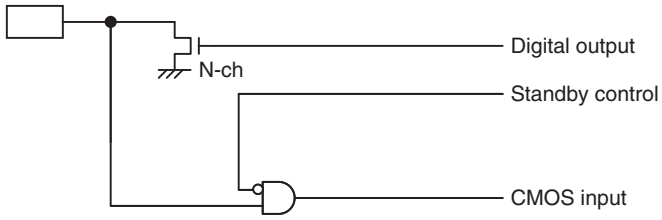
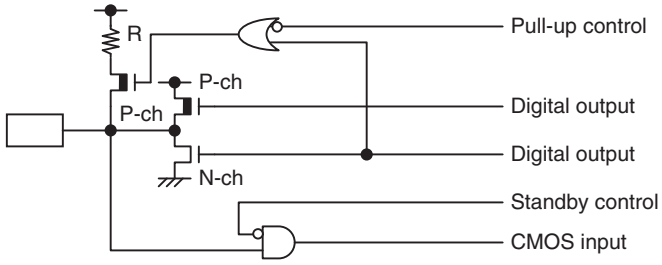
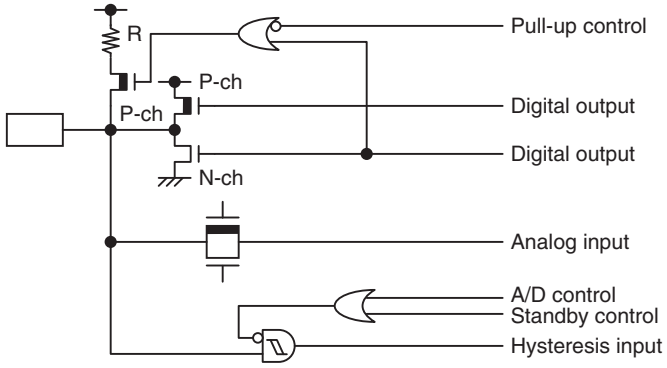
4. Pin Assignment



*: High-current pin (8 mA/12 mA)

5.3 MB95870K Series

Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
1	1	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
2	2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
3	3	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	4	V_{CC}	—	Power supply pin	—	—	—	—
5	5	P77	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S11		TS touch ch. 11 input pin				
6	6	P76	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S10		TS touch ch. 10 input pin				
—	7	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
7	8	P75	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S09		TS touch ch. 9 input pin				
8	9	P74	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S08		TS touch ch. 8 input pin				
9	10	P73	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S07		TS touch ch. 7 input pin				
10	11	P72	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S06		TS touch ch. 6 input pin				
11	12	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S05		TS touch ch. 5 input pin				
12	13	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S04		TS touch ch. 4 input pin				
13	14	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S03		TS touch ch. 3 input pin				
14	15	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S02		TS touch ch. 2 input pin				
15	16	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S01		TS touch ch. 1 input pin				
16	17	P64	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S00		TS touch ch. 0 input pin				
17	18	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AREF		TS reference impedance input pin				
18	19	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		RST		Reset pin				
—	20	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—

Type	Circuit	Remarks
I		• N-ch open drain output • CMOS input
J		• CMOS output • CMOS input • Pull-up control
K		• CMOS output • Hysteresis input • Pull-up control • Analog input • High-current output

Address	Register abbreviation	Register name	R/W	Initial value
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36	ALPH6	TS alpha value setting register ch. 6	R/W	0b00001000
0x0E37	ALPH7	TS alpha value setting register ch. 7	R/W	0b00001000
0x0E38 to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E4F	—	(Disabled)	—	—
0x0E50	STRTH0	TS touch strength threshold setting register ch. 0	R/W	0b00000001
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001
0x0E54	STRTH4	TS touch strength threshold setting register ch. 4	R/W	0b00000001
0x0E55	STRTH5	TS touch strength threshold setting register ch. 5	R/W	0b00000001
0x0E56	STRTH6	TS touch strength threshold setting register ch. 6	R/W	0b00000001
0x0E57	STRTH7	TS touch strength threshold setting register ch. 7	R/W	0b00000001
0x0E58 to 0x0E5F	—	(Disabled)	—	—
0x0E60	STR0	TS touch strength register ch. 0	R	0bXXXXXXXX
0x0E61	STR1	TS touch strength register ch. 1	R	0bXXXXXXXX
0x0E62	STR2	TS touch strength register ch. 2	R	0bXXXXXXXX
0x0E63	STR3	TS touch strength register ch. 3	R	0bXXXXXXXX
0x0E64	STR4	TS touch strength register ch. 4	R	0bXXXXXXXX
0x0E65	STR5	TS touch strength register ch. 5	R	0bXXXXXXXX
0x0E66	STR6	TS touch strength register ch. 6	R	0bXXXXXXXX
0x0E67	STR7	TS touch strength register ch. 7	R	0bXXXXXXXX
0x0E68 to 0x0E6F	—	(Disabled)	—	—
0x0E70	CALIP0	TS calibrated impedance register ch. 0	R	0b0XXXXXXX
0x0E71	CALIP1	TS calibrated impedance register ch. 1	R	0b0XXXXXXX
0x0E72	CALIP2	TS calibrated impedance register ch. 2	R	0b0XXXXXXX
0x0E73	CALIP3	TS calibrated impedance register ch. 3	R	0b0XXXXXXX
0x0E74	CALIP4	TS calibrated impedance register ch. 4	R	0b0XXXXXXX
0x0E75	CALIP5	TS calibrated impedance register ch. 5	R	0b0XXXXXXX
0x0E76	CALIP6	TS calibrated impedance register ch. 6	R	0b0XXXXXXX
0x0E77	CALIP7	TS calibrated impedance register ch. 7	R	0b0XXXXXXX
0x0E78 to 0x0E7F	—	(Disabled)	—	—
0x0E80	IMPE0	TS impedance register ch. 0	R	0b0XXXXXXX
0x0E81	IMPE1	TS impedance register ch. 1	R	0b0XXXXXXX
0x0E82	IMPE2	TS impedance register ch. 2	R	0b0XXXXXXX
0x0F80	WRARH0	Wild register address setting register (upper) ch. 0	R/W	0b00000000
0x0F81	WRARL0	Wild register address setting register (lower) ch. 0	R/W	0b00000000

Address	Register abbreviation	Register name	R/W	Initial value
0x0037	T00CR1	8/16-bit composite timer 00 status control register 1	R/W	0b00000000
0x0038	T11CR1	8/16-bit composite timer 11 status control register 1	R/W	0b00000000
0x0039	T10CR1	8/16-bit composite timer 10 status control register 1	R/W	0b00000000
0x003A	PC01	8/16-bit PPG timer 01 control register	R/W	0b00000000
0x003B	PC00	8/16-bit PPG timer 00 control register	R/W	0b00000000
0x003C	PC11	8/16-bit PPG timer 11 control register	R/W	0b00000000
0x003D	PC10	8/16-bit PPG timer 10 control register	R/W	0b00000000
0x003E	PC21	8/16-bit PPG timer 21 control register	R/W	0b00000000
0x003F	PC20	8/16-bit PPG timer 20 control register	R/W	0b00000000
0x0040 to 0x0047	—	(Disabled)	—	—
0x0048	EIC00	External interrupt circuit control register ch. 0/ch. 1	R/W	0b00000000
0x0049	EIC10	External interrupt circuit control register ch. 2/ch. 3	R/W	0b00000000
0x004A	EIC20	External interrupt circuit control register ch. 4/ch. 5	R/W	0b00000000
0x004B	EIC30	External interrupt circuit control register ch. 6/ch. 7	R/W	0b00000000
0x004C	EIC01	External interrupt circuit control register ch. 8/ch. 9	R/W	0b00000000
0x004D	—	(Disabled)	—	—
0x004E	LVDR	LVD reset voltage selection ID register	R/W	0b00000000
0x004F	LVDCC	LVD reset circuit control register	R/W	0b00000001
0x0050 to 0x0055	—	(Disabled)	—	—
0x0056	SMC10	UART/SIO serial mode control register 1 ch. 0	R/W	0b00000000
0x0057	SMC20	UART/SIO serial mode control register 2 ch. 0	R/W	0b00100000
0x0058	SSR0	UART/SIO serial status and data register ch. 0	R/W	0b00000001
0x0059	TDR0	UART/SIO serial output data register ch. 0	R/W	0b00000000
0x005A	RDR0	UART/SIO serial input data register ch. 0	R	0b00000000
0x005B	CMR0	Comparator control register ch. 0	R/W	0b11000101
0x005C to 0x005F	—	(Disabled)	—	—
0x0060	IBCR00	I^2C bus control register 0 ch. 0	R/W	0b00000000
0x0061	IBCR10	I^2C bus control register 1 ch. 0	R/W	0b00000000
0x0062	IBSR0	I^2C bus status register ch. 0	R/W	0b00000000
0x0063	IDDR0	I^2C data register ch. 0	R/W	0b00000000
0x0064	IAAR0	I^2C address register ch. 0	R/W	0b00000000
0x0065	ICCR0	I^2C clock control register ch. 0	R/W	0b00000000
0x0066 to 0x006B	—	(Disabled)	—	—
0x006C	ADC1	8/10-bit A/D converter control register 1	R/W	0b00000000
0x006D	ADC2	8/10-bit A/D converter control register 2	R/W	0b00000000
0x006E	ADDH	8/10-bit A/D converter data register (upper)	R/W	0b00000000
0x006F	ADDL	8/10-bit A/D converter data register (lower)	R/W	0b00000000
0x0070	WCSR	Watch counter control register	R/W	0b00000000
0x0071	FSR2	Flash memory status register 2	R/W	0b00000000
0x0072	FSR	Flash memory status register	R/W	0b000X0000

14.1.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

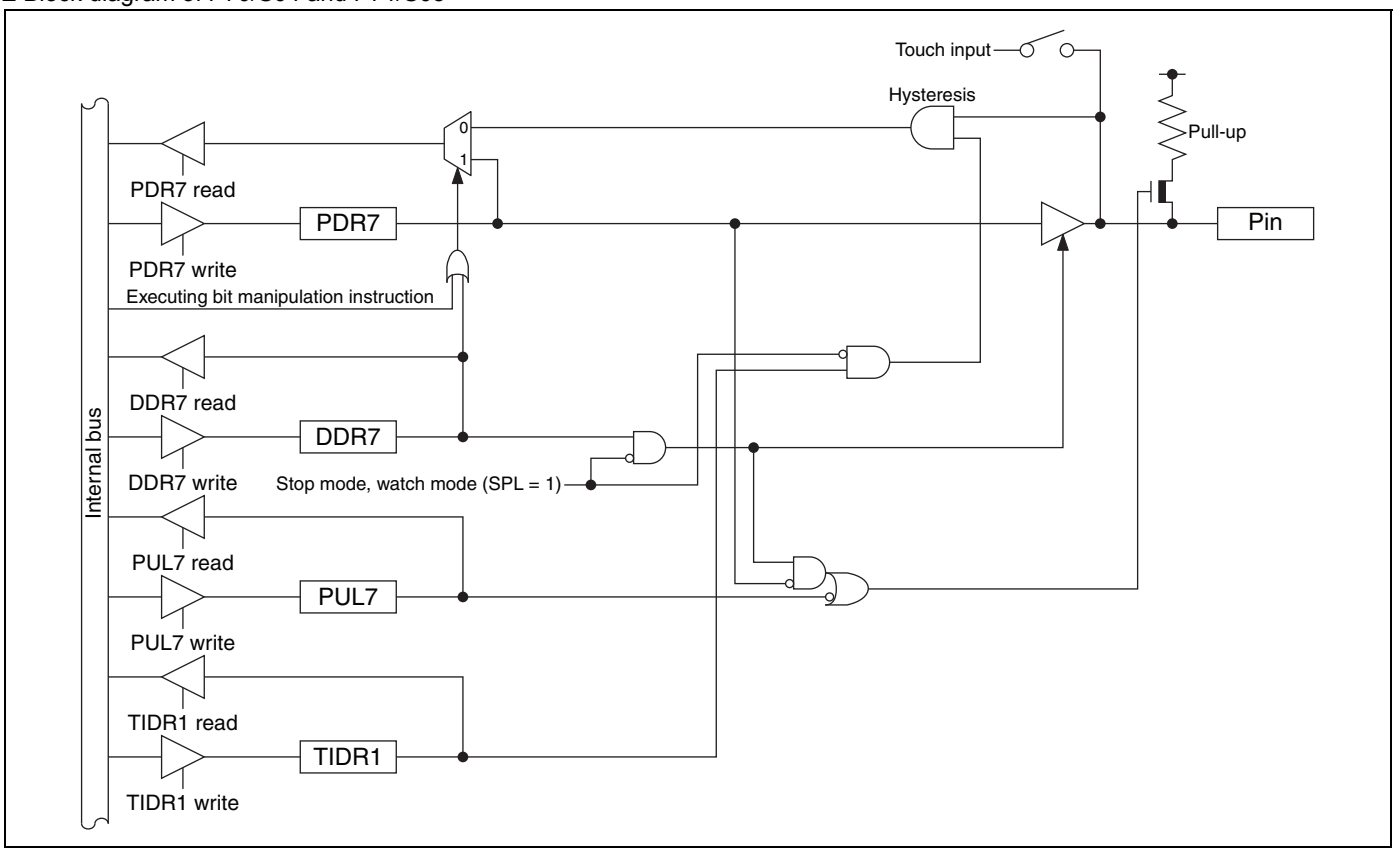
■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

■ Block diagram of P70/S04 and P71/S05



3. Port 7 registers

■ Port 7 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR7	0	Pin state is “L” level.	PDR7 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR7 value is “1”.	As output port, outputs “H” level.
DDR7	0	Port input enabled		
	1	Port output enabled		
PUL7	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR1	0	Touch input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 7

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	-	P71	P70
PDR7	-	-	-	-	-	-	bit1	bit0
DDR7								
PUL7								
TIDR1								

4. Port 7 operations

■ Operation as an output port

- ❒ A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR7 register returns the PDR7 register value.

■ Operation as an input port

- ❒ A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 1 (TIDR1) corresponding to that pin to “1”.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR1 register is initialized to “0”.

■ Operation in stop mode and watch mode

- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

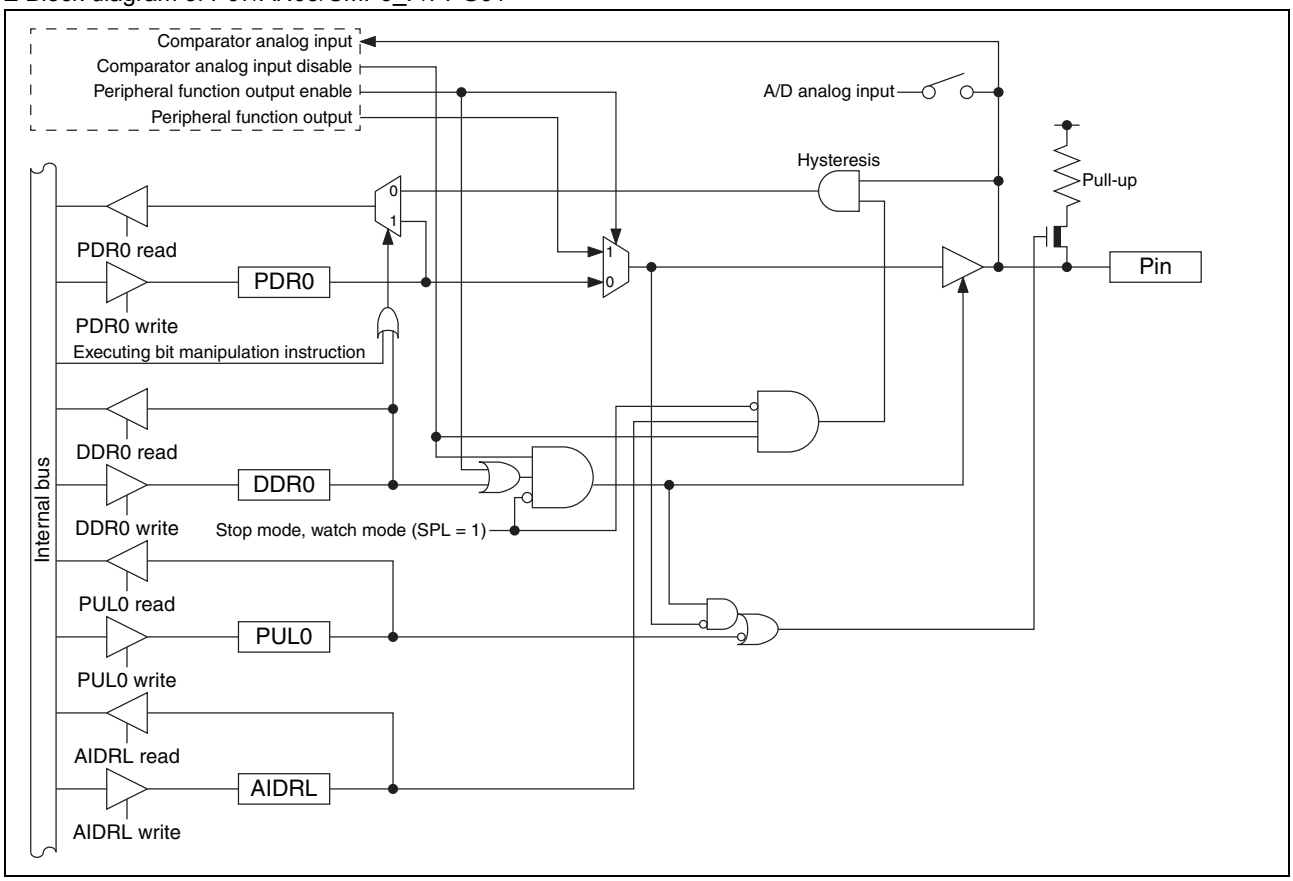
■ Operation as a touch input pin

Set the bit in the DDR7 register corresponding to the touch input pin to “0”, the bit in the TIDR1 register corresponding to the same pin to “0”, and the bit in the PUL7 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

■ Block diagram of P07/AN03/CMP0_P/PPG01



14.2.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 6 configuration

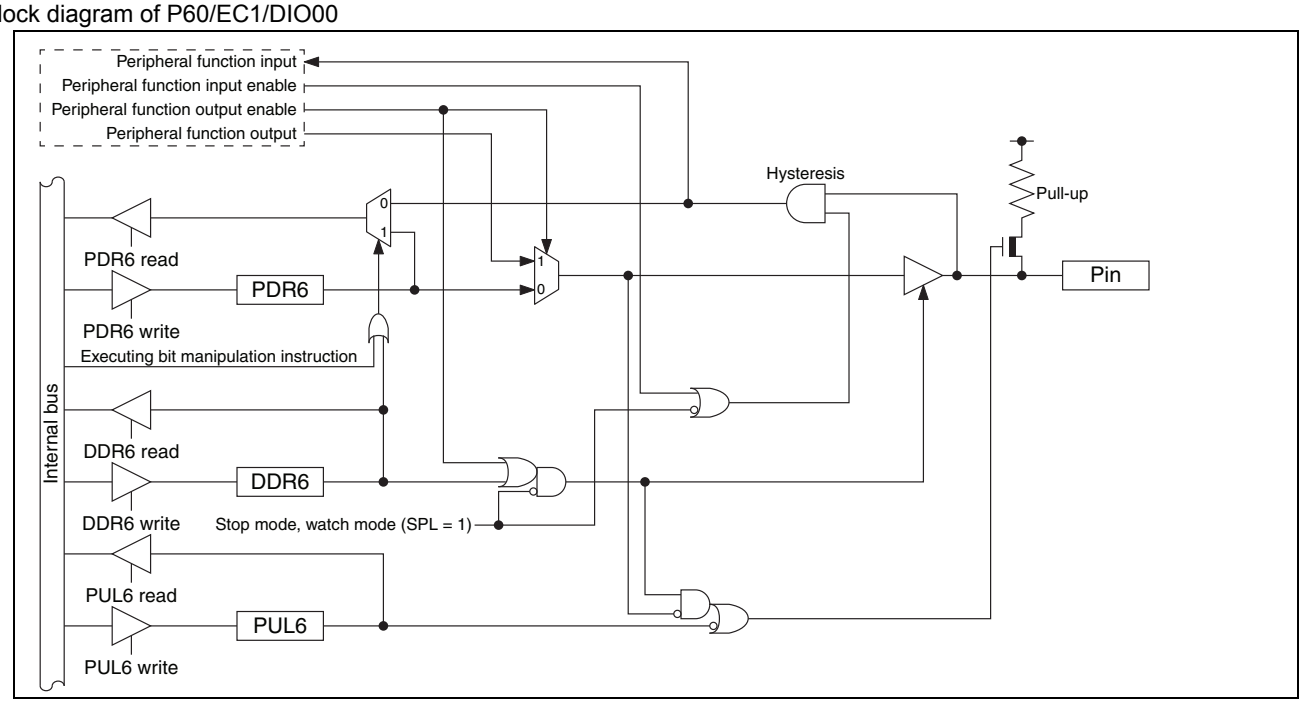
■ Port 6 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 6 data register (PDR6)
- ❒ Port 6 direction register (DDR6)
- ❒ Port 6 pull-up register (PUL6)
- ❒ Touch input disable register 0 (TIDR0)

2. Block diagrams of port 6

■ P60/EC1/DIO00 pin

This pin has the following peripheral functions:
- ❒ 8/16-bit composite timer ch. 1 clock input pin (EC1)
- ❒ TS direct output ch. 0 pin (DIO00)

■ Block diagram of P60/EC1/DIO00



■ P63/AREF pin

This pin has the following peripheral function:
- ❒ TS reference input pin (AREF)

■ P64/S00 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 0 input pin (S00)

■ P65/S01 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 1 input pin (S01)

■ P66/S02 pin

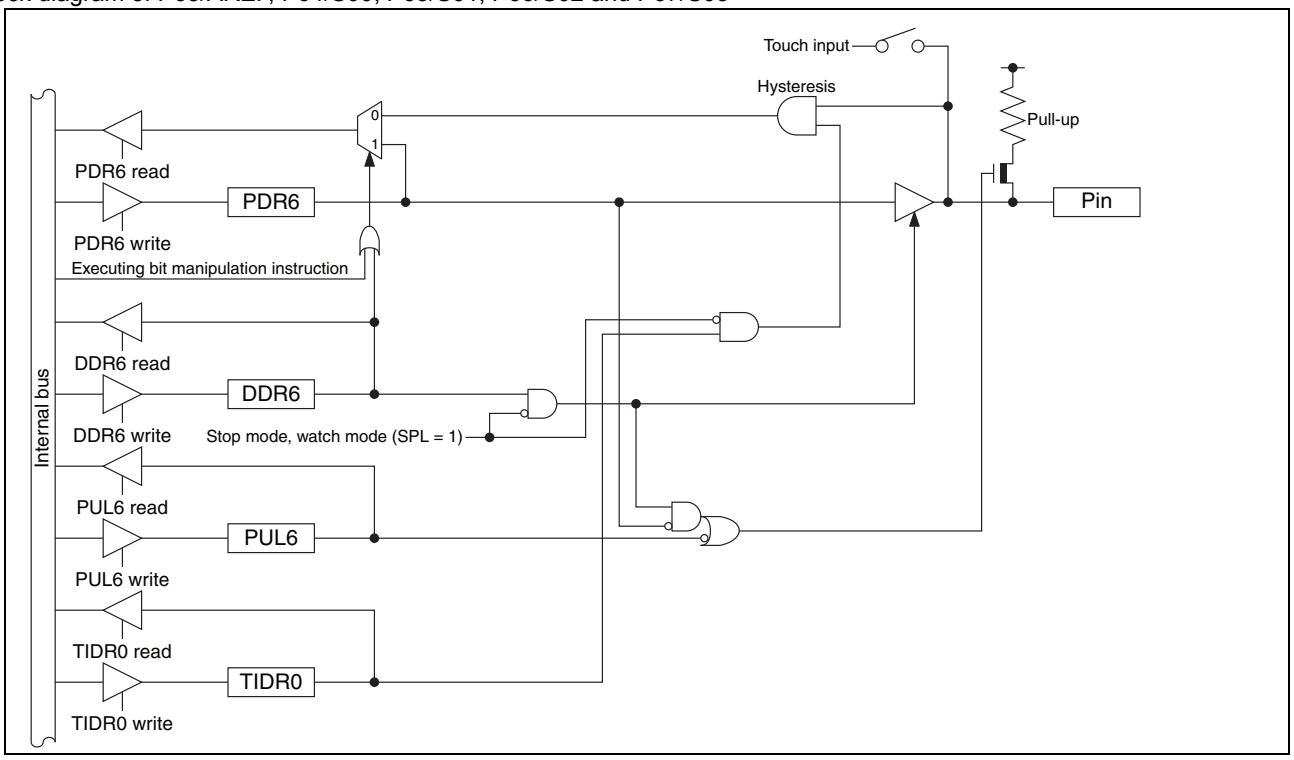
This pin has the following peripheral function:
- ❒ TS touch ch. 2 input pin (S02)

■ P67/S03 pin

This pin has the following peripheral function:

❒ TS touch ch. 3 input pin (S03)

■ Block diagram of P63/AREF, P64/S00, P65/S01, P66/S02 and P67/S03



3. Port 6 registers

■ Port 6 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR6	0	Pin state is “L” level.	PDR6 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR6 value is “1”.	As output port, outputs “H” level.
DDR6	0	Port input enabled		
	1	Port output enabled		
PUL6	0	Pull-up disabled		
	1	Pull-up enabled		
TIDR0	0	Touch input or reference input enabled		
	1	Port input enabled		

■ Correspondence between registers and pins for port 6

Pin name	Correspondence between related register bits and pins							
	P67	P66	P65	P64	P63	-	-	P60
PDR6	bit7	bit6	bit5	bit4	bit3	-	-	bit0
DDR6								
PUL6								
TIDR0	bit7	bit6	bit5	bit4	bit3			-

4. Port 7 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR7 register corresponding to that pin is set to “1”.
- ❒ When a pin is used as an output port, it outputs the value of the PDR7 register to external pins.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR7 register returns the PDR7 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR7 register corresponding to that pin is set to “0”.
- ❒ When using a pin shared with the touch input function as an input port, set the bit in the touch input disable register 1 (TIDR1) corresponding to that pin to “1”.
- ❒ If data is written to the PDR7 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR7 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR7 register, the PDR7 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR7 register are initialized to “0” and port input is enabled. As for a pin shared with the touch input function, its port input is disabled because the TIDR1 register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR7 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ When the stop enable bit in the TS prescaler control register (PSC:STPE) is set to “1”, the TS can operate in stop mode or watch mode, the touch input is enabled and is not blocked. The TS wakes up in stop mode or watch mode provided that the TINT (touch interrupt) and the GINT (general interrupt) are set to enable the TS to wake up in stop mode or watch mode.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

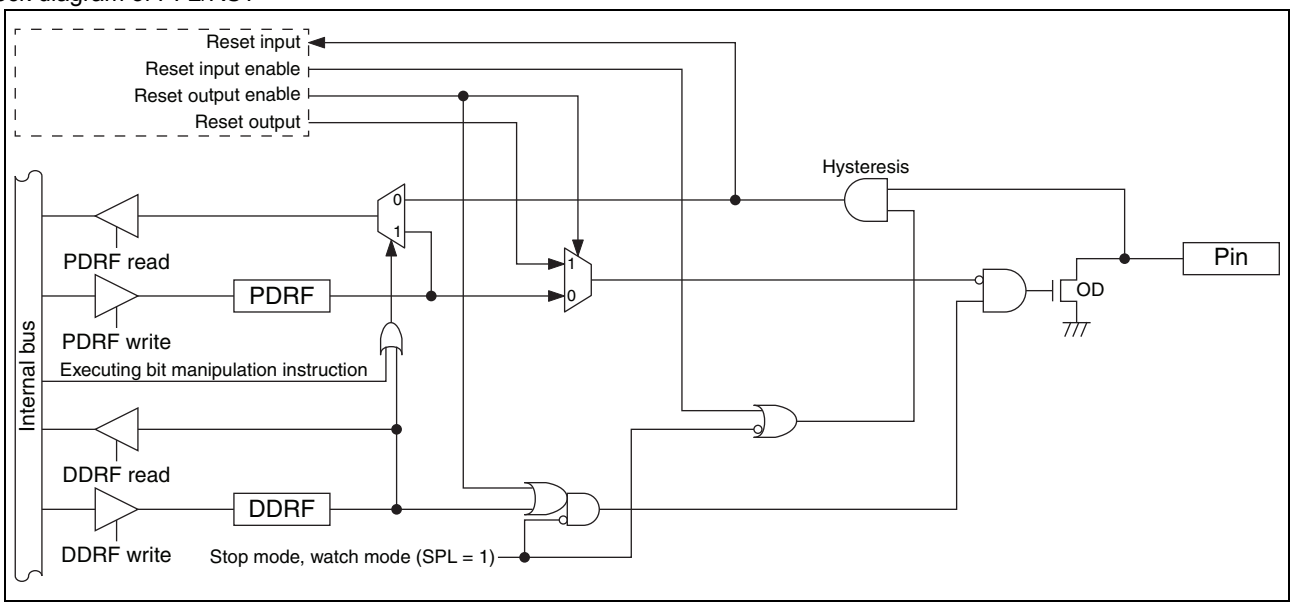
■ Operation as a touch input pin

Set the bit in the DDR7 register corresponding to the touch input pin to “0”, the bit in the TIDR1 register corresponding to the same pin to “0”, and the bit in the PUL7 register corresponding to the same pin to “0”.

■ Operation of the pull-up register

Setting the bit in the PUL7 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL7 register.

■ Block diagram of PF2/$\overline{\text{RST}}$



3. Port F registers

■ Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port F

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PF2	PF1	PF0
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

15. Interrupt Source Tables

15.1 MB95850K Series

Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High ↓ Low
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 6	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 7	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
Touch interrupt (TINT)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
General interrupt (GINT)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
—	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
—	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
—	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
Comparator ch. 0	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
—	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	

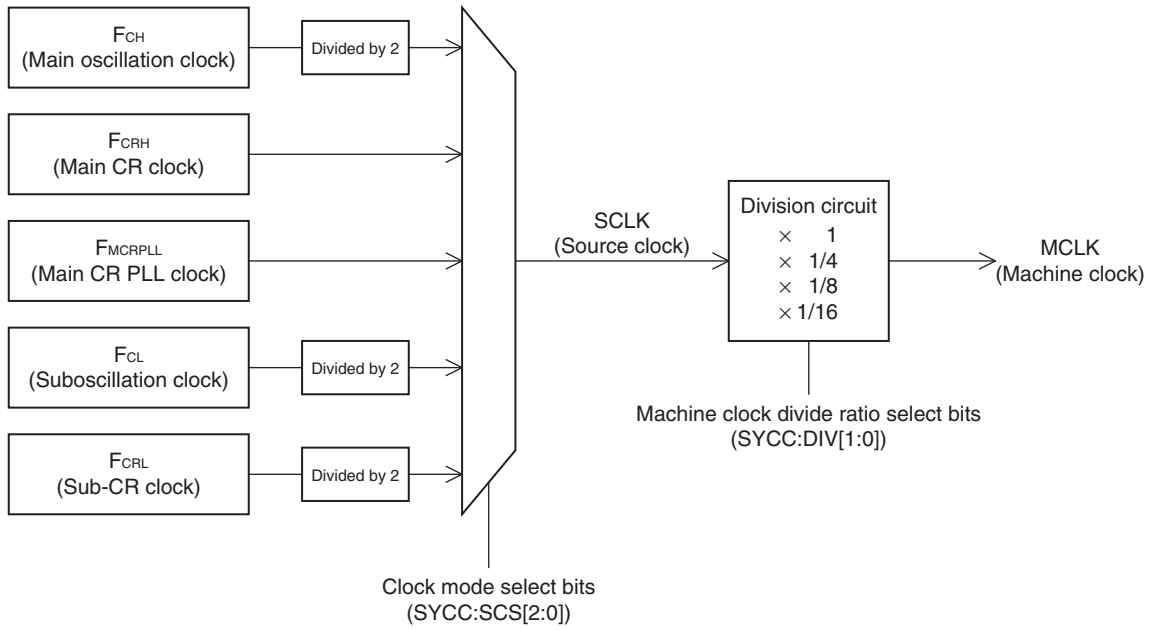
Pin name	Normal operation	Sleep mode	Stop mode		Watch mode		On reset
			SPL=0	SPL=1	SPL=0	SPL=1	
P12/BEEP	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*10 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*10 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P13/UI0/ DIO02	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P14/UO0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P15/UCK0	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P16/INT09/ TO11	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P17/INT08/ TO10							
P40/AN04/ PPG00	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P41/AN05/ PPG01							
P42/INT06/ PPG10	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P43/INT07/ PPG11							
P44/AN06/ TO00/DIO03	I/O port/ peripheral function I/O/ analog input	I/O port/ peripheral function I/O/ analog input	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept*5 Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input blocked*2
P45/AN07/ TO01/DIO04							
P46/SDA	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2, *11	Hi-Z Input blocked*2, *11	Previous state kept Input blocked*2, *11	Hi-Z Input blocked*2, *11	Hi-Z Input enabled*3 (However, it does not function.)
P47/SCL							
P60/EC1/ DIO00	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Previous state kept*5 Input blocked*2, *7	Hi-Z*6 Input blocked*2, *7	Hi-Z Input enabled*3 (However, it does not function.)
P61/PPG20	I/O port/ peripheral function I/O	I/O port/ peripheral function I/O	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Previous state kept Input blocked*2	Hi-Z*6 Input blocked*2	Hi-Z Input enabled*3 (However, it does not function.)
P62/PPG21							

17.3 DC Characteristics

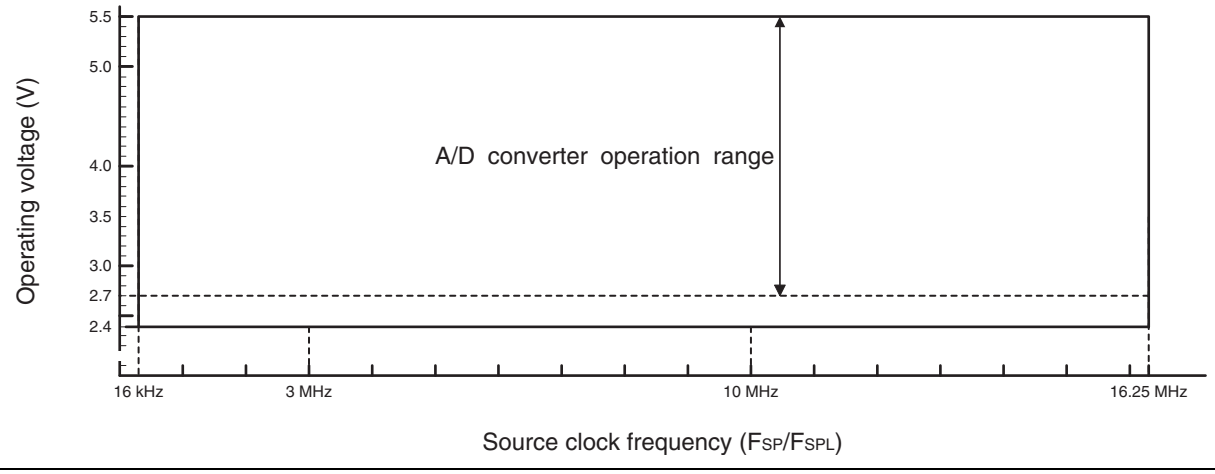
(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHI}	P13, P46, P47	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input level
	V_{IHS}	Other than P13, P46, P47, PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
	V_{IHM}	PF2	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{ILI}	P13, P46, P47	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input level
	V_{ILS}	Other than P13, P46, P47, PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
	V_{ILM}	PF2	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output application voltage	V_D	P10, P46, P47, PF2	—	V_{SS} – 0.3	—	Vss + 5.5	V	
"H" level output voltage	V_{OH1}	Output pins other than P06, P07, P10, P40 to P45, PF2	I_{OH} = –4 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P06, P07, P40 to P45	I_{OH} = –8 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Output pins other than P06, P07, P40 to P45	I_{OL} = 4 mA	—	—	0.4	V	
	V_{OL2}	P06, P07, P40 to P45	I_{OL} = 12 mA	—	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins	0.0 V < V_I < V_{CC}	–5	—	+5	µA	When the internal pull-up resistor is disabled
Internal pull-up resistor	R_{PULL}	Other than P10, P46, P47, PF0, PF1, PF2	V_I = 0 V	25	50	100	kΩ	When the internal pull-up resistor is enabled
Input capacitance	C_{IN}	Other than V_{CC} and V_{SS}	f = 1 MHz	—	5	15	pF	

■ Schematic diagram of the clock generation block



■ Operating voltage - Operating frequency (T_A = –40°C to +85°C)

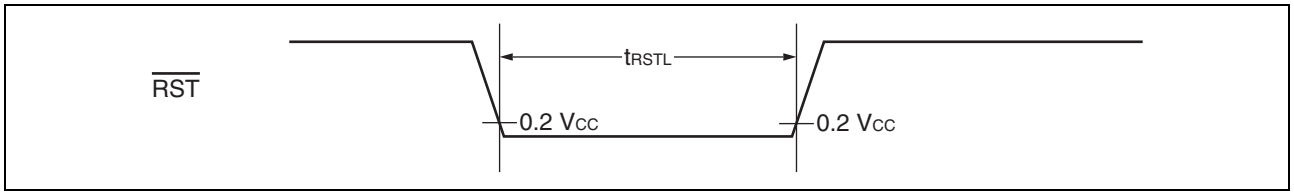


17.4.3 External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

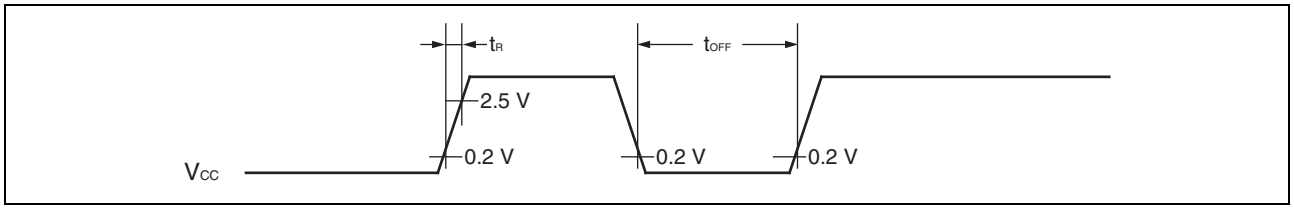
*: See "Source Clock/Machine Clock" for t_{MCLK}.



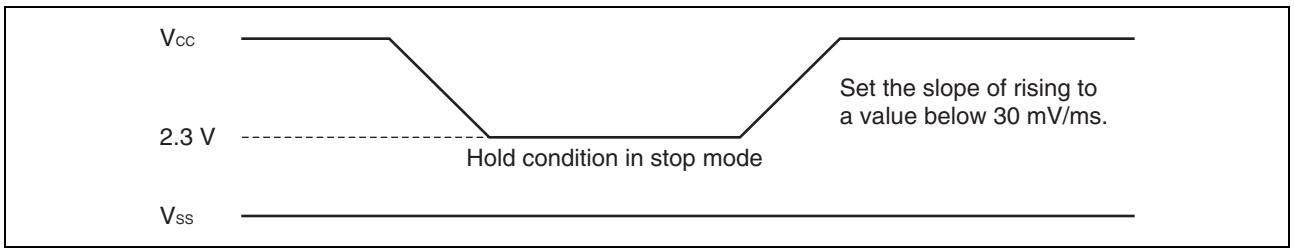
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



Document History Page

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	YSKA	08/02/2012	Migrated to Cypress and assigned document number 002-09305. No change to document contents or format.
*A	5560459	YSKA	12/20/2016	Migrated to Cypress datasheet template
*B	5844036	YSAT	08/04/2017	Adapted new Cypress logo
*C	6038234	YSAT	01/22/2018	Corrected the package codes as bellow FPT-24P-M10 → STI024 FPT-24P-M34 → SOL024 FPT-32P-M30 → LQB032 FPT-48P-M49 → LQA048 FPT-52P-M02 → LQC052 Updated “19. Package Dimension” Updated Arm trademark and the last page