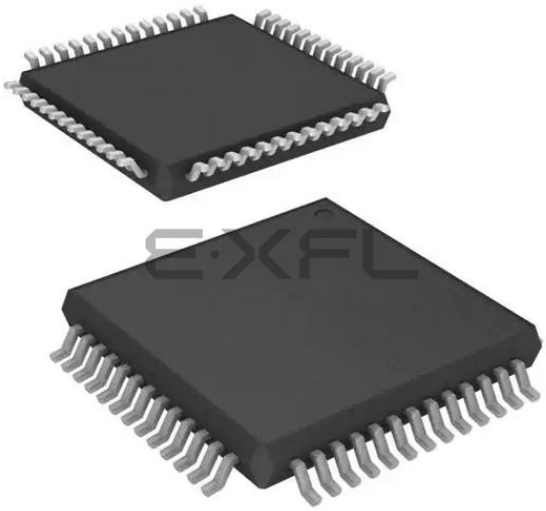

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Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	45
Program Memory Size	36KB (36K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.88V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f876kpmc1-g-sne2

5.3 MB95870K Series

Pin no.		Pin name	I/O circuit type[9]	Function	I/O type			
LQFP48[7]	LQFP52[8]				Input	Output	OD[10]	PU[11]
1	1	PF1	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X1		Main clock I/O oscillation pin				
2	2	PF0	B	General-purpose I/O port	Hysteresis	CMOS	—	—
		X0		Main clock input oscillation pin				
3	3	V_{SS}	—	Power supply pin (GND)	—	—	—	—
4	4	V_{CC}	—	Power supply pin	—	—	—	—
5	5	P77	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S11		TS touch ch. 11 input pin				
6	6	P76	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S10		TS touch ch. 10 input pin				
—	7	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—
7	8	P75	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S09		TS touch ch. 9 input pin				
8	9	P74	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S08		TS touch ch. 8 input pin				
9	10	P73	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S07		TS touch ch. 7 input pin				
10	11	P72	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S06		TS touch ch. 6 input pin				
11	12	P71	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S05		TS touch ch. 5 input pin				
12	13	P70	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S04		TS touch ch. 4 input pin				
13	14	P67	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S03		TS touch ch. 3 input pin				
14	15	P66	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S02		TS touch ch. 2 input pin				
15	16	P65	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S01		TS touch ch. 1 input pin				
16	17	P64	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		S00		TS touch ch. 0 input pin				
17	18	P63	F	General-purpose I/O port	Hysteresis/ analog	CMOS	—	O
		AREF		TS reference impedance input pin				
18	19	PF2	A	General-purpose I/O port	Hysteresis	CMOS	O	—
		RST		Reset pin				
—	20	NC	—	It is an internally connected pin. Always leave it unconnected.	—	—	—	—

Address	Register abbreviation	Register name	R/W	Initial value
0x007C	ILR3	Interrupt level setting register 3	R/W	0b11111111
0x007D	ILR4	Interrupt level setting register 4	R/W	0b11111111
0x007E	ILR5	Interrupt level setting register 5	R/W	0b11111111
0x007F	—	(Disabled)	—	—
0x0E10	BPFREQ	Beep output frequency register	R/W	0b00000000
0x0E11	TER0	TS touch channel enable register 0	R/W	0b00000000
0x0E12	TER1	TS touch channel enable register 1	R/W	0b00000000
0x0E13	PSC	TS prescaler control register	R/W	0b00100000
0x0E14	WRESET	TS warm reset register	R/W	0b00000000
0x0E15	RSEL0	TS sensitivity select register 0	R/W	0b00000010
0x0E16	RSEL1	TS sensitivity select register 1	R/W	0b00010010
0x0E17	RSEL2	TS sensitivity select register 2	R/W	0b00010010
0x0E18	RSEL3	TS sensitivity select register 3	R/W	0b00010010
0x0E19 to 0x0E1B	—	(Disabled)	—	—
0x0E1C	BPDUR	TS beep duration setting register	R/W	0b00000000
0x0E1D	DIOR1	TS direct output control register 1	R/W	0b00000000
0x0E1E	DIOR2	TS direct output control register 2	R/W	0b00000000
0x0E1F	DIOR3	TS direct output control register 3	R/W	0b00000000
0x0E20	FTSEL	TS feature select register	R/W	0b00000100
0x0E21	AICWAT	TS AIC wait time setting register	R/W	0b00100111
0x0E22	CALITV	TS calibration interval setting register	R/W	0b00110000
0x0E23	ITGTM	TS integration time setting register	R/W	0b00001111
0x0E24	IDLETM	TS idle time setting register	R/W	0b00001111
0x0E25	CONTROL	TS control register	R/W	0b00000000
0x0E26	INTMR	TS interrupt mask register	R/W	0b00011000
0x0E27	INTCR	TS interrupt clear register	R/W	0b00000000
0x0E28	FLTP	TS filter period setting register	R/W	0b00000000
0x0E29	FLTTH	TS filter threshold setting register	R/W	0b00000000
0x0E2A	REFDLY	TS reference delay setting register	R/W	0b00000000
0x0E2B to 0x0E30	—	(Disabled)	—	—
0x0E31	ALPH1	TS alpha value setting register ch. 1	R/W	0b00001000
0x0E32	ALPH2	TS alpha value setting register ch. 2	R/W	0b00001000
0x0E33	ALPH3	TS alpha value setting register ch. 3	R/W	0b00001000
0x0E34	ALPH4	TS alpha value setting register ch. 4	R/W	0b00001000
0x0E35	ALPH5	TS alpha value setting register ch. 5	R/W	0b00001000
0x0E36 to 0x0E3F	—	(Disabled)	—	—
0x0E40	BETA	TS beta value setting register	R/W	0b00000100
0x0E41 to 0x0E50	—	(Disabled)	—	—
0x0E51	STRTH1	TS touch strength threshold setting register ch. 1	R/W	0b00000001
0x0E52	STRTH2	TS touch strength threshold setting register ch. 2	R/W	0b00000001
0x0E53	STRTH3	TS touch strength threshold setting register ch. 3	R/W	0b00000001

4. Port 0 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR0 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR0 register to external pins.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR0 register returns the PDR0 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR0 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When using a pin shared with the analog input function as an input port, set the bit in the A/D input disable register (lower) (AIDRL) corresponding to that pin to “1”.
- ❒ If data is written to the PDR0 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR0 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR0 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR0 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR0 register corresponding to the input pin of a peripheral function to “0”.
- ❒ When using a pin shared with the analog input function as another peripheral function input pin, configure it as an input port by setting the bit in the AIDRL register corresponding to that pin to “1”.
- ❒ Reading the PDR0 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR0 register, the PDR0 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR0 register are initialized to “0” and port input is enabled. As for a pin shared with the analog input function, its port input is disabled because the AIDRL register is initialized to “0”.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR0 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT05), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an analog input pin
- ❒ Set the DDR0 register bit corresponding to analog input pin to “0” and the bit corresponding to that pin in the AIDRL register to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions. In addition, set the corresponding bit in the PUL0 register to “0”.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR0 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

■ Operation of the pull-up register

Setting the bit in the PUL0 register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PUL0 register.

■ Operation as a comparator input pin
- ❒ Set the bit in the AIDRL register corresponding to the comparator input pin to “0”.
- ❒ Regardless of the value of the PDR0 register and that of the DDR0 register, if the comparator analog input enable bit in the comparator control register ch. 0 (CMR0:VCID) is set to “0”, the comparator input function is enabled.
- ❒ To disable the comparator input function, set the VCID bit to “1”.
- ❒ For details of the comparator, see “CHAPTER 25 COMPARATOR” in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

3. Port 1 registers

■ Port 1 register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDR1	0	Pin state is “L” level.	PDR1 value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDR1 value is “1”.	As output port, outputs “H” level.*
DDR1	0	Port input enabled		
	1	Port output enabled		
PUL1	0	Pull-up disabled		
	1	Pull-up enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port 1

Pin name	Correspondence between related register bits and pins							
	-	-	P15	P14	P13	-	-	P10
PDR1	-	-	bit5	bit4	bit3	-	-	bit0*
DDR1								
PUL1								

*: Though P10 has no pull-up function, bit0 in the PUL1 register can still be accessed. The operation of P10 is not affected by the setting of bit0 in the PUL1 register.

4. Port 1 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR1 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR1 register to external pins.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR1 register returns the PDR1 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR1 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR1 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR1 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR1 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR1 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR1 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR1 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR1 register, the PDR1 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR1 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode

■ Correspondence between registers and pins for port 4

Pin name	Correspondence between related register bits and pins							
	P47	P46	-	-	-	-	-	-
PDR4	bit7	bit6	-	-	-	-	-	-
DDR4								

4. Port 4 operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDR4 register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDR4 register to external pins.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDR4 register returns the PDR4 register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDR4 register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDR4 register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDR4 register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDR4 register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDR4 register. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation as a peripheral function input pin
- ❒ To set a pin as an input port, set the bit in the DDR4 register corresponding to the input pin of a peripheral function to “0”.
- ❒ Reading the PDR4 register returns the pin value, regardless of whether the peripheral function uses that pin as its input pin. However, if the read-modify-write (RMW) type of instruction is used to read the PDR4 register, the PDR4 register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDR4 register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDR4 register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open. However, if the interrupt input is enabled for the external interrupt (INT06 and INT07), the input is enabled and not blocked.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation as an external interrupt input pin
- ❒ Set the bit in the DDR4 register corresponding to the external interrupt input pin to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ The pin value is always input to the external interrupt circuit. When using a pin for a function other than the interrupt, disable the external interrupt function corresponding to that pin.

14.2.4 Port 6

Port 6 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 6 configuration

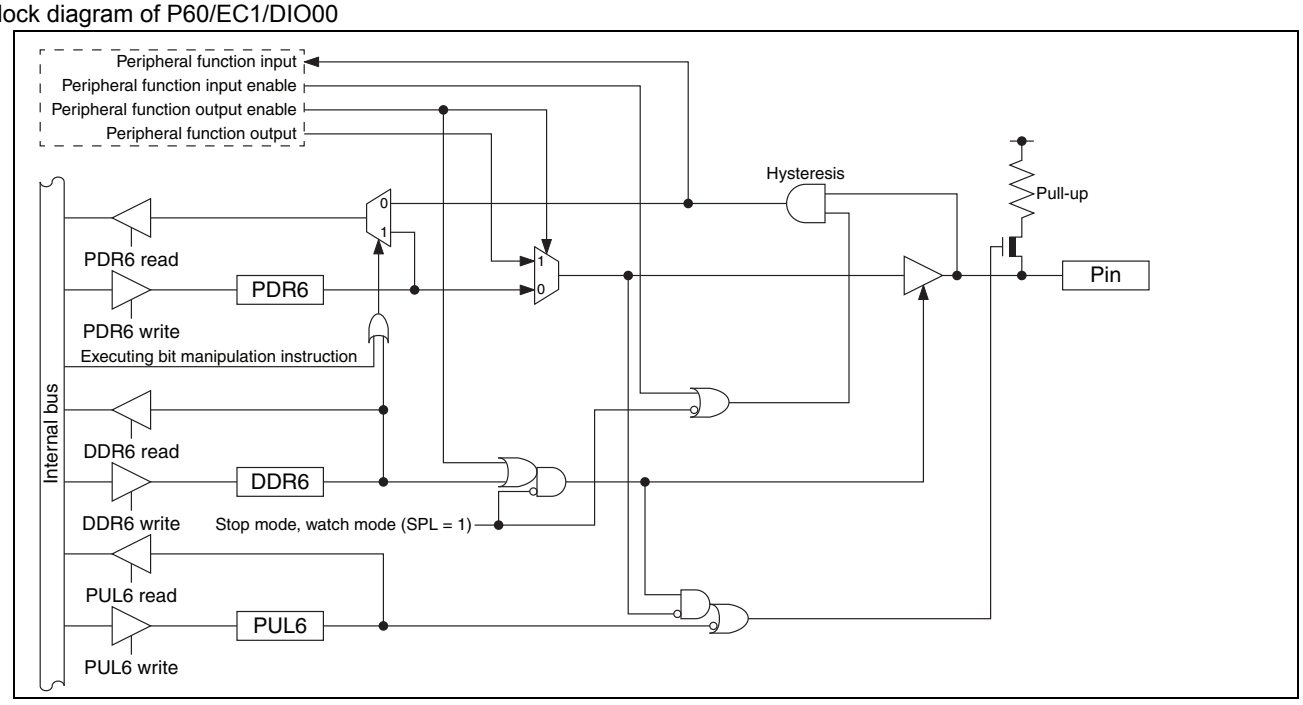
■ Port 6 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 6 data register (PDR6)
- ❒ Port 6 direction register (DDR6)
- ❒ Port 6 pull-up register (PUL6)
- ❒ Touch input disable register 0 (TIDR0)

2. Block diagrams of port 6

■ P60/EC1/DIO00 pin

This pin has the following peripheral functions:
- ❒ 8/16-bit composite timer ch. 1 clock input pin (EC1)
- ❒ TS direct output ch. 0 pin (DIO00)

■ Block diagram of P60/EC1/DIO00



■ P63/AREF pin

This pin has the following peripheral function:
- ❒ TS reference input pin (AREF)

■ P64/S00 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 0 input pin (S00)

■ P65/S01 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 1 input pin (S01)

■ P66/S02 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 2 input pin (S02)

14.2.5 Port 7

Port 7 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 7 configuration

■ Port 7 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 7 data register (PDR7)
- ❒ Port 7 direction register (DDR7)
- ❒ Port 7 pull-up register (PUL7)
- ❒ Touch input disable register 1 (TIDR1)

2. Block diagrams of port 7

■ P70/S04 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 4 input pin (S04)

■ P71/S05 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 5 input pin (S05)

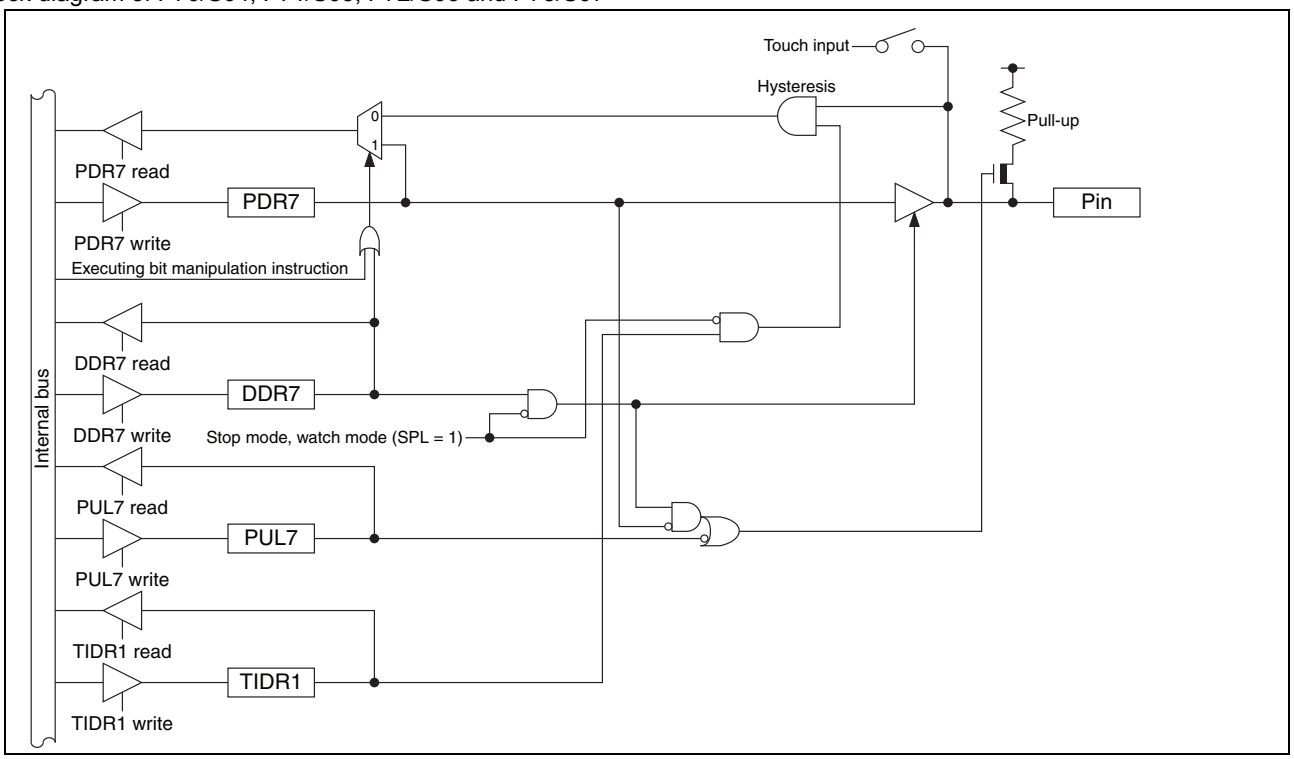
■ P72/S06 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 6 input pin (S06)

■ P73/S07 pin

This pin has the following peripheral function:
- ❒ TS touch ch. 7 input pin (S07)

■ Block diagram of P70/S04, P71/S05, P72/S06 and P73/S07



4. Port F operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- ❒ If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRF register returns the PDRF register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

3. Port G registers

■ Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

■ Correspondence between registers and pins for port G

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PG2	PG1	-
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

4. Port G operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- ❒ If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRG register returns the PDRG register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDRG register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRG register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

14.3.3 Port 4

Port 4 is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port 4 configuration

■ Port 4 is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port 4 data register (PDR4)
- ❒ Port 4 direction register (DDR4)
- ❒ Port 4 pull-up register (PUL4)
- ❒ A/D input disable register (lower) (AIDRL)

2. Block diagrams of port 4

■ P40/AN04/PPG00 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN04)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG00)

■ P41/AN05/PPG01 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN05)
- ❒ 8/16-bit PPG ch. 0 output pin (PPG01)

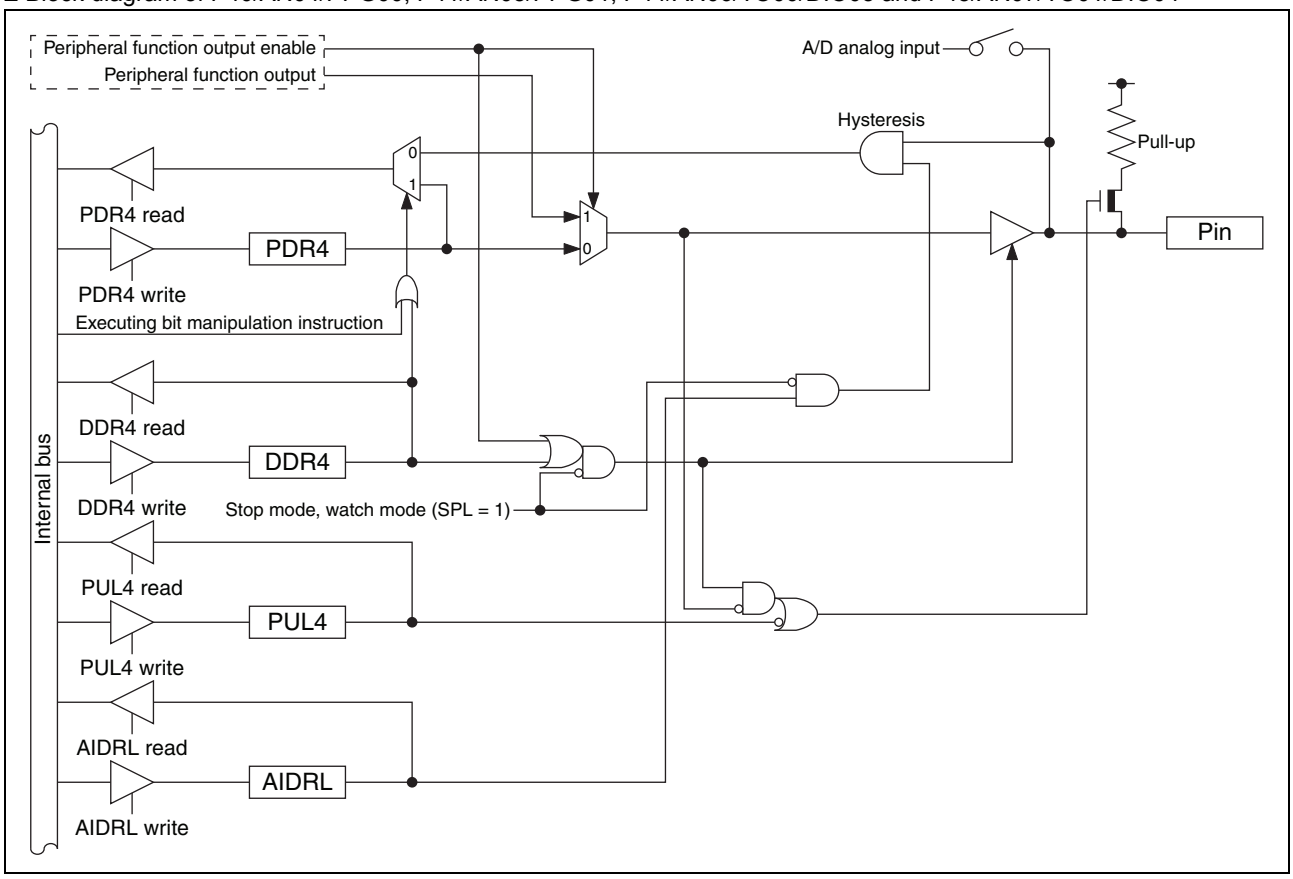
■ P44/AN06/TO00/DIO03 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN06)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO00)
- ❒ TS direct output ch. 3 pin (DIO03)

■ P45/AN07/TO01/DIO04 pin

This pin has the following peripheral functions:
- ❒ 8/10-bit A/D converter analog input pin (AN07)
- ❒ 8/16-bit composite timer ch. 0 output pin (TO01)
- ❒ TS direct output ch. 4 pin (DIO04)

■ Block diagram of P40/AN04/PPG00, P41/AN05/PPG01, P44/AN06/TO00/DIO03 and P45/AN07/TO01/DIO04



■ P42/INT06/PPG10 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT06)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG10)

■ P43/INT07/PPG11 pin

This pin has the following peripheral functions:

- ❒ External interrupt input pin (INT07)
- ❒ 8/16-bit PPG ch. 1 output pin (PPG11)

14.3.6 Port F

Port F is a general-purpose I/O port. This section focuses on its functions as a general-purpose I/O port. For details of peripheral functions, refer to their respective chapters in “New 8FX MB95850K/860K/870K Series Hardware Manual”.

1. Port F configuration

■ Port F is made up of the following elements.
- ❒ General-purpose I/O pins/peripheral function I/O pins
- ❒ Port F data register (PDRF)
- ❒ Port F direction register (DDRF)

2. Block diagrams of port F

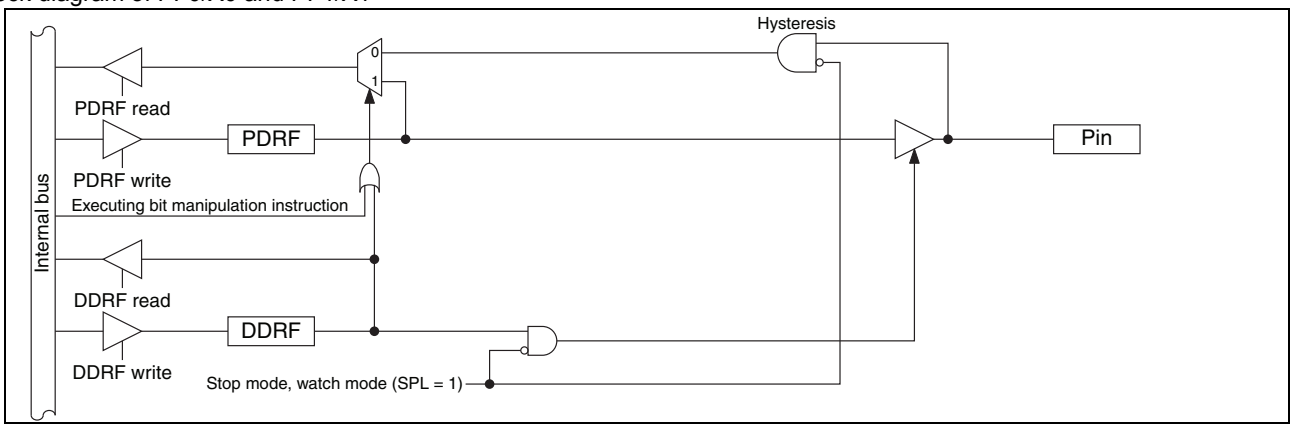
■ PF0/X0 pin

This pin has the following peripheral function:
- ❒ Main clock input oscillation pin (X0)

■ PF1/X1 pin

This pin has the following peripheral function:
- ❒ Main clock I/O oscillation pin (X1)

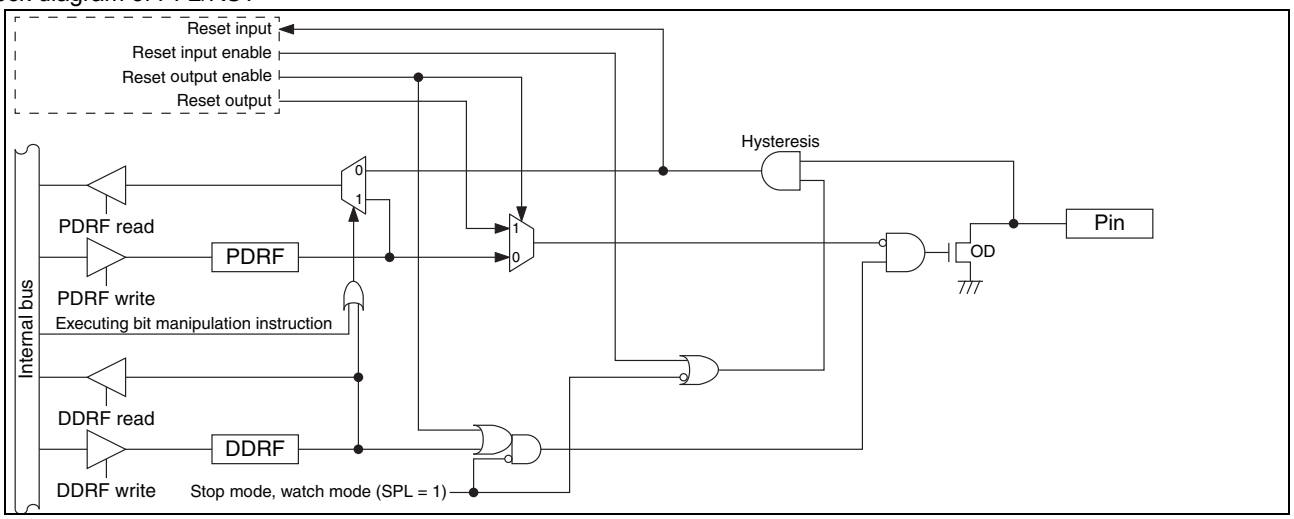
■ Block diagram of PF0/X0 and PF1/X1



■ PF2/$\overline{\text{RST}}$ pin

This pin has the following peripheral function:
- ❒ Reset pin ($\overline{\text{RST}}$)

■ Block diagram of PF2/$\overline{\text{RST}}$



3. Port F registers

■ Port F register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRF	0	Pin state is “L” level.	PDRF value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRF value is “1”.	As output port, outputs “H” level.*
DDRF	0	Port input enabled		
	1	Port output enabled		

*: If the pin is an N-ch open drain pin, the pin state becomes Hi-Z.

■ Correspondence between registers and pins for port F

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PF2	PF1	PF0
PDRF	-	-	-	-	-	bit2	bit1	bit0
DDRF								

4. Port F operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRF register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRF register to external pins.
- ❒ If data is written to the PDRF register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRF register returns the PDRF register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRF register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRF register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRF register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRF register, the PDRF register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRF register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRF register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

3. Port G registers

■ Port G register functions

Register abbreviation	Data	Read	Read by read-modify-write (RMW) instruction	Write
PDRG	0	Pin state is “L” level.	PDRG value is “0”.	As output port, outputs “L” level.
	1	Pin state is “H” level.	PDRG value is “1”.	As output port, outputs “H” level.
DDRG	0	Port input enabled		
	1	Port output enabled		
PULG	0	Pull-up disabled		
	1	Pull-up enabled		

■ Correspondence between registers and pins for port G

Pin name	Correspondence between related register bits and pins							
	-	-	-	-	-	PG2	PG1	-
PDRG	-	-	-	-	-	bit2	bit1	-
DDRG								
PULG								

4. Port G operations

■ Operation as an output port
- ❒ A pin becomes an output port if the bit in the DDRG register corresponding to that pin is set to “1”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ When a pin is used as an output port, it outputs the value of the PDRG register to external pins.
- ❒ If data is written to the PDRG register, the value is stored in the output latch and is output to the pin set as an output port as it is.
- ❒ Reading the PDRG register returns the PDRG register value.

■ Operation as an input port
- ❒ A pin becomes an input port if the bit in the DDRG register corresponding to that pin is set to “0”.
- ❒ For a pin shared with other peripheral functions, disable the output of such peripheral functions.
- ❒ If data is written to the PDRG register, the value is stored in the output latch but is not output to the pin set as an input port.
- ❒ Reading the PDRG register returns the pin value. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation as a peripheral function output pin
- ❒ A pin becomes a peripheral function output pin if the peripheral output function is enabled by setting the output enable bit of a peripheral function corresponding to that pin.
- ❒ The pin value can be read from the PDRG register even if the peripheral function output is enabled. Therefore, the output value of a peripheral function can be read by the read operation on the PDRG register. However, if the read-modify-write (RMW) type of instruction is used to read the PDRG register, the PDRG register value is returned.

■ Operation at reset

If the CPU is reset, all bits in the DDRG register are initialized to “0” and port input is enabled.

■ Operation in stop mode and watch mode
- ❒ If the pin state setting bit in the standby control register (STBC:SPL) is set to “1” and the device transits to stop mode or watch mode, the pin is compulsorily made to enter the high impedance state regardless of the DDRG register value. The input of that pin is locked to “L” level and blocked in order to prevent leaks due to input open.
- ❒ If the pin state setting bit is “0”, the state of the port I/O or that of the peripheral function I/O remains unchanged and the output level is maintained.

■ Operation of the pull-up register

Setting the bit in the PULG register to “1” makes the pull-up resistor be internally connected to the pin. When the pin output is “L” level, the pull-up resistor is disconnected regardless of the value of the PULG register.

15.2 MB95860K Series

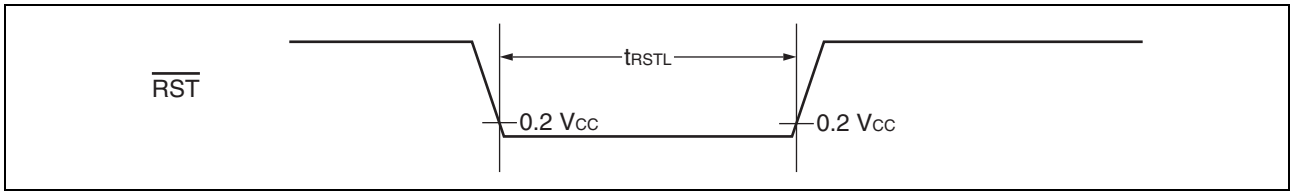
Interrupt source	Interrupt request number	Vector table address		Interrupt level setting register		Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower	Register	Bit	
External interrupt ch. 0	IRQ00	0xFFFA	0xFFFB	ILR0	L00 [1:0]	High ↓ Low
External interrupt ch. 4						
External interrupt ch. 1	IRQ01	0xFFF8	0xFFF9	ILR0	L01 [1:0]	
External interrupt ch. 5						
External interrupt ch. 2	IRQ02	0xFFF6	0xFFF7	ILR0	L02 [1:0]	
External interrupt ch. 6						
External interrupt ch. 3	IRQ03	0xFFF4	0xFFF5	ILR0	L03 [1:0]	
External interrupt ch. 7						
UART/SIO ch. 0	IRQ04	0xFFF2	0xFFF3	ILR1	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	0xFFF0	0xFFF1	ILR1	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	0xFFEE	0xFFEF	ILR1	L06 [1:0]	
Touch interrupt (TINT)	IRQ07	0xFFEC	0xFFED	ILR1	L07 [1:0]	
General interrupt (GINT)	IRQ08	0xFFEA	0xFFEB	ILR2	L08 [1:0]	
8/16-bit PPG ch. 1 (lower)	IRQ09	0xFFE8	0xFFE9	ILR2	L09 [1:0]	
8/16-bit PPG ch. 1 (upper)	IRQ10	0xFFE6	0xFFE7	ILR2	L10 [1:0]	
—	IRQ11	0xFFE4	0xFFE5	ILR2	L11 [1:0]	
8/16-bit PPG ch. 0 (upper)	IRQ12	0xFFE2	0xFFE3	ILR3	L12 [1:0]	
8/16-bit PPG ch. 0 (lower)	IRQ13	0xFFE0	0xFFE1	ILR3	L13 [1:0]	
8/16-bit composite timer ch. 1 (upper)	IRQ14	0xFFDE	0xFFDF	ILR3	L14 [1:0]	
—	IRQ15	0xFFDC	0xFFDD	ILR3	L15 [1:0]	
I^2C bus interface ch. 0	IRQ16	0xFFDA	0xFFDB	ILR4	L16 [1:0]	
—	IRQ17	0xFFD8	0xFFD9	ILR4	L17 [1:0]	
8/10-bit A/D converter	IRQ18	0xFFD6	0xFFD7	ILR4	L18 [1:0]	
Time-base timer	IRQ19	0xFFD4	0xFFD5	ILR4	L19 [1:0]	
Watch prescaler	IRQ20	0xFFD2	0xFFD3	ILR5	L20 [1:0]	
Watch counter						
Comparator ch. 0	IRQ21	0xFFD0	0xFFD1	ILR5	L21 [1:0]	
8/16-bit composite timer ch. 1 (lower)	IRQ22	0xFFCE	0xFFCF	ILR5	L22 [1:0]	
Flash memory	IRQ23	0xFFCC	0xFFCD	ILR5	L23 [1:0]	

17.4.3 External Reset

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{RST}$ "L" level pulse width	t_{RSTL}	2 t_{MCLK}*	—	ns	

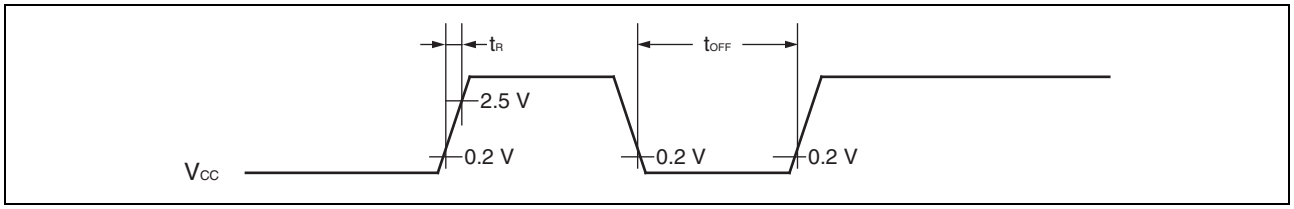
*: See "Source Clock/Machine Clock" for t_{MCLK}.



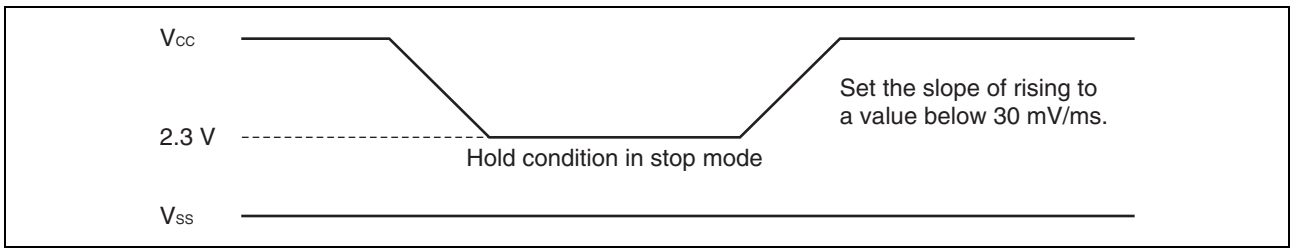
17.4.4 Power-on Reset

(V_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}	—	1	—	ms	Wait time until power-on



Note: A sudden change of power supply voltage may activate the power-on reset function. When changing the power supply voltage during the operation, set the slope of rising to a value below within 30 mV/ms as shown below.



17.5.3 Definitions of A/D Converter Terms

■ Resolution

It indicates the level of analog variation that can be distinguished by the A/D converter.

When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.

■ Linearity error (unit: LSB)

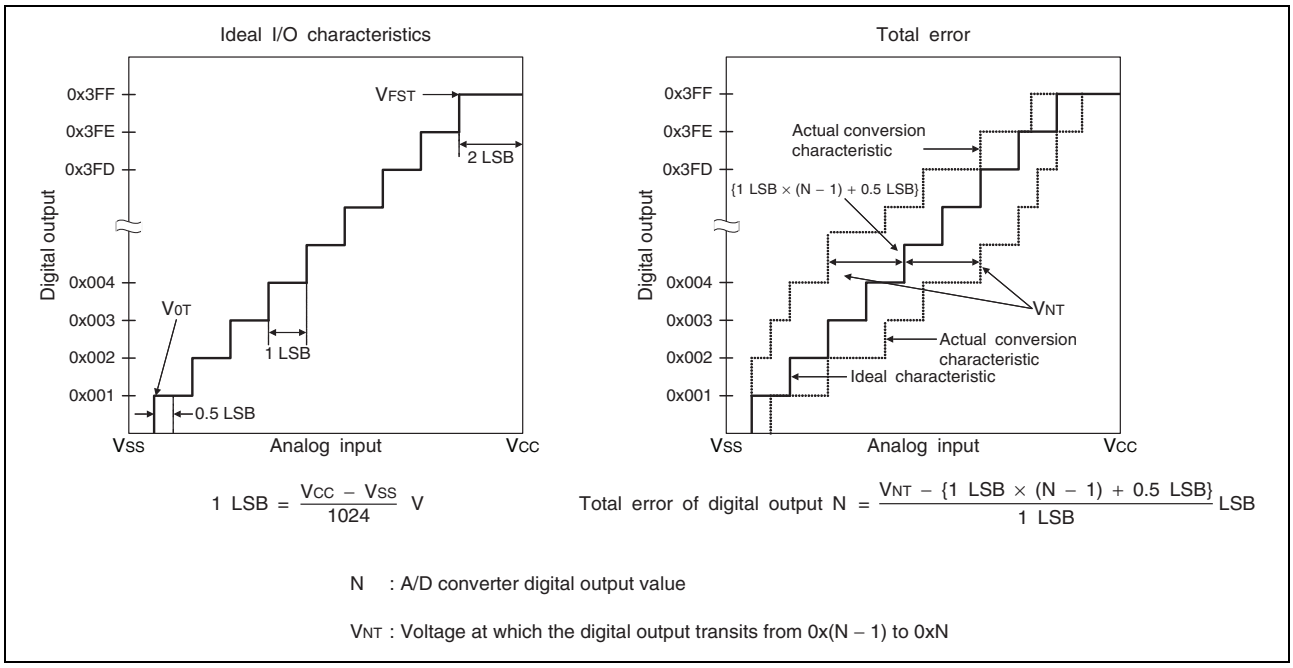
It indicates how much an actual conversion value deviates from the straight line connecting the zero transition point (“0000000000” ← → “0000000001”) of a device to the full-scale transition point (“1111111111” ← → “1111111110”) of the same device.

■ Differential linear error (unit: LSB)

It indicates how much the input voltage required to change the output code by 1 LSB deviates from an ideal value.

■ Total error (unit: LSB)

It indicates the difference between an actual value and a theoretical value. The error can be caused by a zero transition error, a full-scale transition errors, a linearity error, a quantum error, or noise.



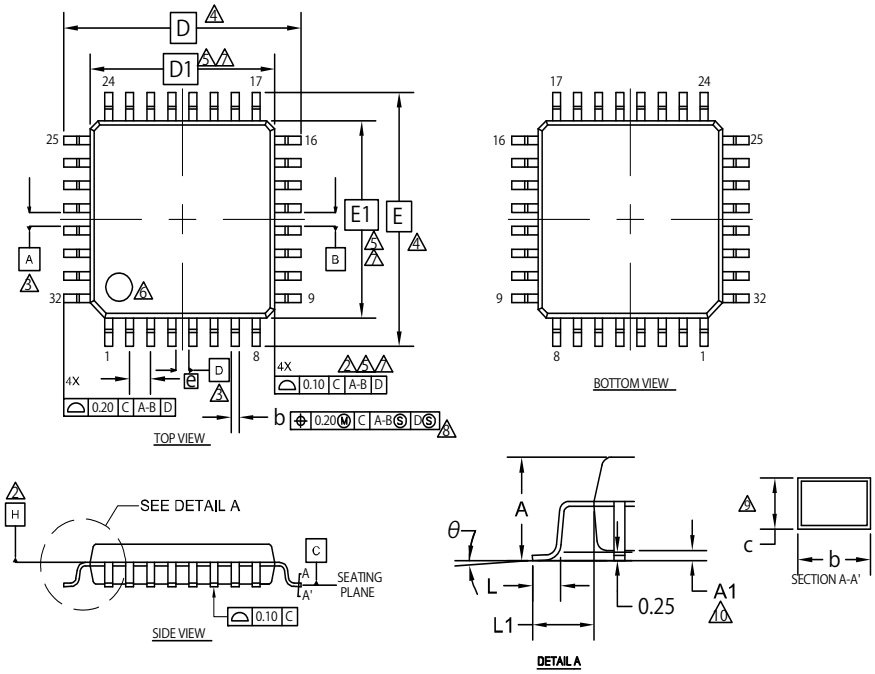
$$1\ \text{LSB} = \frac{V_{CC} - V_{SS}}{1024}\ \text{V}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ \text{LSB}$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from 0x(N – 1) to 0xN

Package Type	Package Code
LQFP 32	LQB032



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
b	0.32	0.35	0.43
c	0.13	—	0.18
D		9.00 BSC	
D1		7.00 BSC	
e		0.80 BSC	
E		9.00 BSC	
E1		7.00 BSC	
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13879 **

PACKAGE OUTLINE, 32 LEAD LQFP
7.0X7.0X1.6 MM LQB032 REV*.*

20. Major Changes in This Edition

Spansion Document Code: DS702-00013-0v02-E.

Page	Section	Details
11	Pin Functions MB95850K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
13	Pin Functions MB95860K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
17	Pin Functions MB95870K Series	Revised the function of the AREF pin. TS reference input pin ® TS reference impedance input pin
29	Pin Connection DBG pin	Revised details of "• DBG pin".
	$\overline{\text{RST}}$ pin	Revised details of "• $\overline{\text{RST}}$ pin".
40	I/O Map MB95850K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
42		Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX

Page	Section	Details
47	I/O Map MB95860K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
		Revised the register name of the RSEL4 register. TS resistance select register 4 → TS sensitivity select register 4
49		Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX
54	I/O Map MB95870K Series	Revised the register name of the RSEL0 register. TS resistance select register 0 → TS sensitivity select register 0
		Revised the register name of the RSEL1 register. TS resistance select register 1 → TS sensitivity select register 1
		Revised the register name of the RSEL2 register. TS resistance select register 2 → TS sensitivity select register 2
		Revised the register name of the RSEL3 register. TS resistance select register 3 → TS sensitivity select register 3
		Revised the register name of the RSEL4 register. TS resistance select register 4 → TS sensitivity select register 4
		Revised the register name of the RSEL5 register. TS resistance select register 5 → TS sensitivity select register 5
		Revised the register name of the RSEL6 register. TS resistance select register 6 → TS sensitivity select register 6
57	I/O MAP MB95870K Series	Corrected the initial value of the TOUCHH register. 0b00000XXX → 0b0000XXXX