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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	SPI, SSP
Clock Rate	160MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21992bstz

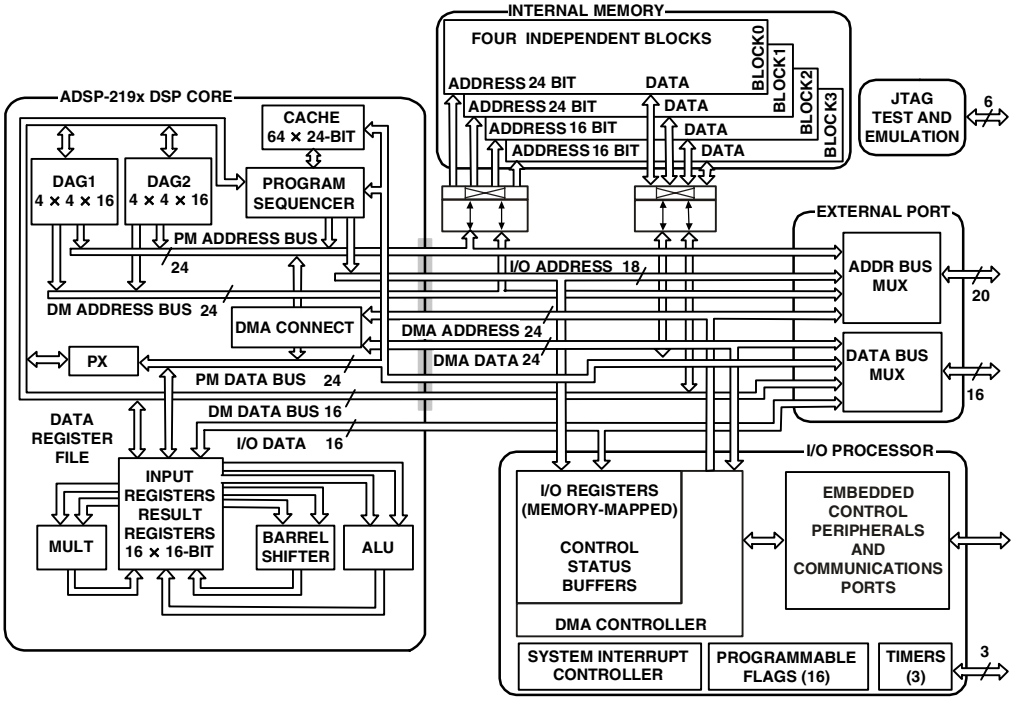

Figure 2. Block Diagram

an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The block diagram (Figure 2) shows the architecture of the embedded SHARC core. It contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data from the register file and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single cycle multiply, multiply/add, and multiply/subtract operations. The MAC has two 40-bit accumulators, which help with overflow. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

Register usage rules influence placement of input and results within the computational units. For most operations, the data registers of the computational units act as a data register file, permitting any input or result register to provide input to any unit for a computation. For feedback operations, the computational units let the output (result) of any unit be input to any unit on the next cycle. For conditional or multifunction instructions, there are restrictions on which data registers may provide inputs or receive results from each computational unit. For more information, see the *ADSP-2199x DSP Instruction Set Reference*.

A powerful program sequencer controls the flow of instruction execution. The sequencer supports conditional jumps, subroutine calls, and low interrupt overhead. With internal loop counters and loop stacks, the ADSP-21992 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four 16-bit address pointers. Whenever the pointer is used to access data (indirect addressing), it is pre- or post-modified by the value of one of four possible modify registers. A length value and base address may be associated with each pointer to implement automatic modulo addressing for circular buffers. Page registers in the DAGs allow circular addressing within 64K word boundaries of each of the 256 memory pages, but these buffers may not cross page boundaries. Secondary registers duplicate all the primary registers in the DAGs; switching between primary and secondary registers provides a fast context switch.

Efficient data transfer in the core is achieved with the use of internal buses:

- Program memory address (PMA) bus
- Program memory data (PMD) bus
- Data memory address (DMA) bus
- Data memory data (DMD) bus
- Direct memory access address bus
- Direct memory access data bus

- SPORT operates at a frequency of up to one-half the clock frequency of the HCLK.
- SPORT: Capable of UART software emulation.

CONTROLLER AREA NETWORK (CAN) MODULE

The ADSP-21992 contains a controller area network (CAN) module. Key features of the CAN module are:

- Conforms to the CAN V2.0B standard.
- Supports both standard (11-bit) and extended (29-bit) identifiers.

  Supports data rates of up to 1 Mbps (and higher).
- 16 configurable mailboxes (all receive or transmit).
- Dedicated acceptance mask for each mailbox.
- Data filtering (first 2 bytes) which can be used for acceptance filtering.
- Error status and warning registers.
- Transmit priority by identifier.
- Universal counter module.
- Readable receive and transmit counters.

The CAN module is a low baud rate serial interface intended for use in applications where baud rates are typically under 1 Mbps. The CAN protocol incorporates a data CRC check, message error tracking and fault node confinement as means to improve network reliability to the level required for control applications.

The CAN module architecture is based around a 16-entry mailbox RAM. The mailbox is accessed sequentially by the CAN serial interface or the host CPU. Each mailbox consists of eight 16-bit data words. The data is divided into fields, which includes a message identifier, a time stamp, a byte count, up to 8 bytes of data, and several control bits. Each node monitors the messages being passed on the network. If the identifier in the transmitted message matches an identifier in one of its mailboxes, then the module knows that the message was meant for it, passes the data into its appropriate mailbox, and signals the host of its arrival with an interrupt.

The CAN network itself is a single, differential pair line. All nodes continuously monitor this line. There is no clock wire. Messages are passed in one of four standard message types or frames. Synchronization is achieved by an elaborate sync scheme performed in each CAN receiver. Message arbitration is accomplished one bit at a time. A dominant polarity is established for the network. All nodes are allowed to start transmitting at the same time following a frame sync pulse.

As each node transmits a bit, it checks to see if the bus is the same state that it transmitted. If it is, it continues to transmit. If not, then another node has transmitted a dominant bit so the first node knows it has lost the arbitration and it stops transmitting. The arbitration continues, bit by bit until only one node is left transmitting.

The electrical characteristics of each network connection are very stringent so the CAN interface is typically divided into two parts: a controller and a transceiver. This allows a single controller to support different drivers and CAN networks. The ADSP-21992 CAN module represents only the controller part of the interface. The network I/O of this module is a single transmit line and a single receive line, which communicate to a line transceiver.

ANALOG-TO-DIGITAL CONVERSION SYSTEM

The ADSP-21992 contains a fast, high accuracy, multiple input analog-to-digital conversion system with simultaneous sampling capabilities. This analog-to-digital conversion system permits the fast, accurate conversion of analog signals needed in high performance embedded systems. Key features of the ADC system are:

- 14-bit pipeline (6-stage pipeline) flash analog-to-digital converter.
- 8 dedicated analog inputs.
- Dual-channel simultaneous sampling capability.
- Programmable ADC clock rate to maximum of HCLK ÷ 4.
- First channel ADC data valid approximately 375 ns after CONVST (at 20 MSPS).
- All 8 inputs converted in approximately 725 ns (at 20 MSPS).
- 2.0 V peak-to-peak input voltage range.
- Multiple convert start sources.
- Internal or external voltage reference.
- Out of range detection.
- DMA capable transfers from ADC to memory.

The ADC system is based on a pipeline flash converter core, and contains dual input sample-and-hold amplifiers so that simultaneous sampling of two input signals is supported. The ADC system provides an analog input voltage range of 2.0 V p-p and provides 14-bit performance with a clock rate of up to HCLK ÷ 4. The ADC system can be programmed to operate at a clock rate from HCLK/4 to HCLK/30, to a maximum clock rate of 20 MHz (at 160 MHz CCLK rate).

The ADC input structure supports eight independent analog inputs; four of which are multiplexed into one sample-and-hold amplifier (A_SHA) and four of which are multiplexed into the other sample-and-hold amplifier (B_SHA).

At the 20 MHz sampling rate, the first data value is valid approximately 375 ns after the convert start command. All eight channels are converted in approximately 725 ns.

The core of the ADSP-21992 provides 14-bit data such that the stored data values in the ADC data registers are 14 bits wide.

VOLTAGE REFERENCE

The ADSP-21992 contains an on-board band gap reference that can be used to provide a precise 1.0 V output for use by the analog-to-digital system and externally on the VREF pin for biasing and level shifting functions. Additionally, the ADSP-21992 may be configured to operate with an external reference applied to the VREF pin, if required.

Table 2. Interrupt Priorities/Addresses (Continued)

Interrupt	IMASK/ IRPTL	Vector Address
User Assigned Interrupt (USR1)	5	0x00 00A0
User Assigned Interrupt (USR2)	6	0x00 00C0
User Assigned Interrupt (USR3)	7	0x00 00E0
User Assigned Interrupt (USR4)	8	0x00 0100
User Assigned Interrupt (USR5)	9	0x00 0120
User Assigned Interrupt (USR6)	10	0x00 0140
User Assigned Interrupt (USR7)	11	0x00 0160
User Assigned Interrupt (USR8)	12	0x00 0180
User Assigned Interrupt (USR9)	13	0x00 01A0
User Assigned Interrupt (USR10)	14	0x00 01C0
User Assigned Interrupt (USR11) —Lowest Priority	15	0x00 01E0

There is no assigned priority for the peripheral interrupts after reset. To assign the peripheral interrupts a different priority, applications write the new priority to their corresponding control bits (determined by their ID) in the interrupt priority control register.

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The emulation, power-down, and reset interrupts are nonmaskable with the IMASK register, but software can use the DIS INT instruction to mask the power-down interrupt.

The interrupt control (ICNTL) register controls interrupt nesting and enables or disables interrupts globally.

The IRPTL register is used to force and clear interrupts. On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. To support interrupt, loop, and subroutine nesting, the PC stack is 33 levels deep, the loop stack is eight levels deep, and the status stack is 16 levels deep. To prevent stack overflow, the PC stack can generate a stack level interrupt if the PC stack falls below three locations full or rises above 28 locations full.

The following instructions globally enable or disable interrupt servicing, regardless of the state of IMASK.

- Ena Int
- Dis Int

At reset, interrupt servicing is disabled.

For quick servicing of interrupts, a secondary set of DAG and computational registers exist. Switching between the primary and secondary registers lets programs quickly service interrupts, while preserving the state of the DSP.

PERIPHERAL INTERRUPT CONTROLLER

The peripheral interrupt controller is a dedicated peripheral unit of the ADSP-21992 (accessed via I/O mapped registers). The peripheral interrupt controller manages the connection of up to 32 peripheral interrupt requests to the DSP core.

For each peripheral interrupt source, there is a unique 4-bit code that allows the user to assign the particular peripheral interrupt to any one of the 12 user assignable interrupts of the embedded ADSP-2199x core. Therefore, the peripheral interrupt controller of the ADSP-21992 contains eight 16-bit interrupt priority registers (Interrupt Priority Register 0 (IPR0) to Interrupt Priority Register 7 (IPR7)).

Each interrupt priority register contains four 4-bit codes; one specifically assigned to each peripheral interrupt. The user may write a value between 0x0 and 0xB to each 4-bit location in order to effectively connect the particular interrupt source to the corresponding user assignable interrupt of the ADSP-2199x core.

Writing a value of 0x0 connects the peripheral interrupt to the USR0 user assignable interrupt of the ADSP-2199x core while writing a value of 0xB connects the peripheral interrupt to the USR11 user assignable interrupt. The core interrupt USR0 is the highest priority user interrupt, while USR11 is the lowest priority. Writing a value between 0xC and 0xF effectively disables the peripheral interrupt by not connecting it to any ADSP-2199x core interrupt input. The user may assign more than one peripheral interrupt to any given ADSP-2199x core interrupt. In that case, the burden is on the user software in the interrupt vector table to determine the exact interrupt source through reading status bits.

This scheme permits the user to assign the number of specific interrupts that are unique to their application to the interrupt scheme of the ADSP-2199x core. The user can then use the existing interrupt priority control scheme to dynamically control the priorities of the 12 core interrupts.

LOW POWER OPERATION

The ADSP-21992 has four low power options that significantly reduce the power dissipation when the device operates under standby conditions. To enter any of these modes, the DSP executes an IDLE instruction. The ADSP-21992 uses the

configuration of the PD, STCK, and STALL bits in the PLLCTL register to select between the low power modes as the DSP executes the IDLE instruction. Depending on the mode, an IDLE shuts off clocks to different parts of the DSP in the different modes. The low power modes are:

- Idle
- Power-down core
- Power-down core/peripherals
- Power-down all

Idle Mode

When the ADSP-21992 is in idle mode, the DSP core stops executing instructions, retains the contents of the instruction pipeline, and waits for an interrupt. The core clock and peripheral clock continue running.

To enter idle mode, the DSP can execute the IDLE instruction anywhere in code. To exit idle mode, the DSP responds to an interrupt and (after two cycles of latency) resumes executing instructions.

Power-Down Core Mode

When the ADSP-21992 is in power-down core mode, the DSP core clock is off, but the DSP retains the contents of the pipeline and keeps the PLL running. The peripheral bus keeps running, letting the peripherals receive data.

To exit power-down core mode, the DSP responds to an interrupt and (after two cycles of latency) resumes executing instructions.

Power-Down Core/Peripherals Mode

When the ADSP-21992 is in power-down core/peripherals mode, the DSP core clock and peripheral bus clock are off, but the DSP keeps the PLL running. The DSP does not retain the contents of the instruction pipeline. The peripheral bus is stopped, so the peripherals cannot receive data.

To exit power-down core/peripherals mode, the DSP responds to an interrupt and (after five to six cycles of latency) resumes executing instructions.

Power-Down All Mode

When the ADSP-21992 is in power-down all mode, the DSP core clock, the peripheral clock, and the PLL are all stopped. The DSP does not retain the contents of the instruction pipeline. The peripheral bus is stopped, so the peripherals cannot receive data.

To exit power-down core/peripherals mode, the DSP responds to an interrupt and (after 500 cycles to restabilize the PLL) resumes executing instructions.

CLOCK SIGNALS

The ADSP-21992 can be clocked by a crystal oscillator or a buffered, shaped clock derived from an external clock oscillator. If a crystal oscillator is used, the crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 6. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel resonant, fundamental frequency, microprocessor grade crystal should be used for this configuration.

If a buffered, shaped clock is used, this external clock connects to the DSP CLKIN pin. CLKIN input cannot be halted, changed, or operated below the specified frequency during normal operation. This clock signal should be a TTL-compatible signal. When an external clock is used, the XTAL input must be left unconnected.

The DSP provides a user-programmable 1× to 32× multiplication of the input clock, including some fractional values, to support 128 external to internal (DSP core) clock ratios. The BYPASS pin, and MSEL6–0 and DF bits, in the PLL configuration register, decide the PLL multiplication factor at reset. At runtime, the multiplication factor can be controlled in software. To support input clocks greater that 100 MHz, the PLL uses an additional bit (DF). If the input clock is greater than 100 MHz, DF must be set. If the input clock is less than 100 MHz, DF must be cleared. For clock multiplier settings, see the *ADSP-2199x DSP Hardware Reference Manual*.

The peripheral clock is supplied to the CLKOUT pin.

All on-chip peripherals for the ADSP-21992 operate at the rate set by the peripheral clock. The peripheral clock (HCLK) is either equal to the core clock rate or one half the DSP core clock rate (CCLK). This selection is controlled by the IOSEL bit in the PLLCTL register. The maximum core clock is 160 MHz for the ADSP-21992BST, 150 MHz for both the ADSP-21992BBC and ADSP-21992YBC, and 100 MHz for the ADSP-21992YST. The maximum peripheral clock is 80 MHz for the ADSP-21992BST, 75 MHz for both the ADSP-21992BBC and ADSP-21992YBC, and 50 MHz for the ADSP-21992YST—the combination of the input clock and core/peripheral clock ratios may not exceed these limits.

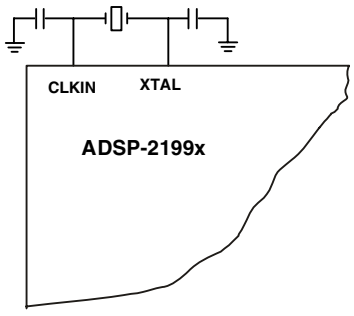

Figure 6. External Crystal Connections

RESET AND POWER-ON RESET (POR)

The $\overline{\text{RESET}}$ pin initiates a complete hardware reset of the ADSP-21992 when pulled low. The $\overline{\text{RESET}}$ signal must be asserted when the device is powered up to assure proper initialization. The ADSP-21992 contains an integrated power-on reset (POR) circuit that provides an output reset signal, $\overline{\text{POR}}$, from the ADSP-21992 on power-up and if the power supply voltage falls below the threshold level. The ADSP-21992 may be reset

from an external source using the $\overline{\text{RESET}}$ signal, or alternatively, the internal power-on reset circuit may be used by connecting the $\overline{\text{POR}}$ pin to the $\overline{\text{RESET}}$ pin. During power-up the $\overline{\text{RESET}}$ line must be activated for long enough to allow the DSP core's internal clock to stabilize. The power-up sequence is defined as the total time required for the crystal oscillator to stabilize after a valid VDD is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 512 cycles will ensure that the PLL has locked (this does not include the crystal oscillator start-up time).

The $\overline{\text{RESET}}$ input contains some hysteresis. If an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the circuit should use an external Schmitt trigger.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and resets all registers to their default values (where applicable). When $\overline{\text{RESET}}$ is released, if there is no pending bus request, program control jumps to the location of the on-chip boot ROM (0xFF0000) and the booting sequence is performed.

POWER SUPPLIES

The ADSP-21992 has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply must be connected to a 3.3 V supply. All external supply pins must be connected to the same supply. The ideal power-on sequence for the DSP is to provide power-up of all supplies simultaneously. If there is going to be some delay in power-up between the supplies, provide V_{DD} first, then V_{DD_IO}.

BOOTING MODES

The ADSP-21992 supports a number of different boot modes that are controlled by the three dedicated hardware boot mode control pins (BMODE2, BMODE1, and BMODE0). The use of three boot mode control pins means that up to eight different boot modes are possible. Of these only five modes are valid on the ADSP-21992. The ADSP-21992 exposes the boot mechanism to software control by providing a nonmaskable boot interrupt that vectors to the start of the on-chip ROM memory block (at address 0xFF0000). A boot interrupt is automatically initiated following either a hardware initiated reset, via the $\overline{\text{RESET}}$ pin, or a software initiated reset, via writing to the software reset register. Following either a hardware or a software reset, execution always starts from the boot ROM at address 0xFF0000, irrespective of the settings of the BMODE2, BMODE1, and BMODE0 pins. The dedicated BMODE2, BMODE1, and BMODE0 pins are sampled at hardware reset.

The particular boot mode for the ADSP-21992 associated with the settings of the BMODE2, BMODE1, BMODE0 pins is defined in Table 3.

Table 3. Summary of Boot Modes

Boot Mode	BMODE2	BMODE1	BMODE0	Function
0	0	0	0	Illegal–Reserved
1	0	0	1	Boot from External 8-Bit Memory over EMI
2	0	1	0	Execute from External 8-Bit Memory
3	0	1	1	Execute from External 16-Bit Memory
4	1	0	0	Boot from SPI ≤ 4K Bits
5	1	0	1	Boot from SPI > 4K Bits
6	1	1	0	Illegal–Reserved
7	1	1	1	Illegal–Reserved

INSTRUCTION SET DESCRIPTION

The ADSP-21992 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the unique architecture of the processor, offers the following benefits:

- SHARC assembly language syntax is a superset of and source code compatible (except for two data registers and DAG base address registers) with ADSP-21xx family syntax. It may be necessary to restructure ADSP-21xx programs to accommodate the unified memory space of the ADSP-21992 and to conform to its interrupt vector map.
- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction, but two, assembles into a single, 24-bit word that can execute in a single instruction cycle. The exceptions are two dual word instructions. One writes 16- or 24-bit immediate data to memory, and the other is an absolute jump/call with the 24-bit address specified in the instruction.
- Multifunction instructions allow parallel execution of an arithmetic, MAC, or shift instruction with up to two fetches or one write to processor memory space during a single instruction cycle.
- Program flow instructions support a wider variety of conditional and unconditional jumps/calls and a larger set of conditions on which to base execution of conditional instructions.

DEVELOPMENT TOOLS

The ADSP-21992 is supported with a complete set of CROSSCORE™ software and hardware development tools, including Analog Devices emulators and VisualDSP++™ development environment. The emulator hardware that supports other SHARC DSPs also fully emulates the ADSP-21992.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The DSP has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have a significant influence on the design development schedule by increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the SHARC development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the command line switches of the tool

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning, when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Table 4. Pin Descriptions (Continued)

Name	Type	Function
BSHAN	A, I	Inverting SHA_B Input
CAPT	A, O	Noise Reduction Pin
CAPB	A, O	Noise Reduction Pin
VREF	A, I, O	Voltage Reference Pin (Mode Selected by State of SENSE)
SENSE	A, I	Voltage Reference Select Pin
CML	A, O	Common-Mode Level Pin
CONVST	D, I	ADC Convert Start Input
CANRX	D, I	Controller Area Network (CAN) Receive
CANTX	D, OT	Controller Area Network (CAN) Transmit
PF15	D, BT, PD	General-Purpose IO15
PF14	D, BT, PD	General-Purpose IO14
PF13	D, BT, PD	General-Purpose IO13
PF12	D, BT, PD	General-Purpose IO12
PF11	D, BT, PD	General-Purpose IO11
PF10	D, BT, PD	General-Purpose IO10
PF9	D, BT, PD	General-Purpose IO9
PF8	D, BT, PD	General-Purpose IO8
PF7/SPISEL7	D, BT, PD	General-Purpose IO7/SPI Slave Select Output 7
PF6/SPISEL6	D, BT, PD	General-Purpose IO6/SPI Slave Select Output 6
PF5/SPISEL5	D, BT, PD	General-Purpose IO5/SPI Slave Select Output 5
PF4/SPISEL4	D, BT, PD	General-Purpose IO4/SPI Slave Select Output 4
PF3/SPISEL3	D, BT, PD	General-Purpose IO3/SPI Slave Select Output 3
PF2/SPISEL2	D, BT, PD	General-Purpose IO2/SPI Slave Select Output 2
PF1/SPISEL1	D, BT, PD	General-Purpose IO1/SPI Slave Select Output 1
PF0/$\overline{\text{SPISS}}$	D, BT, PD	General-Purpose IO0/SPI Slave Select Input 0
SCK	D, BT	SPI Clock
MISO	D, BT	SPI Master In Slave Out Data
MOSI	D, BT	SPI Master Out Slave In Data
DT	D, OT	SPORT Data Transmit
DR	D, I	SPORT Data Receive
RFS	D, BT	SPORT Receive Frame Sync
TFS	D, BT	SPORT Transmit Frame Sync
TCLK	D, BT	SPORT Transmit Clock
RCLK	D, BT	SPORT Receive Clock
EIA	D, I	Encoder A Channel Input
EIB	D, I	Encoder B Channel Input
EIZ	D, I	Encoder Z Channel Input
EIS	D, I	Encoder S Channel Input
AUX0	D, O	Auxiliary PWM Channel 0 Output
AUX1	D, O	Auxiliary PWM Channel 1 Output
$\overline{\text{AUXTRIP}}$	D, I, PD	Auxiliary PWM Shutdown Pin
TMR2	D, BT	Timer 0 Input/Output Pin
TMR1	D, BT	Timer 1 Input/Output Pin
TMR0	D, BT	Timer 2 Input/Output Pin
AH	D, O	PWM Channel A HI PWM
AL	D, O	PWM Channel A LO PWM
BH	D, O	PWM Channel B HI PWM
BL	D, O	PWM Channel B LO PWM
CH	D, O	PWM Channel C HI PWM
CL	D, O	PWM Channel C LO PWM

Table 7. Recommended Operating Conditions—ADSP-21992BST

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		160	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		80	MHz
CLKIN[3]	Input Clock Frequency	0		160	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+85	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK÷2, up to a maximum of a 80 MHz HCLK for the ADSP-21992BST.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 8. Recommended Operating Conditions—ADSP-21992YST

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		100	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		50	MHz
CLKIN[3]	Input Clock Frequency	0		100	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+125	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK÷2, up to a maximum of an 50 MHz HCLK for the ADSP-21992YST.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 14. Peripherals Electrical Characteristics—ADSP-21992BST

Parameter	Description	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER					
AC Specifications					
SNR	Signal-to-Noise Ratio[1]	68	72		dB
SNRD	Signal-to-Noise and Distortion[1]	68	71		dB
THD	Total Harmonic Distortion[1]		–78	–68	dB
CTLK	Channel-Channel Crosstalk[1]		–80	–66	dB
CMRR	Common-Mode Rejection Ratio[1]		–74	–66	dB
PSRR	Power Supply Rejection Ratio[1]		0.05	0.2	%FSR
Accuracy					
INL	Integral Nonlinearity[1]		±0.6	±2.0	LSB
DNL	Differential Nonlinearity[1]		±0.5	±1.25	LSB
No Missing Codes			12		Bits
Zero Error[1]			1.25	2.5	%FSR
Gain Error[1]			0.5	1.5	%FSR
Input Voltage					
V_{IN}	Input Voltage Span		2.0		V
C_{IN}	Input Capacitance[2]		10		pF
Conversion Time					
FCLK	ADC Clock Rate			20	MHz
t_{CONV}	Total Conversion Time All 8 Channels			725	ns
VOLTAGE REFERENCE					
Internal Voltage Reference[3]		0.94	0.98	1.02	V
Output Voltage Tolerance			40		mV
Output Current			100		μA
Load Regulation[4]		–2	+0.5	+2	mV
Power Supply Rejection Ratio		–2	+0.5	+2	mV
Reference Input Resistance			8		kΩ
POWER-ON RESET					
V_{RST}	Reset Threshold Voltage	1.4		2.1	V
V_{HYST}	Hysteresis Voltage		50		mV

[1] In all cases, the input frequency to the ADC system is assumed to be <100 kHz.
[2] Analog input pins VIN0 to VIN7.
[3] These specifications are for operation of the internal voltage reference so that SENSE = REFCOM, with the default 1.0 V operating mode.
[4] Operation with full 0.1 mA load current. For optimal operation, it is recommended to buffer the VREF output voltage before using it in other parts of the system.

Table 15. Peripherals Electrical Characteristics—ADSP-21992YBC

Parameter	Description	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER					
AC Specifications					
SNR	Signal-to-Noise Ratio[1]	68	72		dB
SNRD	Signal-to-Noise and Distortion[1]	66	71		dB
THD	Total Harmonic Distortion[1]		–80	–66	dB
CTLK	Channel-Channel Crosstalk[1]		–80	–66	dB
CMRR	Common-Mode Rejection Ratio[1]		–82	–66	dB
PSRR	Power Supply Rejection Ratio[1]		0.05	0.2	%FSR
Accuracy					
INL	Integral Nonlinearity[1]		±0.6	±2.0	LSB
DNL	Differential Nonlinearity[1]		±0.5	±1.25	LSB
No Missing Codes			12		Bits
Zero Error[1]			1.25	2.5	%FSR
Gain Error[1]			0.5	1.5	%FSR
Input Voltage					
V_{IN}	Input Voltage Span		2.0		V
C_{IN}	Input Capacitance[2]		10		pF
Conversion Time					
FCLK	ADC Clock Rate			18.75	MHz
t_{CONV}	Total Conversion Time All 8 Channels			773	ns
VOLTAGE REFERENCE					
Internal Voltage Reference[3]		0.94	0.98	1.02	V
Output Voltage Tolerance			40		mV
Output Current			100		µA
Load Regulation[4]		–2	+0.5	+2	mV
Power Supply Rejection Ratio		–2	+0.5	+2	mV
Reference Input Resistance			8		kΩ
POWER-ON RESET					
V_{RST}	Reset Threshold Voltage	1.4		2.1	V
V_{HYST}	Hysteresis Voltage		50		mV

[1] In all cases, the input frequency to the ADC system is assumed to be <100 kHz.
[2] Analog input pins VIN0 to VIN7.
[3] These specifications are for operation of the internal voltage reference so that SENSE = REFCOM, with the default 1.0 V operating mode.
[4] Operation with full 0.1 mA load current. For optimal operation, it is recommended to buffer the VREF output voltage before using it in other parts of the system.

Table 16. Peripherals Electrical Characteristics—ADSP-21992YST

Parameter	Description	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER					
AC Specifications					
SNR	Signal-to-Noise Ratio[1]	68	72		dB
SNRD	Signal-to-Noise and Distortion[1]	68	71		dB
THD	Total Harmonic Distortion[1]		–80	–68	dB
CTLK	Channel-Channel Crosstalk[1]		–80	–66	dB
CMRR	Common-Mode Rejection Ratio[1]		–82	–66	dB
PSRR	Power Supply Rejection Ratio[1]		0.05	0.2	%FSR
Accuracy					
INL	Integral Nonlinearity[1]		±0.6	±2.0	LSB
DNL	Differential Nonlinearity[1]		±0.5	±1.25	LSB
No Missing Codes			12		Bits
Zero Error[1]			1.25	2.5	%FSR
Gain Error[1]			0.5	1.5	%FSR
Input Voltage					
V_{IN}	Input Voltage Span		2.0		V
C_{IN}	Input Capacitance[2]		10		pF
Conversion Time					
FCLK	ADC Clock Rate			12.5	MHz
t_{CONV}	Total Conversion Time All 8 Channels			1160	ns
VOLTAGE REFERENCE					
Internal Voltage Reference[3]		0.94	0.98	1.02	V
Output Voltage Tolerance			40		mV
Output Current			100		µA
Load Regulation[4]		–2	+0.5	+2	mV
Power Supply Rejection Ratio		–2	+0.5	+2	mV
Reference Input Resistance			8		kΩ
POWER-ON RESET					
V_{RST}	Reset Threshold Voltage	1.4		2.1	V
V_{HYST}	Hysteresis Voltage		50		mV

[1] In all cases, the input frequency to the ADC system is assumed to be <100 kHz.
[2] Analog input pins VIN0 to VIN7.
[3] These specifications are for operation of the internal voltage reference so that SENSE = REFCOM, with the default 1.0 V operating mode.
[4] Operation with full 0.1 mA load current. For optimal operation, it is recommended to buffer the VREF output voltage before using it in other parts of the system.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Internal (Core) Supply Voltage[1] (V_{DDINT})	–0.3 V to +3.0 V
External (I/O) Supply Voltage[1] (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage1, [2] (V_{IL} – V_{IH})	–0.5 V to +5.5 V
Output Voltage Swing[1, 2] (V_{OL} – V_{OH})	–0.5 V to +5.5 V
Load Capacitance1 (C_L)	200 pF
Core Clock Period1 (t_{CCLK})	6.25 ns
Core Clock Frequency1 (f_{CCLK})	160 MHz
Peripheral Clock Period1 (t_{HCLK})	12.5 ns
Peripheral Clock Frequency1 (f_{HCLK})	80 MHz
Storage Temperature Range1 (T_{STORE})	–65°C to +150°C
Lead Temperature (5 seconds)1 (T_{LEAD})	85°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Except CLKIN and analog pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

This next section contains timing information for the external signals of the DSP. Use the exact information given. Do not attempt to derive parameters from the addition or subtraction of other information. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added meaningfully to derive longer times.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Switching characteristics specify how the processor changes its signals. No control is possible over this timing; circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics indicate what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timer PWM_OUT Cycle Timing

Table 19 and Figure 9 describe timer expired operations. The input signal is asynchronous in "width capture mode" and has an absolute maximum input frequency of 40 MHz.

Table 19. Timer PWM_OUT Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output[1]	12.5	$(2^{32}-1)$ cycles	ns

[1] The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}-1)$ cycles.

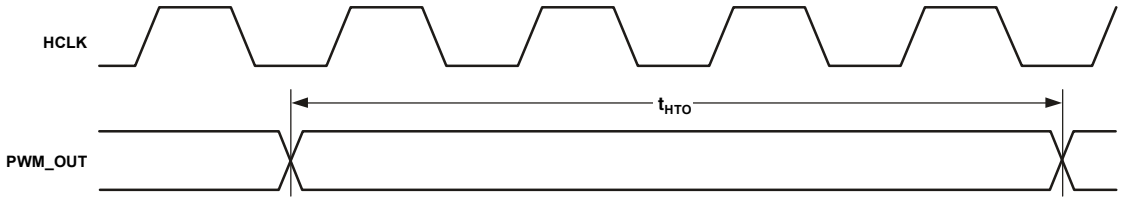

Figure 9. Timer PWM_OUT Cycle Timing

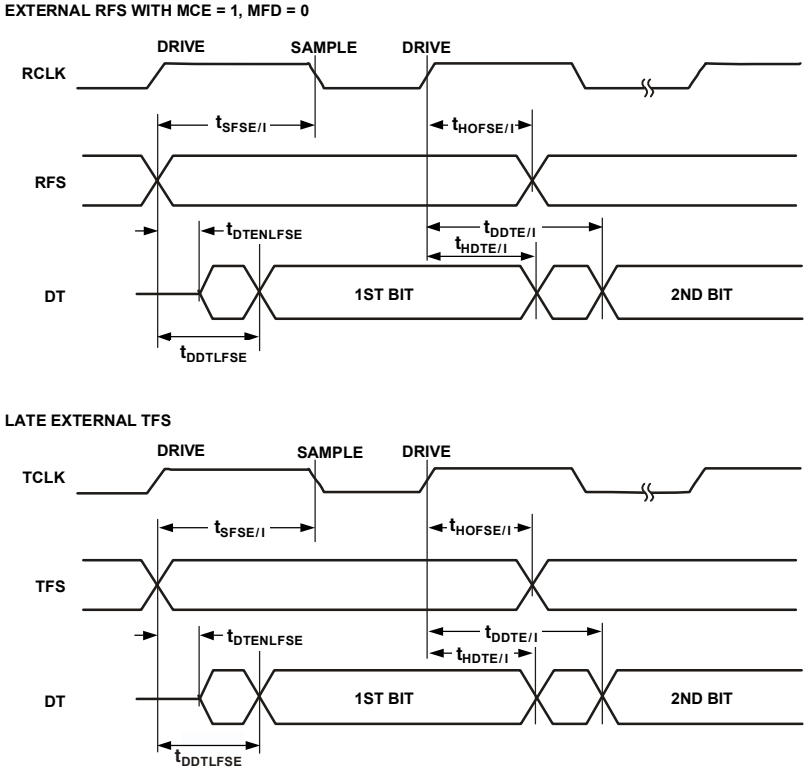

Figure 15. Serial Port—External Late Frame Sync (Frame Sync Setup < $0.5t_{HCLK}$)

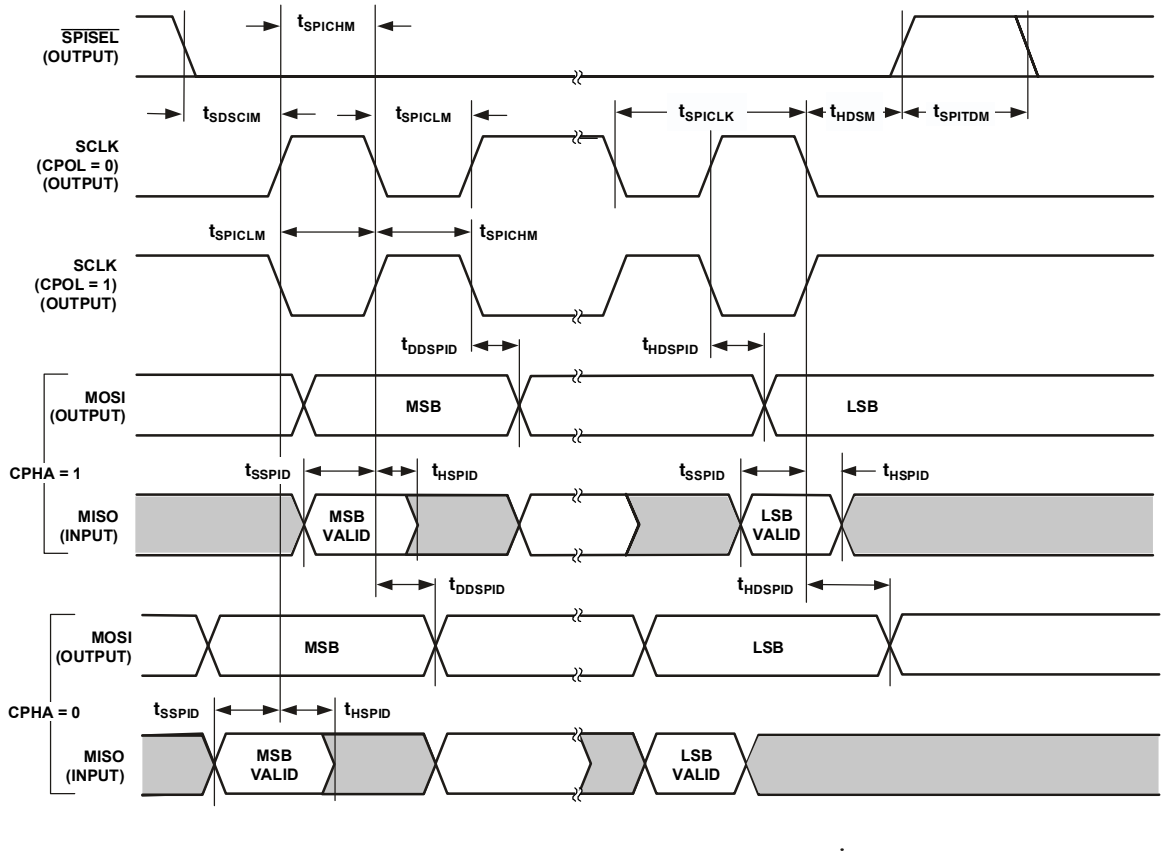

Figure 16. Serial Peripheral Interface (SPI) Port—Master Timing

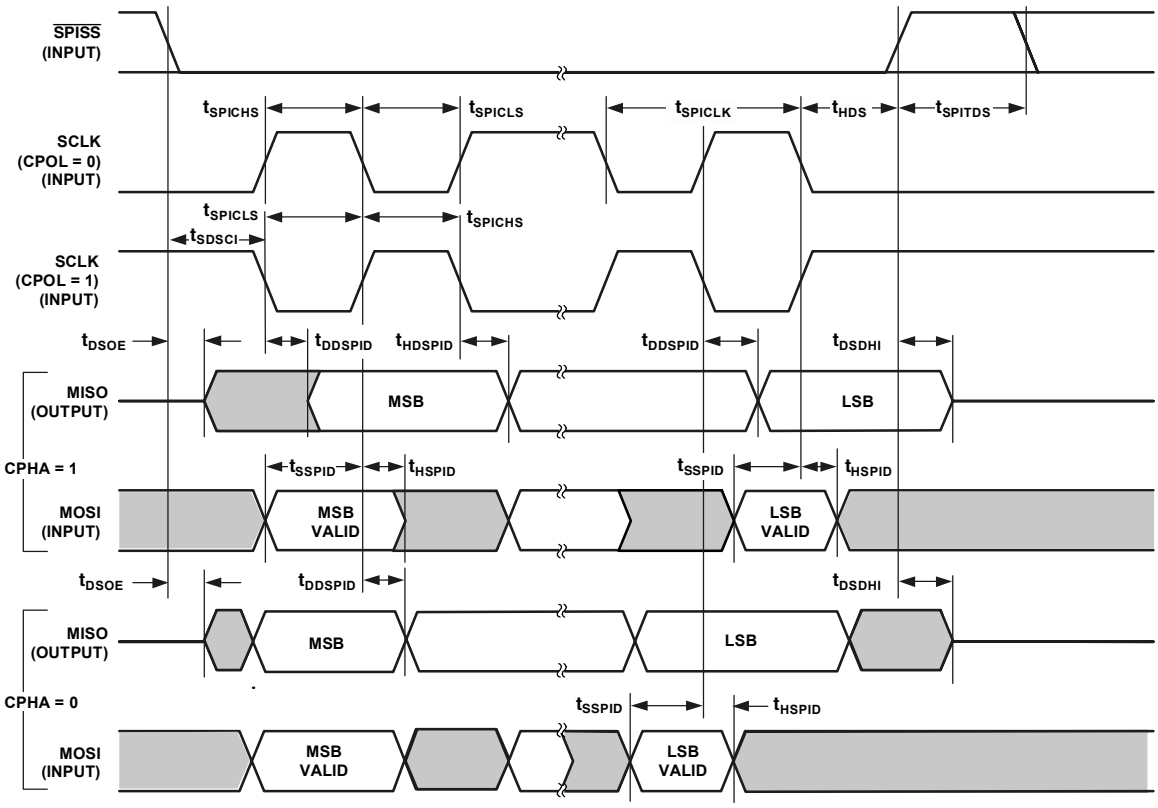

Figure 17. Serial Peripheral Interface (SPI) Port—Slave Timing

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by the formula below.

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance includes the package capacitance (C_{IN} of the processor). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle. For example, estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory—asynchronous RAM (16-bit)
- One 64K × 16 RAM chip is used with a load of 10 pF
- Maximum peripheral speed CCLK = 80 MHz, HCLK = 80 MHz
- External data memory writes occur every other cycle, a rate of $1/(4t_{HCLK})$, with 50% of the pins switching
- The bus cycle time is 80 MHz (t_{HCLK} = 12.5 ns)

The P_{EXT} equation is calculated for each class of pins that can drive as shown in Table 27.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation with the following formula.

$$P_{TOTAL} = P_{EXT} + P_{INT}$$

where:

P_{EXT} is from Table 27.

P_{INT} is I_{DDINT} × 2.5 V, using the calculation I_{DDINT} listed in Power Dissipation.

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 27. P_{EXT} Calculation Example

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	10 pF	20 MHz	10.9 V	= 0.01635 W
$\overline{MSx}$	1	0	10 pF	20 MHz	10.9 V	= 0.0 W
$\overline{WR}$	1		10 pF	40 MHz	10.9 V	= 0.00436 W
Data	16	50	10 pF	20 MHz	10.9 V	= 0.01744 W
CLKOUT	1		10 pF	80 MHz	10.9 V	= 0.00872 W = 0.04687 W

PIN CONFIGURATIONS

Table 28 identifies the signal for each CSP_BGA ball number. Table 29 identifies the CSP_BGA ball number for each signal name. Table 30 identifies the signal for each LQFP lead. Table 31 identifies the LQFP lead for each signal name. Table 4 on Page 17 describes each signal.

Table 28. 196-Ball CSP_BGA Signal by Ball Number

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	nc	D8	AVSS	H1	A10	L8	VDDINT
A2	DR	D9	PF3/SPISEL3	H2	A11	L9	VDDEXT
A3	DT	D10	$\overline{\text{AUXTRIP}}$	H3	$\overline{\text{MS3}}$	L10	VDDEXT
A4	RFS	D11	VDDEXT	H4	GND	L11	GND
A5	VIN4	D12	AUX1	H5	nc	L12	BMODE2
A6	BSHAN	D13	AUX0	H6	nc	L13	BMODE1
A7	VIN0	D14	PF15	H7	nc	L14	CLKIN
A8	VIN1	E1	A16	H8	nc	M1	A2
A9	VIN3	E2	A17	H9	nc	M2	A3
A10	PF0/$\overline{\text{SPISS}}$	E3	$\overline{\text{WR}}$	H10	nc	M3	$\overline{\text{MS2}}$
A11	PF4/SPISEL4	E4	GND	H11	VDDEXT	M4	GND
A12	PF6/SPISEL6	E5	VDDEXT	H12	TMR0	M5	VDDEXT
A13	PF7/SPISEL7	E6	nc	H13	$\overline{\text{POR}}$	M6	GND
A14	nc	E7	nc	H14	$\overline{\text{RESET}}$	M7	VDDEXT
B1	SCK	E8	nc	J1	A8	M8	CANRX
B2	RCLK	E9	nc	J2	A9	M9	CL
B3	TCLK	E10	nc	J3	$\overline{\text{BMS}}$	M10	AL
B4	TFS	E11	GND	J4	VDDEXT	M11	PWMPOL
B5	VIN6	E12	EIA	J5	nc	M12	$\overline{\text{PWMTRIP}}$
B6	ASHAN	E13	EIB	J6	nc	M13	BYPASS
B7	VIN2	E14	EIS	J7	nc	M14	BMODE0
B8	SENSE	F1	A14	J8	nc	N1	A0
B9	CAPB	F2	A15	J9	nc	N2	A1
B10	PF1/SPISEL1	F3	$\overline{\text{BG}}$	J10	nc	N3	D13
B11	PF5/SPISEL5	F4	GND	J11	GND	N4	D11
B12	PF8	F5	nc	J12	TMS	N5	D9
B13	PF9	F6	nc	J13	TCK	N6	D7
B14	PF13	F7	nc	J14	TDI	N7	D5
C1	$\overline{\text{BR}}$	F8	nc	K1	A6	N8	D3
C2	$\overline{\text{RD}}$	F9	nc	K2	A7	N9	D1
C3	MISO	F10	nc	K3	$\overline{\text{MS0}}$	N10	CH
C4	MOSI	F11	VDDINT	K4	GND	N11	AH
C5	VIN7	F12	EIZ	K5	GND	N12	nc
C6	VIN5	F13	TMR2	K6	GND	N13	PWMSYNC
C7	CAPT	F14	XTAL	K7	GND	N14	$\overline{\text{PWMSR}}$
C8	VREF	G1	A12	K8	GND	P1	nc
C9	CML	G2	A13	K9	GND	P2	D15
C10	PF2/SPISEL2	G3	$\overline{\text{BGH}}$	K10	GND	P3	D14
C11	PF10	G4	VDDINT	K11	VDDINT	P4	D12
C12	PF11	G5	nc	K12	$\overline{\text{EMU}}$	P5	D10
C13	PF12	G6	nc	K13	$\overline{\text{TRST}}$	P6	D8
C14	PF14	G7	nc	K14	TDO	P7	D6
D1	A18	G8	nc	L1	A4	P8	D4
D2	A19	G9	nc	L2	A5	P9	D2
D3	$\overline{\text{IOMS}}$	G10	nc	L3	$\overline{\text{MS1}}$	P10	D0
D4	ACK	G11	GND	L4	VDDEXT	P11	BL
D5	AVDD	G12	TMR1	L5	VDDINT	P12	BH
D6	AVDD	G13	CONVST	L6	VDDEXT	P13	CANTX
D7	AVSS	G14	CLKOUT	L7	VDDINT	P14	nc

Table 31. 176-Lead LQFP Lead Number by Signal

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
A0	50	CAPB	156	EIS	116	$\overline{\text{PWMTRIP}}$	87
A1	49	CAPT	155	EIZ	119	RCLK	4
A10	35	CH	77	$\overline{\text{EMU}}$	99	$\overline{\text{RD}}$	8
A11	34	CL	76	$\overline{\text{IOMS}}$	14	$\overline{\text{RESET}}$	106
A12	33	CLKIN	107	MISO	6	RFS	172
A13	30	CLKOUT	109	MOSI	7	SCK	5
A14	29	CML	154	$\overline{\text{MS0}}$	21	SENSE	157
A15	28	CONVST	110	$\overline{\text{MS1}}$	20	TCK	104
A16	27	D0	72	$\overline{\text{MS2}}$	19	TCLK	174
A17	26	D1	71	$\overline{\text{MS3}}$	16	TDI	102
A18	25	D10	60	nc	1	TDO	101
A19	24	D11	55	nc	2	TFS	173
A2	48	D12	54	nc	42	TMR0	111
A3	47	D13	53	nc	43	TMR1	114
A4	46	D14	52	nc	44	TMR2	115
A5	40	D15	51	nc	83	TMS	103
A6	39	D2	70	nc	89	$\overline{\text{TRST}}$	100
A7	38	D3	69	nc	90	VDDEXT	3
A8	37	D4	68	nc	96	VDDEXT	18
A9	36	D5	65	nc	130	VDDEXT	32
ACK	10	D6	64	nc	131	VDDEXT	45
AH	81	D7	63	nc	132	VDDEXT	57
AL	80	D8	62	nc	152	VDDEXT	75
ASHAN	162	D9	61	nc	176	VDDEXT	91
AUX0	124	GND	17	PF0/$\overline{\text{SPISS}}$	147	VDDEXT	113
AUX1	123	GND	22	PF1/SPISEL1	146	VDDEXT	133
$\overline{\text{AUXTRIP}}$	122	GND	31	PF10	135	VDDEXT	143
AVDD	151	GND	41	PF11	134	VDDINT	23
AVDD	169	GND	56	PF12	128	VDDINT	59
AVSS	150	GND	58	PF13	127	VDDINT	67
AVSS	168	GND	66	PF14	126	VDDINT	98
$\overline{\text{BG}}$	12	GND	74	PF15	125	VDDINT	118
$\overline{\text{BGH}}$	13	GND	88	PF2/SPISEL2	145	VDDINT	149
BH	79	GND	97	PF3/SPISEL3	144	VIN0	161
BL	78	GND	112	PF4/SPISEL4	141	VIN1	160
BMODE0	93	GND	117	PF5/SPISEL5	140	VIN2	159
BMODE1	94	GND	129	PF6/SPISEL6	139	VIN3	158
BMODE2	95	GND	142	PF7/SPISEL7	138	VIN4	164
$\overline{\text{BMS}}$	15	GND	148	PF8	137	VIN5	165
$\overline{\text{BR}}$	11	GND	175	PF9	136	VIN6	166
BSHAN	163	DR	171	$\overline{\text{POR}}$	105	VIN7	167
BYPASS	92	DT	170	PWMPOL	85	VREF	153
CANRX	73	EIA	121	$\overline{\text{PWMSR}}$	86	$\overline{\text{WR}}$	9
CANTX	82	EIB	120	PWMSYNC	84	XTAL	108