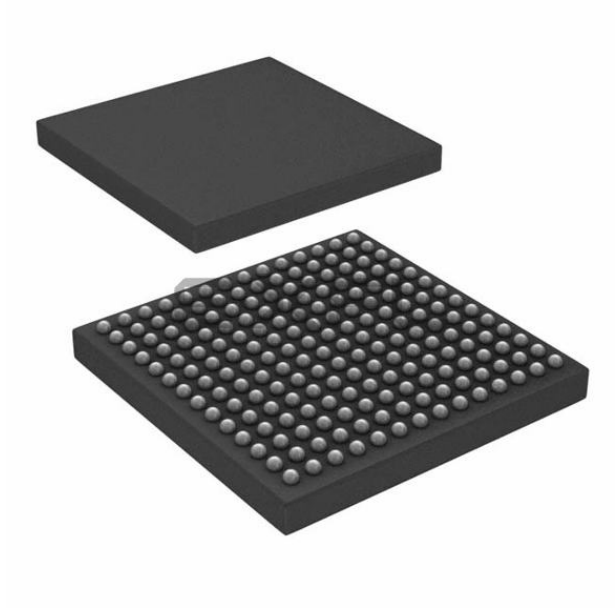

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	SPI, SSP
Clock Rate	150MHz
Non-Volatile Memory	External
On-Chip RAM	128kB
Voltage - I/O	3.30V
Voltage - Core	2.50V
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	196-BGA, CSPBGA
Supplier Device Package	196-MBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-21992ybc

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REVISION HISTORY

8/07—Rev. 0 to Rev. A

Added RoHS part number to Ordering Guide 59

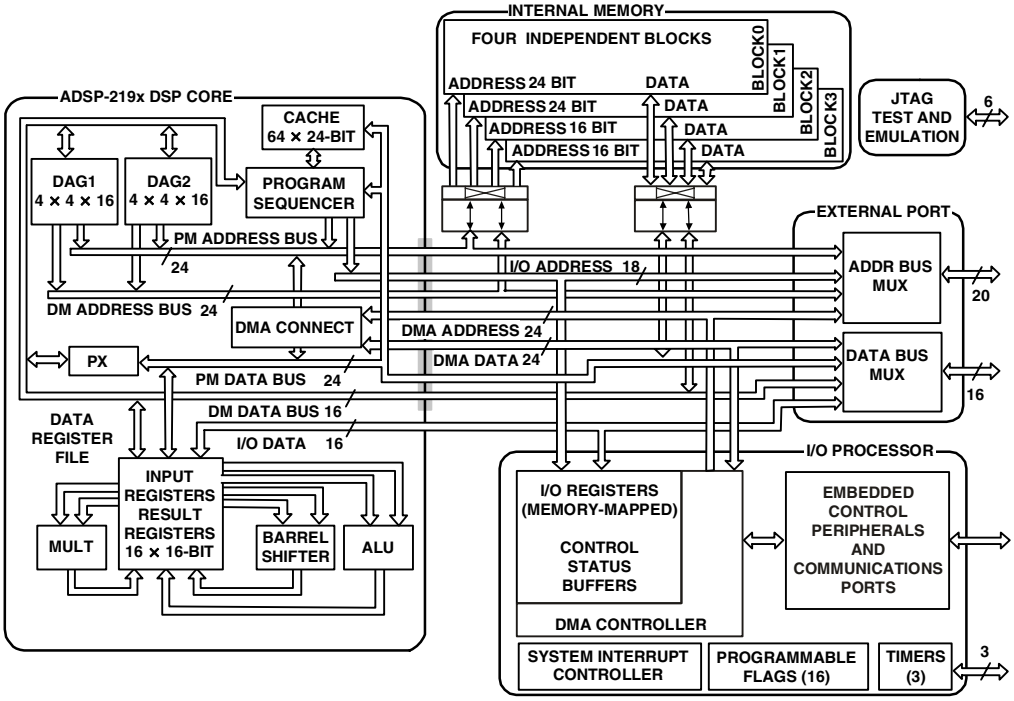


Figure 2. Block Diagram

an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

The block diagram (Figure 2) shows the architecture of the embedded SHARC core. It contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data from the register file and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single cycle multiply, multiply/add, and multiply/subtract operations. The MAC has two 40-bit accumulators, which help with overflow. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control, including multiword and block floating-point representations.

Register usage rules influence placement of input and results within the computational units. For most operations, the data registers of the computational units act as a data register file, permitting any input or result register to provide input to any unit for a computation. For feedback operations, the computational units let the output (result) of any unit be input to any unit on the next cycle. For conditional or multifunction instructions, there are restrictions on which data registers may provide inputs or receive results from each computational unit. For more information, see the *ADSP-2199x DSP Instruction Set Reference*.

A powerful program sequencer controls the flow of instruction execution. The sequencer supports conditional jumps, subroutine calls, and low interrupt overhead. With internal loop counters and loop stacks, the ADSP-21992 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four 16-bit address pointers. Whenever the pointer is used to access data (indirect addressing), it is pre- or post-modified by the value of one of four possible modify registers. A length value and base address may be associated with each pointer to implement automatic modulo addressing for circular buffers. Page registers in the DAGs allow circular addressing within 64K word boundaries of each of the 256 memory pages, but these buffers may not cross page boundaries. Secondary registers duplicate all the primary registers in the DAGs; switching between primary and secondary registers provides a fast context switch.

Efficient data transfer in the core is achieved with the use of internal buses:

- Program memory address (PMA) bus
- Program memory data (PMD) bus
- Data memory address (DMA) bus
- Data memory data (DMD) bus
- Direct memory access address bus
- Direct memory access data bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Boot memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-21992 to fetch two operands in a single cycle, one from program memory and one from data memory. The DSP dual memory buses also let the embedded SHARC core fetch an operand from data memory and the next instruction from program memory in a single cycle.

MEMORY ARCHITECTURE

The ADSP-21992 provides 48K words of on-chip SRAM memory. This memory is divided into three blocks: two 16K × 24-bit blocks (Blocks 0 and 1) and one 16K × 16-bit block (Block 2). In addition, the ADSP-21992 provides a 4K × 24-bit block of program memory boot ROM (that is reserved by ADI for boot load routines). The memory map of the ADSP-21992 is illustrated in Figure 2.

As shown in Figure 2, the three internal memory RAM blocks reside in memory page 0. The entire DSP memory map consists of 256 pages (Pages 0 to 255), and each page is 64K words long. External memory space consists of four memory banks (Banks3–0) and supports a wide variety of memory devices. Each bank is selectable using unique memory select lines ($\overline{MS3–0}$) and has configurable page boundaries, wait states, and wait state modes. The 4K words of on-chip boot ROM populates the top of Page 255, while the remaining 254 pages are addressable off-chip. I/O memory pages differ from external memory in that they are 1K word long, and the external I/O pages have their own select pin ($\overline{IOMS}$). Pages 31–0 of I/O memory space reside on-chip and contain the configuration registers for the peripherals. Both the ADSP-2199x core and DMA capable peripherals can access the entire memory map of the DSP.

NOTE: The physical external memory addresses are limited by 20 address lines, and are determined by the external data width and packing of the external memory space. The Strobe signals ($\overline{MS3-0}$) can be programmed to allow the user to change starting page addresses at runtime.

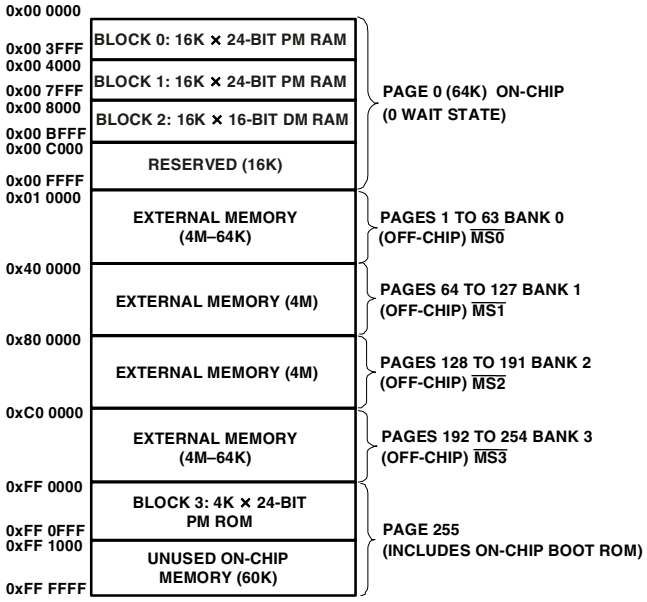


Figure 3. Core Memory Map at Reset

Internal (On-Chip) Memory

The unified program and data memory space of the ADSP-21992 consists of 16M locations that are accessible through two 24-bit address buses, the PMA, and DMA buses. The DSP uses slightly different mechanisms to generate a 24-bit address for each bus. The DSP has three functions that support access to the full memory map.

- The DAGs generate 24-bit addresses for data fetches from the entire DSP memory address range. Because DAG index (address) registers are 16 bits wide and hold the lower 16 bits of the address, each of the DAGs has its own 8-bit page register (DMPGx) to hold the most significant eight address bits. Before a DAG generates an address, the program must set the DAG DMPGx register to the appropriate memory page. The DMPG1 register is also used as a page register when accessing external memory. The program must set DMPG1 accordingly, when accessing data variables in external memory. A "C" program macro is provided for setting this register.
- The program sequencer generates the addresses for instruction fetches. For relative addressing instructions, the program sequencer bases addresses for relative jumps, calls, and loops on the 24-bit program counter (PC). In direct addressing instructions (two word instructions), the instruction provides an immediate 24-bit address value. The PC allows linear addressing of the full 24-bit address range.
- For indirect jumps and calls that use a 16-bit DAG address register for part of the branch address, the program sequencer relies on an 8-bit indirect jump page (IJPG)

from an external source using the $\overline{\text{RESET}}$ signal, or alternatively, the internal power-on reset circuit may be used by connecting the $\overline{\text{POR}}$ pin to the $\overline{\text{RESET}}$ pin. During power-up the $\overline{\text{RESET}}$ line must be activated for long enough to allow the DSP core's internal clock to stabilize. The power-up sequence is defined as the total time required for the crystal oscillator to stabilize after a valid VDD is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 512 cycles will ensure that the PLL has locked (this does not include the crystal oscillator start-up time).

The $\overline{\text{RESET}}$ input contains some hysteresis. If an RC circuit is used to generate the $\overline{\text{RESET}}$ signal, the circuit should use an external Schmitt trigger.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts, and resets all registers to their default values (where applicable). When $\overline{\text{RESET}}$ is released, if there is no pending bus request, program control jumps to the location of the on-chip boot ROM (0xFF0000) and the booting sequence is performed.

POWER SUPPLIES

The ADSP-21992 has separate power supply connections for the internal (V_{DDINT}) and external (V_{DDEXT}) power supplies. The internal supply must meet the 2.5 V requirement. The external supply must be connected to a 3.3 V supply. All external supply pins must be connected to the same supply. The ideal power-on sequence for the DSP is to provide power-up of all supplies simultaneously. If there is going to be some delay in power-up between the supplies, provide V_{DD} first, then V_{DD_IO}.

BOOTING MODES

The ADSP-21992 supports a number of different boot modes that are controlled by the three dedicated hardware boot mode control pins (BMODE2, BMODE1, and BMODE0). The use of three boot mode control pins means that up to eight different boot modes are possible. Of these only five modes are valid on the ADSP-21992. The ADSP-21992 exposes the boot mechanism to software control by providing a nonmaskable boot interrupt that vectors to the start of the on-chip ROM memory block (at address 0xFF0000). A boot interrupt is automatically initiated following either a hardware initiated reset, via the $\overline{\text{RESET}}$ pin, or a software initiated reset, via writing to the software reset register. Following either a hardware or a software reset, execution always starts from the boot ROM at address 0xFF0000, irrespective of the settings of the BMODE2, BMODE1, and BMODE0 pins. The dedicated BMODE2, BMODE1, and BMODE0 pins are sampled at hardware reset.

The particular boot mode for the ADSP-21992 associated with the settings of the BMODE2, BMODE1, BMODE0 pins is defined in Table 3.

Table 3. Summary of Boot Modes

Boot Mode	BMODE2	BMODE1	BMODE0	Function
0	0	0	0	Illegal–Reserved
1	0	0	1	Boot from External 8-Bit Memory over EMI
2	0	1	0	Execute from External 8-Bit Memory
3	0	1	1	Execute from External 16-Bit Memory
4	1	0	0	Boot from SPI ≤ 4K Bits
5	1	0	1	Boot from SPI > 4K Bits
6	1	1	0	Illegal–Reserved
7	1	1	1	Illegal–Reserved

SPECIFICATIONS

Specifications subject to change without notice.

OPERATING CONDITIONS

Table 5. Recommended Operating Conditions—ADSP-21992BBC

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		150	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		75	MHz
CLKIN[3]	Input Clock Frequency	0		150	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+85	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK÷2, up to a maximum of a 75 MHz HCLK for the ADSP-21992BBC.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 6. Recommended Operating Conditions—ADSP-21992YBC

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		150	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		75	MHz
CLKIN[3]	Input Clock Frequency	0		150	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+125	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK ÷ 2, up to a maximum of an 75 MHz HCLK for the ADSP-21992YBC.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 7. Recommended Operating Conditions—ADSP-21992BST

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		160	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		80	MHz
CLKIN[3]	Input Clock Frequency	0		160	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+85	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK÷2, up to a maximum of a 80 MHz HCLK for the ADSP-21992BST.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 8. Recommended Operating Conditions—ADSP-21992YST

Parameter	Conditions	Min	Typ	Max	Unit
V_{DDINT}	Internal (Core) Supply Voltage	2.375	2.5	2.625	V
V_{DDEXT}	External (I/O) Supply Voltage	3.135	3.3	3.465	V
AVDD	Analog Supply Voltage	2.375	2.5	2.625	V
CCLK	DSP Instruction Rate, Core Clock	0		100	MHz
HCLK[1, 2]	Peripheral Clock Rate	0		50	MHz
CLKIN[3]	Input Clock Frequency	0		100	MHz
T_{JUNC}[4]	Silicon Junction Temperature			140	°C
T_{AMB}	Ambient Operating Temperature	–40		+125	°C

[1] The HCLK frequency may be made to appear at the dedicated CLKOUT pin of the device. For low power operation, however, the CLKOUT pin can be disabled.
[2] The peripherals operate at the HCLK rate, which may be selected to be equal to CCLK or CCLK÷2, up to a maximum of an 50 MHz HCLK for the ADSP-21992YST.
[3] In order to attain the correct CCLK and HCLK values, the input clock frequency or crystal frequency depends on the internal operation of the clock generation PLL circuit and the associated frequency ratio.
[4] The maximum junction temperature is limited to 140°C in order to meet all of the electrical specifications. It is ultimately the responsibility of the user to ensure that the power dissipation of the ADSP-21992 (including all dc and ac loads) is such that the maximum junction temperature limit of 140°C is not exceeded.

Table 9. Electrical Characteristics—ADSP-21992BBC

Parameter	Conditions	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage[1]	@ V_{DDEXT} = Maximum	2.0		V_{DDEXT}	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Maximum	2.2		V_{DDEXT}	V
V_{IL}	High Level Input Voltage[1, 2]	@ V_{DDEXT} = Minimum			0.8	V
V_{OH}	High Level Output Voltage[3]	@ V_{DDEXT} = Minimum, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage[3]	@ V_{DDEXT} = Minimum, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[4]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{IH}	High Level Input Current[5]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			150	µA
I_{IH}	High Level Input Current[6]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			150	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
C_I	Input Pin Capacitance	f_{IN} = 1 MHz		10		pF
C_O	Output Pin Capacitance	f_{IN} = 1 MHz		10		pF
$I_{DD-PEAK}$	Supply Current (Internal)[8, 9]			190	325	mA
I_{DD-TYP}	Supply Current (Internal)[8]			155	275	mA
$I_{DD-IDLE}$	Supply Current (Idle)[8]			145	250	mA
$I_{DD-STOPCLK}$	Supply Current (Power-Down)[8, 10]			60	125	mA
$I_{DD-STOPALL}$	Supply Current (Power-Down)[8, 11]			12	40	mA
$I_{DD-PDOWN}$	Supply Current (Power-Down)[8, 12]			6	30	mA
I_{AVDD}	Analog Supply Current[13]			46	65	mA
$I_{AVDD-ADCOFF}$	Analog Supply Current[12]			5	15	mA

[1] Applies to all input and bidirectional pins.
[2] Applies to input pins CLKIN, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.
[3] Applies to all output and bidirectional pins.
[4] Applies to all input only pins.
[5] Applies to input pins with internal pull-down.
[6] Applies to input pins with internal pull-up.
[7] Applies to three-stateable pins.
[8] The I_{DD} supply currents are affected by the operating frequency of the device. The guaranteed numbers are based on an assumed CCLK = 150 MHz, HCLK = 75 MHz for the ADSP-21992BBC. I_{DD} refers only to the current consumption on the internal power supply lines (V_{DDINT}). The current consumption at the I/O on the V_{DDEXT} power supply is very much dependent on the particular connection of the device in the final system.
[9] $I_{DD-PEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. Measured at V_{DDINT} = maximum.
[10] IDLE denotes the current consumption during execution of the IDLE instruction. Measured at V_{DDINT} = maximum.
[11] $I_{DD-PDOWN}$ represents the processor operation in full power-down mode with both core and peripheral clocks disabled. Measured at V_{DDINT} = maximum.
[12] I_{AVDD} represents the power consumption of the analog system. Measured at AVDD = maximum.
[13] The responsibility lies with the user to ensure that the device is operated in such a manner that the maximum allowable junction temperature is not exceeded.

Table 11. Electrical Characteristics—ADSP-21992BST

Parameter	Conditions	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High Level Input Voltage[1]	@ V_{DDEXT} = Maximum	2.0		V_{DDEXT}	V
V_{IH}	High Level Input Voltage[2]	@ V_{DDEXT} = Maximum	2.2		V_{DDEXT}	V
V_{IL}	High Level Input Voltage[1, 2]	@ V_{DDEXT} = Minimum			0.8	V
V_{OH}	High Level Output Voltage[3]	@ V_{DDEXT} = Minimum, I_{OH} = –0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage[3]	@ V_{DDEXT} = Minimum, I_{OL} = 2.0 mA			0.4	V
I_{IH}	High Level Input Current[4]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{IH}	High Level Input Current[5]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			150	µA
I_{IH}	High Level Input Current[6]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
I_{IL}	Low Level Input Current	@ V_{DDINT} = Maximum, V_{IN} = 0 V			150	µA
I_{OZH}	Three-State Leakage Current[7]	@ V_{DDINT} = Maximum, V_{IN} = 3.6 V			10	µA
I_{OZL}	Three-State Leakage Current[7]	@ V_{DDINT} = Maximum, V_{IN} = 0 V			10	µA
C_I	Input Pin Capacitance	f_{IN} = 1 MHz		10		pF
C_O	Output Pin Capacitance	f_{IN} = 1 MHz		10		pF
$I_{DD-PEAK}$	Supply Current (Internal)[8, 9]			300	350	mA
I_{DD-TYP}	Supply Current (Internal)[8]			240	300	mA
$I_{DD-IDLE}$	Supply Current (Idle)[8]			225	275	mA
$I_{DD-STOPCLK}$	Supply Current (Power-Down)[8, 10]			90	150	mA
$I_{DD-STOPALL}$	Supply Current (Power-Down)[8, 11]			20	50	mA
$I_{DD-PDOWN}$	Supply Current (Power-Down)[8, 12]			7	35	mA
I_{AVDD}	Analog Supply Current[13]			49	65	mA
$I_{AVDD-ADCOFF}$	Analog Supply Current[12]			7	15	mA

[1] Applies to all input and bidirectional pins.
[2] Applies to input pins CLKIN, $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.
[3] Applies to all output and bidirectional pins.
[4] Applies to all input only pins.
[5] Applies to input pins with internal pull-down.
[6] Applies to input pins with internal pull-up.
[7] Applies to three-stateable pins.
[8] The I_{DD} supply currents are affected by the operating frequency of the device. The guaranteed numbers are based on an assumed CCLK = 160 MHz, HCLK = 80 MHz for the ADSP-21992BST. I_{DD} refers only to the current consumption on the internal power supply lines (V_{DDINT}). The current consumption at the I/O on the V_{DDEXT} power supply is very much dependent on the particular connection of the device in the final system.
[9] $I_{DD-PEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified. Measured at V_{DDINT} = maximum.
[10] IDLE denotes the current consumption during execution of the IDLE instruction. Measured at V_{DDINT} = maximum.
[11] $I_{DD-PDOWN}$ represents the processor operation in full power-down mode with both core and peripheral clocks disabled. Measured at V_{DDINT} = maximum.
[12] I_{AVDD} represents the power consumption of the analog system. Measured at AVDD = maximum.
[13] The responsibility lies with the user to ensure that the device is operated in such a manner that the maximum allowable junction temperature is not exceeded.

Table 15. Peripherals Electrical Characteristics—ADSP-21992YBC

Parameter	Description	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER					
AC Specifications					
SNR	Signal-to-Noise Ratio[1]	68	72		dB
SNRD	Signal-to-Noise and Distortion[1]	66	71		dB
THD	Total Harmonic Distortion[1]		–80	–66	dB
CTLK	Channel-Channel Crosstalk[1]		–80	–66	dB
CMRR	Common-Mode Rejection Ratio[1]		–82	–66	dB
PSRR	Power Supply Rejection Ratio[1]		0.05	0.2	%FSR
Accuracy					
INL	Integral Nonlinearity[1]		±0.6	±2.0	LSB
DNL	Differential Nonlinearity[1]		±0.5	±1.25	LSB
No Missing Codes			12		Bits
Zero Error[1]			1.25	2.5	%FSR
Gain Error[1]			0.5	1.5	%FSR
Input Voltage					
V_{IN}	Input Voltage Span		2.0		V
C_{IN}	Input Capacitance[2]		10		pF
Conversion Time					
FCLK	ADC Clock Rate			18.75	MHz
t_{CONV}	Total Conversion Time All 8 Channels			773	ns
VOLTAGE REFERENCE					
Internal Voltage Reference[3]		0.94	0.98	1.02	V
Output Voltage Tolerance			40		mV
Output Current			100		µA
Load Regulation[4]		–2	+0.5	+2	mV
Power Supply Rejection Ratio		–2	+0.5	+2	mV
Reference Input Resistance			8		kΩ
POWER-ON RESET					
V_{RST}	Reset Threshold Voltage	1.4		2.1	V
V_{HYST}	Hysteresis Voltage		50		mV

[1] In all cases, the input frequency to the ADC system is assumed to be <100 kHz.
[2] Analog input pins VIN0 to VIN7.
[3] These specifications are for operation of the internal voltage reference so that SENSE = REFCOM, with the default 1.0 V operating mode.
[4] Operation with full 0.1 mA load current. For optimal operation, it is recommended to buffer the VREF output voltage before using it in other parts of the system.

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
Internal (Core) Supply Voltage[1] (V_{DDINT})	–0.3 V to +3.0 V
External (I/O) Supply Voltage[1] (V_{DDEXT})	–0.3 V to +4.6 V
Input Voltage1, [2] (V_{IL} – V_{IH})	–0.5 V to +5.5 V
Output Voltage Swing[1, 2] (V_{OL} – V_{OH})	–0.5 V to +5.5 V
Load Capacitance1 (C_L)	200 pF
Core Clock Period1 (t_{CCLK})	6.25 ns
Core Clock Frequency1 (f_{CCLK})	160 MHz
Peripheral Clock Period1 (t_{HCLK})	12.5 ns
Peripheral Clock Frequency1 (f_{HCLK})	80 MHz
Storage Temperature Range1 (T_{STORE})	–65°C to +150°C
Lead Temperature (5 seconds)1 (T_{LEAD})	85°C

[1] Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Except CLKIN and analog pins.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TIMING SPECIFICATIONS

This next section contains timing information for the external signals of the DSP. Use the exact information given. Do not attempt to derive parameters from the addition or subtraction of other information. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, parameters cannot be added meaningfully to derive longer times.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

Switching characteristics specify how the processor changes its signals. No control is possible over this timing; circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics indicate what the processor will do in a given circumstance. Switching characteristics can also be used to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Programmable Flags Cycle Timing

Table 18 and Figure 8 describe programmable flag operations.

Table 18. Programmable Flags Cycle Timing

Parameter		Min	Max	Unit
Timing Requirement				
t_{HFI}	Flag Input Hold Is Asynchronous	3		ns
Switching Characteristics				
t_{DFO}	Flag Output Delay with Respect to CLKOUT		7	ns
t_{HFO}	Flag Output Hold After CLKOUT High		6	ns

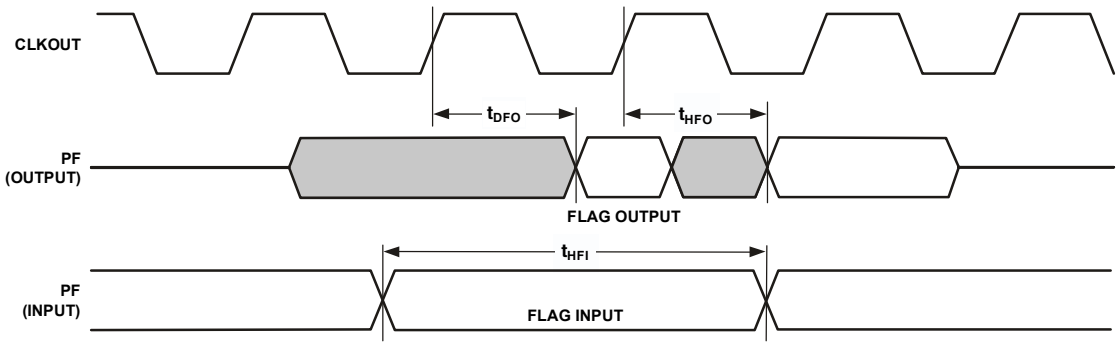


Figure 8. Programmable Flags Cycle Timing

Timer PWM_OUT Cycle Timing

Table 19 and Figure 9 describe timer expired operations. The input signal is asynchronous in "width capture mode" and has an absolute maximum input frequency of 40 MHz.

Table 19. Timer PWM_OUT Cycle Timing

Parameter		Min	Max	Unit
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output[1]	12.5	$(2^{32}-1)$ cycles	ns

[1] The minimum time for t_{HTO} is one cycle, and the maximum time for t_{HTO} equals $(2^{32}-1)$ cycles.

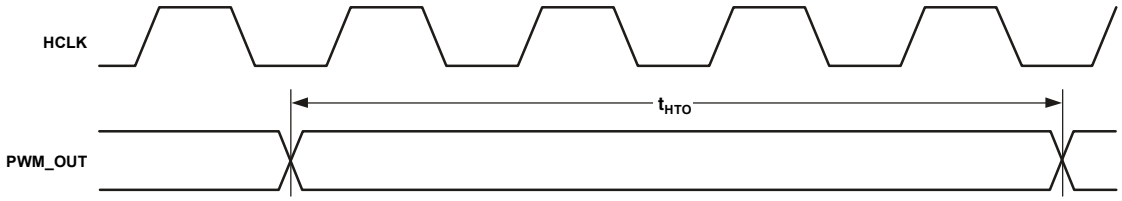


Figure 9. Timer PWM_OUT Cycle Timing

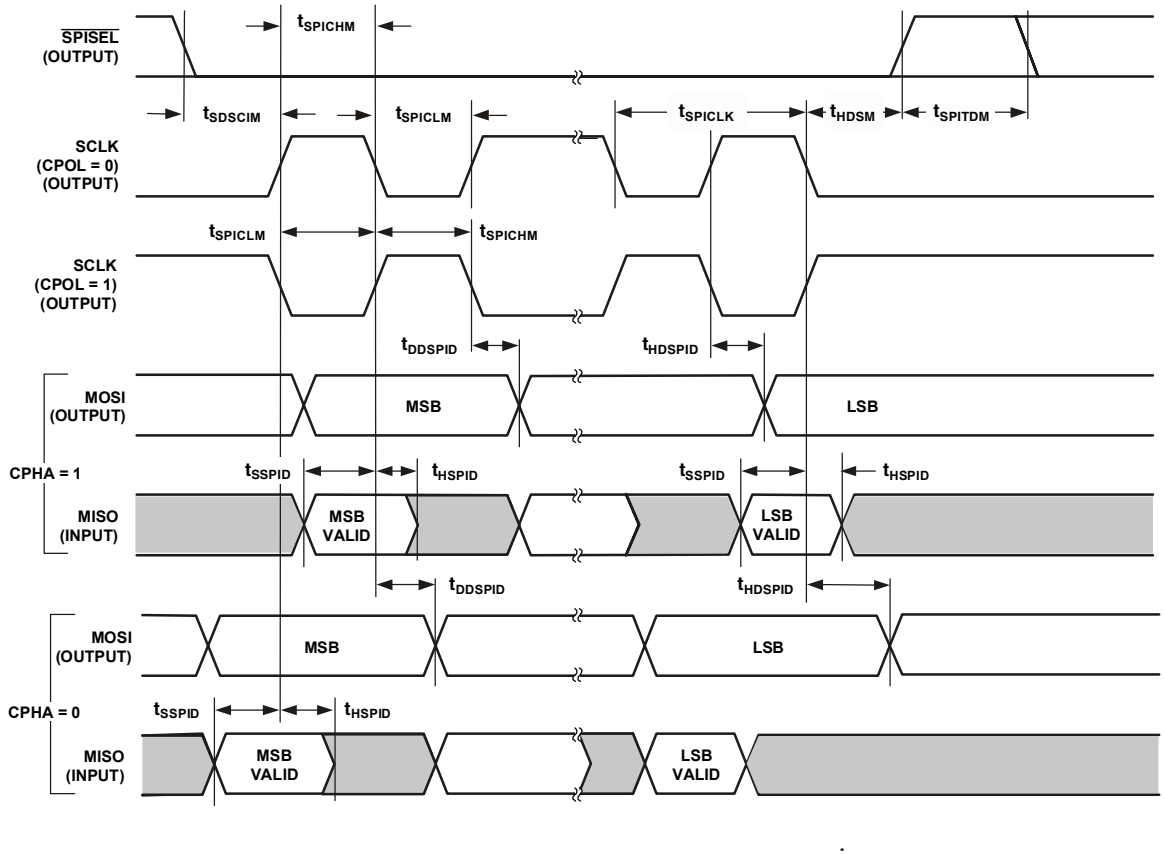


Figure 16. Serial Peripheral Interface (SPI) Port—Master Timing

JTAG Test and Emulation Port Timing

Table 26 and Figure 18 describe JTAG port operations.

Table 26. JTAG Port Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	20		ns
t_{STAP}	TDI, TMS Setup Before TCK High		4	ns
t_{HTAP}	TDI, TMS Hold After TCK High		4	ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]		4	ns
t_{HSYS}	System Inputs Hold After TCK Low[a]		5	ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width[2]	$4t_{TCK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		8	ns
t_{DSYS}	System Outputs Delay After TCK Low[3]	0	22	ns

[1] System outputs = DATA15–0, ADDR21–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, ACK, CLKOUT, $\overline{BG}$, PF15–0, DT, TCLK, RCLK, TFS, RFS, $\overline{BMS}$.
[2] 50 MHz maximum.
[3] System inputs = DATA15–0, ADDR21–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{BR}$, $\overline{BG}$, PF15–0, $\overline{DR}$, TCLK, RCLK, TFS, RFS, CLKOUT, $\overline{RESET}$.

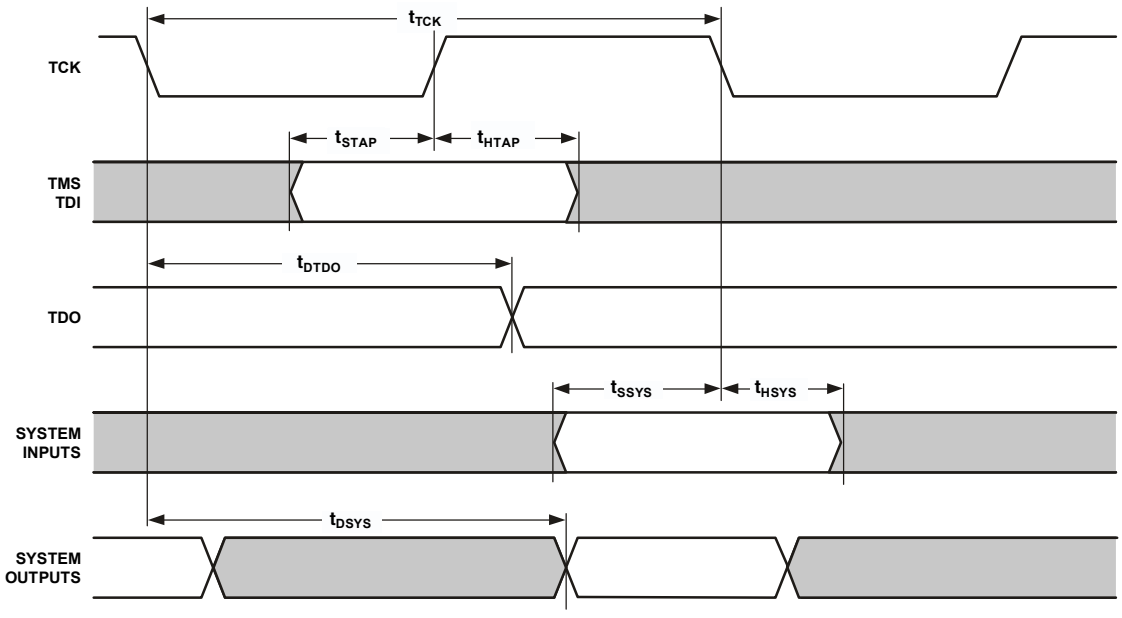


Figure 18. JTAG Port Timing

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved.

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- Number of output pins that switch during each cycle (O)
- The maximum frequency at which they can switch (f)
- Their load capacitance (C)
- Their voltage swing (V_{DD})

and is calculated by the formula below.

$$P_{EXT} = O \times C \times V_{DD}^{2} \times f$$

The load capacitance includes the package capacitance (C_{IN} of the processor). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle. For example, estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory—asynchronous RAM (16-bit)
- One 64K × 16 RAM chip is used with a load of 10 pF
- Maximum peripheral speed CCLK = 80 MHz, HCLK = 80 MHz
- External data memory writes occur every other cycle, a rate of $1/(4t_{HCLK})$, with 50% of the pins switching
- The bus cycle time is 80 MHz (t_{HCLK} = 12.5 ns)

The P_{EXT} equation is calculated for each class of pins that can drive as shown in Table 27.

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation with the following formula.

$$P_{TOTAL} = P_{EXT} + P_{INT}$$

where:

P_{EXT} is from Table 27.

P_{INT} is I_{DDINT} × 2.5 V, using the calculation I_{DDINT} listed in Power Dissipation.

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

Table 27. P_{EXT} Calculation Example

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	10 pF	20 MHz	10.9 V	= 0.01635 W
$\overline{MSx}$	1	0	10 pF	20 MHz	10.9 V	= 0.0 W
$\overline{WR}$	1		10 pF	40 MHz	10.9 V	= 0.00436 W
Data	16	50	10 pF	20 MHz	10.9 V	= 0.01744 W
CLKOUT	1		10 pF	80 MHz	10.9 V	= 0.00872 W = 0.04687 W

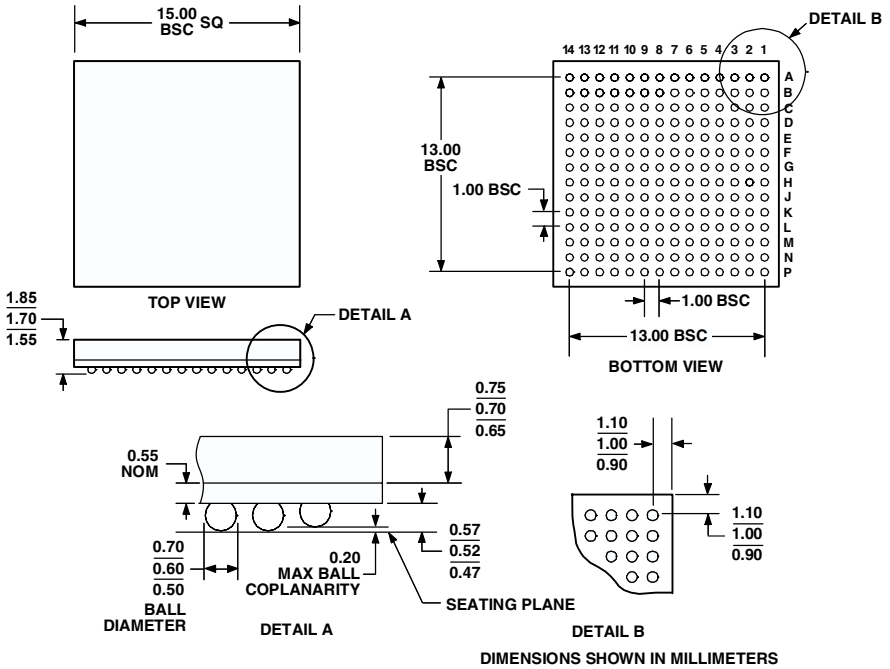
PIN CONFIGURATIONS

Table 28 identifies the signal for each CSP_BGA ball number. Table 29 identifies the CSP_BGA ball number for each signal name. Table 30 identifies the signal for each LQFP lead. Table 31 identifies the LQFP lead for each signal name. Table 4 on Page 17 describes each signal.

Table 31. 176-Lead LQFP Lead Number by Signal

Signal	Lead No.	Signal	Lead No.	Signal	Lead No.	Signal	Lead No.
A0	50	CAPB	156	EIS	116	$\overline{\text{PWMTRIP}}$	87
A1	49	CAPT	155	EIZ	119	RCLK	4
A10	35	CH	77	$\overline{\text{EMU}}$	99	$\overline{\text{RD}}$	8
A11	34	CL	76	$\overline{\text{IOMS}}$	14	$\overline{\text{RESET}}$	106
A12	33	CLKIN	107	MISO	6	RFS	172
A13	30	CLKOUT	109	MOSI	7	SCK	5
A14	29	CML	154	$\overline{\text{MS0}}$	21	SENSE	157
A15	28	CONVST	110	$\overline{\text{MS1}}$	20	TCK	104
A16	27	D0	72	$\overline{\text{MS2}}$	19	TCLK	174
A17	26	D1	71	$\overline{\text{MS3}}$	16	TDI	102
A18	25	D10	60	nc	1	TDO	101
A19	24	D11	55	nc	2	TFS	173
A2	48	D12	54	nc	42	TMR0	111
A3	47	D13	53	nc	43	TMR1	114
A4	46	D14	52	nc	44	TMR2	115
A5	40	D15	51	nc	83	TMS	103
A6	39	D2	70	nc	89	$\overline{\text{TRST}}$	100
A7	38	D3	69	nc	90	VDDEXT	3
A8	37	D4	68	nc	96	VDDEXT	18
A9	36	D5	65	nc	130	VDDEXT	32
ACK	10	D6	64	nc	131	VDDEXT	45
AH	81	D7	63	nc	132	VDDEXT	57
AL	80	D8	62	nc	152	VDDEXT	75
ASHAN	162	D9	61	nc	176	VDDEXT	91
AUX0	124	GND	17	PF0/$\overline{\text{SPISS}}$	147	VDDEXT	113
AUX1	123	GND	22	PF1/SPISEL1	146	VDDEXT	133
$\overline{\text{AUXTRIP}}$	122	GND	31	PF10	135	VDDEXT	143
AVDD	151	GND	41	PF11	134	VDDINT	23
AVDD	169	GND	56	PF12	128	VDDINT	59
AVSS	150	GND	58	PF13	127	VDDINT	67
AVSS	168	GND	66	PF14	126	VDDINT	98
$\overline{\text{BG}}$	12	GND	74	PF15	125	VDDINT	118
$\overline{\text{BGH}}$	13	GND	88	PF2/SPISEL2	145	VDDINT	149
BH	79	GND	97	PF3/SPISEL3	144	VIN0	161
BL	78	GND	112	PF4/SPISEL4	141	VIN1	160
BMODE0	93	GND	117	PF5/SPISEL5	140	VIN2	159
BMODE1	94	GND	129	PF6/SPISEL6	139	VIN3	158
BMODE2	95	GND	142	PF7/SPISEL7	138	VIN4	164
$\overline{\text{BMS}}$	15	GND	148	PF8	137	VIN5	165
$\overline{\text{BR}}$	11	GND	175	PF9	136	VIN6	166
BSHAN	163	DR	171	$\overline{\text{POR}}$	105	VIN7	167
BYPASS	92	DT	170	PWMPOL	85	VREF	153
CANRX	73	EIA	121	$\overline{\text{PWMSR}}$	86	$\overline{\text{WR}}$	9
CANTX	82	EIB	120	PWMSYNC	84	XTAL	108

OUTLINE DIMENSIONS



NOTES:
1. THE ACTUAL POSITION OF THE BALL GRID IS WITHIN 0.25 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES.
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.10 OF ITS IDEAL POSITION RELATIVE TO THE BALL GRID.
3. DIMENSIONS COMPLY WITH JEDEC STANDARD MO-192 VARIATION AAE-1 WITH THE EXCEPTION OF MAXIMUM HEIGHT.
4. CENTER DIMENSIONS ARE NOMINAL.

Figure 22. 196-Ball CSP_BGA (BC-196-2)

ORDERING GUIDE

Model	Temperature Range[1]	Instruction Rate	Operating Voltage	Package Description	Package Option
ADSP-21992BBC	–40°C to +85°C	150 MHz	2.5 Int. V/3.3 Ext. V	196-Ball CSP_BGA	BC-196-2
ADSP-21992YBC	–40°C to +125°C	150 MHz	2.5 Int. V/3.3 Ext. V	196-Ball CSP_BGA	BC-196-2
ADSP-21992BST	–40°C to +85°C	160 MHz	2.5 Int. V/3.3 Ext. V	176-Lead LQFP	ST-176
ADSP-21992BSTZ[2]	–40°C to +85°C	160 MHz	2.5 Int. V/3.3 Ext. V	176-Lead LQFP	ST-176
ADSP-21992YST	–40°C to +125°C	100 MHz	2.5 Int. V/3.3 Ext. V	176-Lead LQFP	ST-176

[1] Referenced temperature is ambient temperature.
[2] Z = RoHS Complaint Part

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