



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

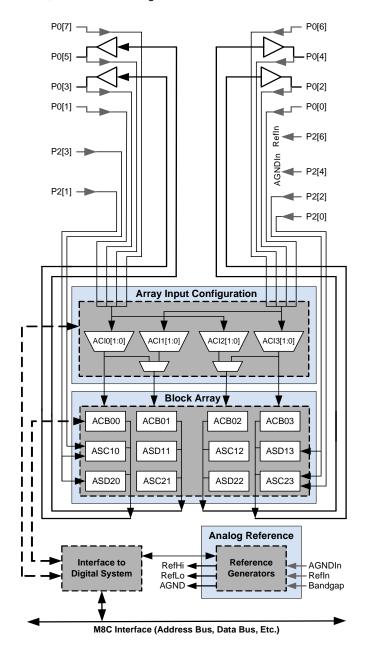
Details

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K × 8)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27243-24pvi

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.



Analog System Block Diagram

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is shown in the second row of the table.

PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x43	up to 44	2	8	12	4	4	12
CY8C24x23	up to 24	1	4	12	2	2	6
CY8C24x23A	up to 24	1	4	12	2	2	6
CY8C22x13	up to 16	1	4	8	1	1	3

PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.



This chapter describes, lists, and illustrates the CY8C27x43 PSoC device pins and pinout configurations.

1.1 Pinouts

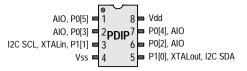
The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

1.1.1 8-Pin Part Pinout

Pin	Ту	ре	Pin	Description
No.	Digital	Analog	Name	Description
1	10	10	P0[5]	Analog column mux input and column output.
2	10	10	P0[3]	Analog column mux input and column output.
3	10		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
4	Power		Vss	Ground connection.
5	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
6	10	10	P0[2]	Analog column mux input and column output.
7	10	10	P0[4]	Analog column mux input and column output.
8	Power Vdd		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27143 8-Pin PSoC Device



1.1.2 20-Pin Part Pinout

Table 1-2. 20-Pin Part Pinout (SSOP, SOIC)

Pin	Ту	ре	Pin				
No.	Digital	Analog	Name	Description			
1	10	I	P0[7]	Analog column mux input.			
2	10	10	P0[5]	Analog column mux input and column output.			
3	10	10	P0[3]	Analog column mux input and column output.			
4	10	I	P0[1]	Analog column mux input.			
5	Po	wer	SMP	Switch Mode Pump (SMP) connection to external components required.			
6	10		P1[7]	I2C Serial Clock (SCL)			
7	10		P1[5]	I2C Serial Data (SDA)			
8	10		P1[3]				
9	10		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SC			
10	Power		Vss	Ground connection.			
11	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)			
12	ю		P1[2]				
13	10		P1[4]	Optional External Clock Input (EXTCLK)			
14	10		P1[6]				
15	Inj	out	XRES	Active high external reset with internal pull down.			
16	IO	I	P0[0]	Analog column mux input.			
17	10	10	P0[2]	Analog column mux input and column output.			
18	Ю	10	P0[4]	Analog column mux input and column output.			
19	ю	Ι	P0[6]	Analog column mux input.			
20	Power V		Vdd	Supply voltage.			

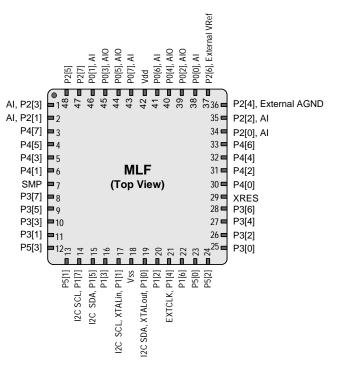
CY8C27243 20-Pin PSoC Device

LEGEND: A = Analog, I = Input, and O = Output.

Table 1-6. 48-Pin Part Pinout (MLF*)

Pin	Ту	ре	Pin	
No.	Digital	Analog	Name	Description
1	10		P2[3]	Direct switched capacitor block input.
2	10	I	P2[1]	Direct switched capacitor block input.
3	10		P4[7]	
4	10		P4[5]	
5	10		P4[3]	
6	10		P4[1]	
7	Po	wer	SMP	Switch Mode Pump (SMP) connection to external components required.
8	10		P3[7]	
9	10		P3[5]	
10	Ю		P3[3]	
11	10		P3[1]	
12	10		P5[3]	
13	Ю		P5[1]	
14	10		P1[7]	I2C Serial Clock (SCL)
15	Ю		P1[5]	I2C Serial Data (SDA)
16	10		P1[3]	
17	10		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
18	Po	wer	Vss	Ground connection.
19	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
20	10		P1[2]	
21	10		P1[4]	Optional External Clock Input (EXTCLK)
22	10		P1[6]	
23	Ю		P5[0]	
24	10		P5[2]	
25	10		P3[0]	
26	10		P3[2]	
27	10		P3[4]	
28	10		P3[6]	
29		out	XRES	Active high external reset with internal pull down.
30	10		P4[0]	
31	10		P4[2]	
32	10		P4[4]	
33	10		P4[6]	
34	10	I	P2[0]	Direct switched capacitor block input.
35	10	I	P2[2]	Direct switched capacitor block input.
36	10		P2[4]	External Analog Ground (AGND)
37	10		P2[6]	External Voltage Reference (VRef)
38	10	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42		wer	Vdd	Supply voltage.
43	10	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	10		P2[5]	

CY8C27643 48-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

 * The MLF package has a center pad that must be connected to ground (Vss).

PRTOIDE 00 R/W 40 ASC10CR0 80 R/W C0 PRTOBE 01 R/W 441 ASC10CR1 81 R/W C2 PRTOBM2 03 R/W 443 ASC10CR1 84 R/W C3 PRTIDR 04 R/W 444 ASD11CR1 85 R/W C4 PRTIG 05 R/W 445 ASD11CR1 86 R/W C6 PRTIG 06 R/W 446 ASD11CR2 86 R/W C6 PRTZDR 08 R/W 448 ASC12CR1 88 R/W C8 PRTZBN2 08 R/W 448 ASC12CR2 88 R/W C8 PRTZBN2 08 R/W 444 ASD13CR1 80 R/W C6 PRTZBN2 00 R/W 446 ASD13CR2 86 R/W C0 P PRT3L 00 R/W 450 <	Name	Addr (0,Hex)	Access									
PRTODM2 O2 R/W H 42 ASC10CR2 82 R/W CC3 PRTIDM 04 R/W H 44 ASD11CR0 84 R/W CC3 PRTIDR 04 R/W H 45 ASD11CR1 85 R/W CC6 PRTISD 05 R/W H ASD11CR1 85 R/W CC6 PRTISD 06 R/W H ASD11CR1 85 R/W CC6 PRTOM2 08 R/W H ASC12CR2 AS R/W CA PRTZSS 0.0 R/W H ASC12CR3 B R/W CA PRTZSS 0.0 R/W H ASC12CR3 B R/W CC8 PRTADR 0.0 R/W H ASC12CR3 B R/W CC6 PRTADR 0.0 R/W ASC12CR3 B R/W CC7 PRTADR 0.0 R/W ASC12CR					-							
PRTODRUZ 0.3 F.W. 4.4 ASC10CR3 8.3 R.W. C.G. PRTIJR 0.4 R.W. 4.5 ASD11CR1 85 R.W. C.G. PRTIJS 0.5 R.W. 4.6 ASD11CR1 85 R.W. C.G. PRTIJDR 0.6 R.W. 4.7 ASD11CR1 85 R.W. C.G. PRTIJDR 0.6 R.W. 4.8 ASC12CR1 83 R.W. C.G. PRT2DR 0.8 R.W. 4.4 ASC12CR2 8.4 R.W. C.G. PRT2DR 0.6 R.W. 4.4 ASC12CR3 8.8 R.W. C.G. PRT3DR 0.6 R.W. 4.6 ASD13CR1 8.0 R.W. C.G. PRT3DR 0.6 R.W. 4.6 ASD20CR0 9.0 R.W. D.0 PRT3DR 0.7 R.W. 5.0 ASD20CR0 9.0 R.W. D.0 PRT3DR 10 R		-										
PRT1IE 04 RW 44 ASD11CR0 84 RW CC 5 PRT16S 06 RW 46 ASD11CR1 86 RW C6 C7 PRT10M2 07 RW 47 ASD11CR3 87 RW C7 PRT2DR 08 RW 48 ASC12CR0 88 RW C6 PRT3DR 08 RW 44 ASC12CR1 89 RW C4 PRT3DR 00 RW 44 ASC12CR3 48 RW C4 PRT3DR 0C RW 44 ASD13CR0 86 RW C6 PRT3DR 0C RW 44 ASD13CR0 86 RW C6 PRT3DR 0C RW 45 ASD20CR1 87 RW C6 PRT3DR 10 RW 51 ASD20CR1 97 RW D0 PRT3DR 11 RVW 52 ASD20CR1		-										
PRT11E O.G R.W 45 ASD11CR1 85 R.W C.G PRT102 OF R.W C.G PRT102 OF R.W C.G PRT102 OF R.W C.G PRT102 OF R.W C.G PRT2DR OS R.W C.G D.S PRT2DR OS R.W C.G D.S PRT2DR OS R.W C.G D.S PRT2DR OS R.S D.S	-											
PRT10S 06 RW 46 ASD11CR3 87 RW C6 PRT1DM2 07 RW 47 ASD11CR3 RS RW C6 PRT2E 08 RW 48 ASC12CR1 88 RW C6 PRT2G 00 RW 44 ASC12CR2 84 RW CA PRT3DR 00 RW 44 ASC12CR3 88 RW CA PRT3DR 00 RW 44 ASC12CR3 88 RW CC PRT3DR 00 RW 44 ASC12CR3 88 RW CC PRT3DR 00 RW 45 ASD20CR1 80 RW CD PRT3DR 00 RW 51 ASD20CR3 93 RW D0 PRT4GS 16 RW 55 ASC21CR3 93 RW D2 RM3 PRT3DR 14 RW 56 ASC21CR3 94<		-										
PRT1DM2 07 RW 47 ASD11CR3 87 RW C.7 PRT2DR 08 RW 48 ASC12CR0 88 RW C6 PRT3CS 0A RW 40 ASC12CR0 88 RW C6 PRT3CS 0A RW 44 ASC12CR1 89 RW C6 PRT3DR 0C RW 44 ASC12CR2 88 RW C6 PRT3DR 0D RW 44 ASC12CR2 88 RW C6 PRT3DR 0D RW 44 ASD13CR3 86 RW C6 PRT3DR 0C RW 44 ASD2CR0 90 RW D0 PRT3DR 10 RW 50 ASD2CR19 91 RW D1 PRT41E 11 RW 51 ASD2CR18 93 RW D2 PRT3 PRT41E 18 W 55 ASC21CR19												
PRT2DR 06 R/W 48 ASC12CR1 89 R/W C63 PRT2E 00 R/W 49 ASC12CR1 89 R/W C63 PRT2DM2 06 R/W 40 ASC12CR2 8A R/W C64 PRT3DR 0C R/W 40 ASC12CR3 8B R/W C62 PRT3DR 0C R/W 40 ASD13CR4 8D R/W C62 PRT3DR 0C R/W 40 ASD13CR4 8D R/W C62 PRT3DR 0F R/W 44 ASD13CR4 8F R/W C62 PRT3DR 0F R/W 451 ASD20CR1 90 R/W D0 PRT41E 11 R/W 53 ASD20CR3 93 R/W D3 PRT3DR 14 R/W 55 ASC21CR1 95 R/W D6 PRT3DR 14 R/W 56 ASC221CR1												
PRT2DS 0.A R/W 4A ASC12CR2 8A R/W C.A PRT3DR 06 R/W 4B ASC12CR2 8A R/W CG PRT3DR 0C R/W 4C ASD13CR0 8C R/W CC PRT3DR 0D R/W 4D ASD13CR2 8R R/W CC PRT3DR 0D R/W 4D ASD13CR2 8R R/W CC PRT3DR 0D R/W 4F ASD13CR3 8F R/W CC PRT4DR 10 R/W 51 ASD20CR1 91 R/W D0 PRT4DR 13 R/W 53 ASD20CR2 92 R/W D4 PRT3DR 14 R/W 54 ASC21CR1 91 R/W D4 PRT3DK 15 R/W 55 ASC21CR2 96 R/W 12C_CRG D6 PRT3DK 14 R/W 56 A	PRT2DR	08	RW				ASC12CR0	88	RW		C8	
PRT2DM2 0B RW 4B ASC12CR3 8B RW CB PRT3JE 0C RW 4D ASD13CR1 8D RW CC PRT3JE 0D RW 4D ASD13CR1 8D RW CC PRT3JE 0F RW 4E ASD13CR3 8F RW CF PRT3DM2 0F RW 4E ASD13CR3 8F RW CF PRT3DM2 0F RW 4E ASD13CR3 8F RW CF PRT4DM2 10 RW 50 ASD20CR3 91 RW D0 PRT4DM2 12 RW 53 ASD20CR3 93 RW D3 PRT3DR 14 RW 54 ASD21CR3 96 RW CC_SCR D7 PRT3DR 14 RW 57 ASC21CR3 97 RW I2C_SCR D7 PRT3DM2 17 RW 55	PRT2IE	09	RW		49		ASC12CR1	89	RW		C9	
PRT3DR 0C RW 4C ASD13CR0 8C RW CC CC PRT3GS 0E RW 4D ASD13CR1 8D RW CD PRT3GS 0E RW 4E ASD13CR2 8E RW CE PRT3GS 0F RW 4F ASD13CR2 8E RW CE PRT4DR 10 RW 50 ASD20CR2 90 RW D0 PRT41R 11 RW 51 ASD20CR2 92 RW D2 PRT41R 11 RW 53 ASD20CR2 92 RW D3 PRT41SE 11 RW 55 ASC21CR1 95 RW D3 PRT51E 16 RW 56 ASC21CR2 96 RW ICC_CFG D6 RW PRT50M2 17 RW 57 ASC21CR2 9A RW INT_CLR0 DA RW ICC_CFG D8	PRT2GS	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT31E OD RW 4D ASD13CR1 8D RW CD PRT30M2 0F RW 4E ASD13CR2 8E RW CF PRT3DM2 0F RW 4F ASD13CR2 8F RW CF PRT4DR 10 RW 50 ASD20CR1 91 RW D0 PRT41E 11 RW 51 ASD20CR2 92 RW D2 PRT40M2 13 RW 53 ASD20CR2 93 RW D3 PRT50R 14 RW 55 ASD20CR3 93 RW D4 PRT30K2 16 RW 56 ASC21CR3 98 RW ICC_CFG D6 RW PRT30K2 17 RW 57 ASC21CR3 98 RW ICC_CFG D6 RW 18 58 ASD22CR3 98 RW ICL_CR DA RW 10 55 <t< td=""><td></td><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>		-										
PRT3G OE RW 4E ASD13CR2 8E RW CE PRT3DM2 OF RW 4F ASD13CR3 8F RW CF PRT4DR 10 RW 50 ASD20CR0 90 RW D0 PRT4IE 11 RW 51 ASD20CR3 93 RW D3 PRT4GS 12 RW 52 ASD20CR3 93 RW D3 PRT5DR 14 RW 55 ASC21CR0 94 RW D4 PRTSDR 16 RW 56 ASC21CR2 96 RW IC2_CFG D5 PRTSDR 17 RW 57 ASC21CR2 96 RW IC2_SCR D7 # PRTSDR 18 58 ASD22CR1 98 RW IC2_MSCR D8 RW 10 5D ASC23CR1 98 RW INT_CLR1 D8 RW												
PRT3DM2 OF RW 4F ASD13CR3 8F RW CF PRT4DR 10 RW 50 ASD20CR0 90 RW D0 PRT4E 11 RW 51 ASD20CR1 91 RW D2 PRT4E 11 RW 53 ASD20CR3 93 RW D3 PRT5DR 14 RW 54 ASD20CR3 93 RW D4 PRT5DR 14 RW 55 ASC1CR1 95 RW D4 PRT5DR 16 RW 56 ASC21CR2 96 RW 12C_CBC D6 RW PRT5DN2 17 RW 57 ASC21CR2 98 RW IZC_SCR D7 # 19 C 59 ASD22CR3 98 RW INT_CLR1 D8 RW 10 C 5C ASC23CR1 90 RW INT_CLR1 D8 RW 10<												
PRT4DR 10 RW 50 ASD20CR0 90 RW D0 PRT4IE 11 RW 51 ASD20CR1 91 RW D1 PRT40S 12 RW 53 ASD20CR2 92 RW D2 PRT4DR 13 RW 53 ASD21CR2 92 RW D3 PRT5DR 14 RW 54 ASC21CR2 96 RW D4 PRT5GS 16 RW 56 ASC21CR3 97 RW I2C_CFG D6 RW PRT5DM2 17 RW 56 ASC21CR3 97 RW I2C_CMC D8 RW 18 58 ASD22CR1 98 RW I2C_CMC DA RW 10 56 ASC23CR3 96 RW INT_CLR1 DB RW 11C 55 ASC23CR3 96 RW INT_MSK1 E1 RW		-						-				
PRT4IE 11 RW 51 ASD20CR1 91 RW D1 PRT4GS 12 RW 52 ASD20CR2 92 RW D2 PRT4DW2 13 RW 53 ASD20CR3 93 RW D3 PRT5DR 14 RW 54 ASC21CR1 95 RW D4 PRT5DR 14 RW 56 ASC21CR2 96 RW 12C_CFG D6 RW PRT5DL2 17 RW 57 ASC21CR2 98 RW 12C_CSCR D7 # PRT5DL1 17 RW 57 ASC22CR1 99 RW 12C_CMSCR D8 RW 18 58 ASD22CR3 98 RW INT_CLR1 D8 RW 10 50 ASC23CR3 9F RW INT_MSK3 DE RW 11 1 F 55 ASC23CR3 9F RW INT_MSK3 DE		-										
PRT4DX2 12 RW 52 ASD20CR2 92 RW D2 PRT4DM2 13 RW 53 ASD20CR3 93 RW D3 PRT5DR 14 RW 55 ASC21CR0 94 RW D4 PRT5IE 15 RW 56 ASC21CR3 97 RW I2C_CFG D6 RW PRT50S 16 RW 57 ASC21CR3 97 RW I2C_CFG D8 RW PRT50M2 17 RW 57 ASC22CR3 98 RW I2C_DR D8 RW 14 C 58 ASD22CR3 98 RW IZC_MSC D0 RW 16 C 56 ASC23CR1 90 RW INT_CLR3 DD RW 17 AMX_IN 60 RW ASC INT_MSK1 E1 RW DB800DR0 23 # ARF_CR 63 RW A3		-										
PRT4DM2 13 RW 53 ASD20CR3 93 RW D3 PRT5DR 14 RW 54 ASC21CR1 94 RW D4 PRT5DR 15 RW 55 ASC21CR1 95 RW D25 PRT5CS 16 RW 56 ASC21CR2 96 RW I2C_SCR D7 # PRT5DM2 17 RW 57 ASC21CR3 97 RW I2C_SCR D7 # 18 58 ASD22CR1 99 RW IZC_MSCR D9 # 14 55 ASD22CR2 9A RW INT_CLR0 DA RW 16 56 ASD22CR3 9B RW INT_CLR3 DD RW 17 57 ASC23CR3 9F RW DE RW 18 56 ASC23CR3 9F RW DE RW DB												
PRT50R 14 RW 54 ASC21CR0 94 RW D4 PRTSIE 15 RW 55 ASC21CR1 95 RW D5 PRTS0M 17 RW 56 ASC21CR2 96 RW I2C_CFG D6 RW PRT50M2 17 RW 57 ASC21CR3 97 RW I2C_SCR D7 # 18 58 ASD22CR1 99 RW I2C_MSCR D9 # 14 58 ASD22CR2 9A RW INT_CLR0 DA RW 16 55 ASC23CR3 9E RW INT_CLR3 DC RW RW DR DR RW DR DR RW DR RW INT_MSK3 DE RW DR RW INT_MSK3 DE RW DB DB DB DB DE DB RW DB DB DE RW <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>-</td><td></td><td></td><td></td><td> </td></t<>								-				
PRT6IE 15 RW 55 ASC21CR1 95 RW D5 PRT6GS 16 RW 56 ASC21CR2 96 RW I2C_CFG D6 RW PRT5DM2 17 RW S8 ASD22CR3 97 RW I2C_SCR D7 # 18 58 ASD22CR1 99 RW I2C_MSCR D8 RW 14 54 ASD22CR2 9A RW INT_CLR DA RW 18 55 ASC23CR1 99 RW INT_CLR DA RW 10 55 ASC23CR3 95 RW INT_CLR3 DD RW 116 55 ASC23CR3 97 RW INT_MSK3 DE RW 118 57 ASC33CR3 97 RW INT_MSK3 DE RW 116 58 ASC23CR3 97 RW INT_MSK3 DE RW DB800DR0 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>												
PRT5GS 16 RW 56 ASC21CR2 96 RW 12C_CFG D6 RW PRT5DM2 17 RW 57 ASC21CR3 97 RW 12C_SCR D7 # 19 59 ASD22CR1 99 RW 12C_MSCR D9 # 14 54 ASD22CR3 98 RW INT_CLR1 D8 RW 16 56 ASD22CR3 98 RW INT_CLR1 D8 RW 16 56 ASC23CR1 90 RW INT_CLR3 DD RW 17 T 55 ASC23CR2 95 RW INT_MSK3 DE RW 18 58 ASC23CR2 97 RW INT_MSK3 DE RW 16 4 ASC23CR2 97 RW INT_MSK3 DE RW DB800DR0 20 # AMX_I 60 RW A0 INT_MSK1 E1 RW												
18 18 58 ASD22CR0 98 RW 12C_DR D8 RW 14 59 ASD22CR1 99 RW IIZ_MSCR D9 # 18 58 ASD22CR2 9A RW INT_CLR0 DA RW 18 58 ASD22CR3 9B RW INT_CLR1 DB RW 10 55C ASC32CR1 9D RW INT_CLR3 DD RW 11 10 55F ASC23CR2 9E RW INT_MSK3 DE RW 11F 55F ASC23CR3 9F RW DF DB00DR0 20 # AMX_IN 60 RW ASC32CR2 9E RW INT_MSK3 DE RW DB800DR0 20 # AMX_IN 60 RW ASC32CR2 9E RW INT_MSK3 DE RW DB00DR0 28 W DB01DR1 21 W 61 A1 IN	-	-								I2C CFG		RW
19 59 ASD22CR1 99 RW I2C_MSCR D9 # 1A 5A ASD22CR2 9A RW INT_CLR0 DA RW 1B 5B ASD22CR3 9B RW INT_CLR1 DB RW 1C 5C ASC23CR0 9C RW INT_CLR3 DD RW 1D 5D ASC23CR1 9D RW INT_CLR3 DD RW 1E 5F ASC23CR2 9F RW INT_MSK3 DE RW DB800DR0 20 # AMA_IN 60 RW A0 INT_MSK1 E1 RW DB800DR1 21 W 61 A1 INT_MSK1 E1 RW DB800DR2 22 RW 61 A1 INT_MSK1 E1 RW DB800DR1 24 # CMP_CR0 63 RW A3 RES_WDT E3 W DB801DR2 26 </td <td>PRT5DM2</td> <td>17</td> <td>RW</td> <td></td> <td>57</td> <td></td> <td>ASC21CR3</td> <td>97</td> <td>RW</td> <td>I2C_SCR</td> <td>D7</td> <td>#</td>	PRT5DM2	17	RW		57		ASC21CR3	97	RW	I2C_SCR	D7	#
1A 1A 5A ASD22CR2 9A RW INT_CLR0 DA RW 1B 5B ASD22CR3 9B RW INT_CLR1 DB RW 1C 5C ASC23CR0 9C RW INT_CLR3 DD RW 1D 5D ASC23CR1 9D RW INT_CLR3 DD RW 1E 5F ASC23CR2 9E RW INT_MSK3 DE RW DB800DR0 20 # AMX_IN 60 RW ASC23CR3 9F RW DF DB800DR1 21 W 61 AT INT_MSK0 E0 RW DB800DR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DB800DR1 24 # CMP_CR0 64 A4 A4 DEC_DL E5 RC DB801DR1 25 W ASY CR67 A7 DEC_DL E5		18			58		ASD22CR0	98	RW	I2C_DR	D8	RW
1B 5B ASD22CR3 9B RW INT_CLR1 DB RW 1C 5C ASC23CR0 9C RW DC DC 1D 5D ASC23CR1 9D RW INT_CLR3 DD RW 1E 5E ASC23CR2 9E RW INT_MSK3 DE RW DB800DR 20 # AMX_IN 60 RW AO INT_MSK3 DE RW DB800DR0 20 # AMX_IN 60 RW AO INT_MSK1 E1 RW DB800DR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DB801DR1 25 W ASY_CR 65 # A4 DEC_DL E5 RC DB801DR1 25 W ASY_CR 66 RW A6 DEC_OL E5 RV DB801CR0 27 # 67 A7 DEC_CR1		19			59		ASD22CR1	99	RW	I2C_MSCR	D9	#
1C 5C ASC23CR0 9C RW INT_CLR3 DC 1D 5D ASC23CR1 9D RW INT_CLR3 DD RW 1F 5F ASC23CR2 9E RW INT_MSK3 DE RW DB600DR0 20 # AMX_IN 60 RW AO INT_MSK0 EO RW DB600DR1 21 W 61 A1 INT_MSK0 EO RW DB600DR2 22 RW 62 A2 INT_MSK1 E1 RW DB601DR1 24 # CMP_CR0 64 # A4 DEC_DH E5 RC DB801DR1 25 W ASY_CR 65 # A5 DEC_DH E5 RW DB801DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DC802DR1 29 W 69 A9 MUL_Y E9 W											DA	RW
1D 5D ASC23CR1 9D RW INT_CLR3 DD RW 1E 5E ASC23CR2 9E RW INT_MSK3 DE RW DB800DR0 20 # AMX_IN 60 RW AO INT_MSK0 EO RW DB800DR1 21 W 61 A1 INT_MSK1 E1 RW DB800DR1 21 W 61 A1 INT_MSK1 E1 RW DB800CR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DB801DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DB801DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DC802DR0 28 # 68 A8 A8 MUL_Y E9 W DC802DR1 29 W 69 A7 DEC_CR1										INT_CLR1		RW
1E 5E ASC23CR2 9E RW INT_MSK3 DE RW DBB00DR 20 # AMX_IN 60 RW AO INT_MSK0 E0 RW DBB00DR1 21 W 61 A1 INT_MSK1 E1 RW DBB00DR2 22 RW 62 A2 INT_VC E2 RC DBB00DR1 24 # CMP_CR0 64 # A4 DEC_DL E5 RC DBB01DR1 25 W ASY_CR 65 # A4 DEC_DL E5 RC DBB01DR1 25 W ASY_CR 65 # A4 DEC_DL E5 RC DB801DR2 26 RW CMB A6 DEC_DL E5 RC DB801DR2 28 # 68 A8 MUL_X E8 W DC802DR1 29 W 69 A9 MUL_Y E9 W<												
1F 5F ASC23CR3 9F RW DF DBB00DR0 20 # AMX_IN 60 RW A0 INT_MSK0 E0 RW DBB00DR1 21 W 61 A1 INT_MSK1 E1 RW DBB00DR2 22 RW 62 A2 INT_VC E2 RC DBB00DR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DB801DR1 25 W ASY_CR 65 # A4 DEC_DH E4 RC DB801DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DB801DR1 25 W CMP_CR1 66 RW A6 DEC_CR1 E7 RW DC802DR1 29 W 69 A8 MUL_X E8 W DC802DR2 2A RW 6A AA AMU_DL E <r< td=""></r<>												
DBB00DR0 20 # AMX_IN 60 RW A0 INT_MSK0 E0 RW DBB00DR1 21 W 61 A1 INT_MSK1 E1 RW DBB00DR2 22 RW 62 A2 INT_VC E2 RC DBB00CR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DBB01DR0 24 # CMP_CR0 64 # A4 DEC_DL E5 RC DB801DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DB801CR0 27 # 67 A7 DEC_CR1 E7 RW DC802DR1 29 W 68 A8 MUL_Y E9 W DC802DR2 2A RW 66 AA AA MUL_DH EA R DC803DR1 2D W 6B AA AC ACC_DRD								-		INT_MSK3		RW
DBB00DR1 21 W - 61 A1 INT_MSK1 E1 RW DBB00DR2 22 RW 62 A2 INT_VC E2 RC DBB00DR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DBB01DR0 24 # CMP_CR0 64 # A4 DEC_DH E4 RC DBB01DR1 25 W ASY_CR 65 # A4 DEC_DL E5 RC DB801DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DCB02DR0 28 # 68 A8 MUL_X E8 W DCB02DR1 29 W 69 A9 MUL_Y E9 W DCB02DR2 2A RW 6A AA MUL_DH EA R DCB03DR1 2D W 6D AD ACC_DRO ED <td>DBB00DB0</td> <td></td> <td>#</td> <td>ΔΜΧ ΙΝΙ</td> <td></td> <td>RW/</td> <td>ASUZSUKS</td> <td></td> <td>RVV</td> <td>INT MSKO</td> <td></td> <td>RW/</td>	DBB00DB0		#	ΔΜΧ ΙΝΙ		RW/	ASUZSUKS		RVV	INT MSKO		RW/
DBB00DR2 22 RW 62 A A2 INT_VC E2 RC DBB00CR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DB01DR0 24 # CMP_CR0 64 # A4 DEC_DH E4 RC DB01DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DB01DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DCB02DR0 28 # 68 A3 MUL_X E8 W DCB02DR1 29 W 69 A49 MUL_V E9 W DCB03DR1 20 W 66 AA AA MUL_DL EB R DCB03DR1 2C # 6C AC ACC_DR0 ED RW DCB03DR2 2E RW 6F AB ACC_DR3		-				1				_	-	
DBB00CR0 23 # ARF_CR 63 RW A3 RES_WDT E3 W DBB01DR0 24 # CMP_CR0 64 # A4 DEC_DH E4 RC DBB01DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DBB01DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DBB01CR0 27 # 66 RW A6 DEC_CR1 E7 RW DCB02DR0 28 # 68 A8 MUL_Y E9 W DCB02DR1 29 W 6A AA AA MUL_DL EB R DCB02DR2 2A RW 6A AA AA MUL_DL EB R DCB03DR1 2D W 6D AA AC ACC_DR3 EE RW DCB03DR1 2D W 6E												
DBB01DR0 24 # CMP_CR0 64 # A4 DEC_DH E4 RC DBB01DR1 25 W ASY_CR 65 # A5 DEC_DL E5 RC DBB01DR2 26 RW CMP_CR1 66 RW A6 DEC_CR1 E7 RW DBB01CR0 27 # 66 RW A6 DEC_CR1 E7 RW DCB02DR0 28 # 68 A8 MUL_X E8 W DCB02DR1 29 W 68 A8 MUL_DH EA R DCB02DR1 29 W 6A AA AB MUL_DH EA R DCB02DR1 20 W 6A AA AC ACC_DR1 EC RW DCB03DR1 2D W 6C AC AC ACC_DR3 EE RW DCB03DR2 2E RW 6E AE ACC_DR3				ARF CR	-	RW				-		
DBB01DR2 26 RW CMP_CR1 66 RW A6 DEC_CR0 E6 RW DBB01CR0 27 # 67 A7 DEC_CR1 E7 RW DCB02DR0 28 # 68 A8 MUL_X E8 W DCB02DR1 29 W 69 A9 MUL_Y E9 W DCB02DR2 2A RW 6A A8 MUL_DL EB R DCB02DR0 2E RW 6A AA MUL_DL EB R DCB02DR0 2C # 6C AA AC ACC_DR1 EC RW DCB03DR1 2D W 6D AE ACC_DR0 ED RW DCB03DR2 2E RW 6E AE ACC_DR2 EF RW DB810DR1 30 # ACB00CR3 70 RW RDIOSIN B0 RW F1 DB DB810DR1	DBB01DR0	24	#	CMP_CR0	64	#		A4		DEC_DH	E4	RC
DBB01CR0 27 # 67 A7 DEC_CR1 E7 RW DCB02DR0 28 # 68 A8 MUL_X E8 W DCB02DR1 29 W 69 A9 MUL_Y E9 W DCB02DR2 2A RW 6A AA MUL_DH EA R DCB02CR0 2B # 6B AB MUL_DL EB R DCB03DR0 2C # 6C AC AC ACC_DR1 EC RW DCB03DR1 2D W 6D AD AC ACC_DR3 EE RW DCB03DR1 2D W 6E AE ACC_DR3 EE RW DCB03CR0 2F # 6F AF ACC_DR2 EF RW DB810DR1 30 # ACB00CR3 70 RW RDI0SYN B1 RW F1 DB810DR3 E RW F2	DBB01DR1	25	W	ASY_CR	65	#		A5		DEC_DL	E5	RC
DCB02DR0 28 # 68 A8 MUL_X E8 W DCB02DR1 29 W 69 A9 MUL_Y E9 W DCB02DR2 2A RW 6A AA MUL_DH EA R DCB02DR0 2B # 6B AA MUL_DH EA R DCB03DR0 2C # 6C AC ACC_DR1 EC RW DCB03DR1 2D W 6C AC ACC_DR3 EE RW DCB03DR1 2D W 6E AE ACC_DR3 EE RW DCB03DR1 2D W 6F AF ACC_DR2 EF RW DCB03CR0 2F # ACB00CR3 70 RW RDI0RI B0 RW F0 PD DB810DR1 31 W ACB00CR1 72 RW RDI0IS B2 RW F3 DBB11DR1 S ACB01C	DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DCB02DR1 29 W 69 A9 MUL_Y E9 W DCB02DR2 2A RW 6A AA MUL_DH EA R DCB02CR0 2B # 6B AB MUL_DL EB R DCB03DR0 2C # 6C AC ACC_DR1 EC RW DCB03DR1 2D W 6D AD ACC_DR0 ED RW DCB03DR1 2D W 6D AE ACC_DR0 ED RW DCB03DR2 2E RW 6E AF ACC_DR3 EE RW DCB03DR0 30 # ACB00CR3 70 RW RDIORI B0 RW F0 D DB810DR1 31 W ACB00CR1 72 RW RDIOS B2 RW F1 D D DB10R1 31 W ACB01CR2 73 RW RDIOS B2 RW F3					67			A7		DEC_CR1		
DCB02DR2 2A RW 6A AA MUL_DH EA R DCB02CR0 2B # 6B AB MUL_DL EB R DCB03DR0 2C # 6C AC AC ACC_DR1 EC RW DCB03DR1 2D W 6D AD ACC_DR0 ED RW DCB03DR2 2E RW 6E AE ACC_DR3 EE RW DCB03OR0 2F # 6F AE ACC_DR3 EE RW DB810DR0 30 # ACB00CR3 70 RW RDI0RI B0 RW F0 D DB810DR1 31 W ACB00CR1 72 RW RDI0SYN B1 RW F1 D DB810DR2 32 RW ACB00CR2 73 RW RDI0IT0 B3 RW F3 D DB811DR0 34 # ACB01CR0 75 <t< td=""><td></td><td>-</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>		-										
DCB02CR0 2B # 6B AB MUL_DL EB R DCB03DR0 2C # 6C AC AC ACC_DR1 EC RW DCB03DR1 2D W 6D AD AC ACC_DR0 ED RW DCB03DR2 2E RW 6E AE ACC_DR3 EE RW DCB03CR0 2F # 6F AF ACC_DR2 EF RW DB810DR0 30 # ACB00CR3 70 RW RDI0SI B0 RW F1 DB810DR1 31 W ACB00CR1 72 RW RDI0SI B2 RW F2 DB810DR2 32 RW ACB01CR3 74 RW RDI0IT0 B3 RW F3 DB811DR0 34 # ACB01CR1 75 RW RDI0R0 B5 RW F5 DB811DR1 35 W		-								_		
DCB03DR0 2C # 6C AC AC ACC_DR1 EC RW DCB03DR1 2D W 6D AD AD ACC_DR0 ED RW DCB03DR2 2E RW 6E AE ACC_DR3 EE RW DCB03CR0 2F # 6F AF ACC_DR2 EF RW DB810DR0 30 # ACB00CR3 70 RW RDI0RI B0 RW F0 PRW DB810DR1 31 W ACB00CR0 71 RW RDI0SIN B1 RW F1 PRW DB810DR2 32 RW ACB00CR1 72 RW RDI0SIN B1 RW F2 PRW DB810DR2 33 # ACB01CR1 72 RW RDI0SIN B2 RW F3 PRW DB810DR3 34 # ACB01CR2 73 RW RDI0LT0 B3 RW F4 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>_</td> <td></td> <td></td>										_		
DCB03DR1 2D W 6D AD AD ACC_DR0 ED RW DCB03DR2 2E RW 6E AE ACC_DR3 EE RW DCB03CR0 2F # 6F AF ACC_DR2 EF RW DBB10DR0 30 # ACB00CR3 70 RW RDIORI B0 RW F0 F0 DBB10DR1 31 W ACB00CR0 71 RW RDI0S B2 RW F1 F1 DBB10DR2 32 RW ACB00CR1 72 RW RDI0IS B2 RW F2 F3 DBB10DR0 33 # ACB01CR1 74 RW RDI0IT0 B3 RW F4 F4 DBB11DR0 34 # ACB01CR0 75 RW RDI0R00 B5 RW F5 F5 DBB11DR1 35 W ACB01CR1 76 RW RDI0R01 B6												
DCB03DR2 2E RW 6E AE AE ACC_DR3 EE RW DCB03CR0 2F # 6F AF ACC_DR2 EF RW DBB10DR0 30 # ACB00CR3 70 RW RDIORI B0 RW ACC_DR2 EF RW DBB10DR1 31 W ACB00CR0 71 RW RDIOSYN B1 RW F1 DBB10DR2 32 RW ACB00CR1 72 RW RDIOIS B2 RW F2 DBB10DR2 33 # ACB00CR2 73 RW RDIOIS B2 RW F3 DBB10R0 34 # ACB01CR3 74 RW RDIOLT0 B3 RW F4 DBB11DR1 35 W ACB01CR1 75 RW RDIOR00 B5 RW F5 DBB11DR1 35 W ACB01CR1												
DCB03CR0 2F # 6F AF AF ACC_DR2 EF RW DBB10DR0 30 # ACB00CR3 70 RW RDIORI B0 RW F0 F0 DBB10DR1 31 W ACB00CR0 71 RW RDIOSYN B1 RW F1 F0 DBB10DR2 32 RW ACB00CR1 72 RW RDIOIS B2 RW F2 F2 DBB10DR2 32 RW ACB00CR2 73 RW RDIOIS B2 RW F3 F3 DBB10CR0 33 # ACB01CR3 74 RW RDIOLT0 B3 RW F4 F4 DBB11DR1 35 W ACB01CR0 75 RW RDIORO1 B6 RW F6 F5 DBB11DR2 36 RW ACB01CR2 77 RW RDIORO1 B6 RW F6 F8 DCB12DR0 38<										_		
DBB10DR0 30 # ACB00CR3 70 RW RDIORI B0 RW F0 DBB10DR1 31 W ACB00CR0 71 RW RDIOSYN B1 RW F1 DBB10DR2 32 RW ACB00CR1 72 RW RDIOIS B2 RW F2 DBB10DR2 33 # ACB00CR2 73 RW RDIOIS B2 RW F3 DBB11DR0 34 # ACB01CR3 74 RW RDIOLT0 B3 RW F4 DBB11DR1 35 W ACB01CR0 75 RW RDIOR00 B5 RW F6 DBB11DR2 36 RW ACB01CR1 76 RW RDIOR01 B6 RW F6 DBB11DR2 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>_</td><td></td><td></td></t<>										_		
DBB10DR1 31 W ACB00CR0 71 RW RDIOSYN B1 RW F1 F1 DBB10DR2 32 RW ACB00CR1 72 RW RDIOIS B2 RW F2 DBB10CR0 33 # ACB00CR2 73 RW RDIOIS B2 RW F3 DBB10CR0 33 # ACB01CR3 74 RW RDIOLT0 B3 RW F3 DBB11DR0 34 # ACB01CR3 74 RW RDIOR00 B5 RW F4 DBB11DR1 35 W ACB01CR1 76 RW RDIOR00 B5 RW F6 DBB11DR2 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 RW RDI1SIN B8 RW F9 CDCB12DR1 39				ACB00CR3		RW	RDI0RI		RW			
DBB10CR0 33 # ACB00CR2 73 RW RDIOLT0 B3 RW F3 DBB11DR0 34 # ACB01CR3 74 RW RDIOLT1 B4 RW F4 DBB11DR1 35 W ACB01CR0 75 RW RDIORO0 B5 RW F5 DBB11DR2 36 RW ACB01CR1 76 RW RDIORO1 B6 RW F6 DBB11DR2 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DBB12DR0 38 # ACB02CR3 78 RW RDI1RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR2 7B RW RDI1SYN B9 RW F4 DCB12DR2 3A RW ACB02CR2 7B RW RDI1LT0 <td></td> <td></td> <td>W</td> <td></td> <td></td> <td></td> <td>RDI0SYN</td> <td></td> <td>RW</td> <td></td> <td></td> <td> </td>			W				RDI0SYN		RW			
DBB11DR0 34 # ACB01CR3 74 RW RDIOLT1 B4 RW F4 DBB11DR1 35 W ACB01CR0 75 RW RDIORO0 B5 RW F5 DBB11DR2 36 RW ACB01CR1 76 RW RDIORO1 B6 RW F6 DBB11DR2 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 RW RDI1RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RDI1SYN B9 RW F4 DCB12DR0 3B # ACB02CR2 7B RW RDI1SYN B9 RW F4 DCB12DR0 3B # ACB02CR2 7B RW RD11LT0			RW		72	RW		B2	RW		F2	
DBB11DR1 35 W ACB01CR0 75 RW RDI0RO0 B5 RW F5 DBB11DR2 36 RW ACB01CR1 76 RW RDI0RO1 B6 RW F6 DBB11DR2 36 RW ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 RW RDI1RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RDI1SYN B9 RW FA DCB12DR0 3B # ACB02CR2 7B RW RDI1IS BA RW FA DCB12DR0 3B # ACB03CR3 7C RW RDI1LT0 BB RW FB DCB13DR0 3C # ACB03CR0 7D RW RDI1RO0		33										
DBB11DR2 36 RW ACB01CR1 76 RW RDI0RO1 B6 RW F6 DBB11CR0 37 # ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 RW RDI1RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RDI1SYN B9 RW FA DCB12DR0 3B # ACB02CR2 7B RW RDI1SYN B9 RW FA DCB12DR0 3B # ACB02CR2 7B RW RDI1ITO BB RW FB DCB13DR0 3C # ACB03CR3 7C RW RDI1LT1 BC RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1RO0												
DBB11CR0 37 # ACB01CR2 77 RW B7 CPU_F F7 RL DCB12DR0 38 # ACB02CR3 78 RW RD11RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RD11SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RD11SYN B9 RW FA DCB12DR2 3A RW ACB02CR1 7A RW RD11SYN B9 RW FA FA DCB12DR2 3B # ACB02CR2 7B RW RD11SYN BB RW FA FB DCB13DR0 3C # ACB03CR3 7C RW RD11LT0 BB RW FC FC TO DCB13DR1 3D W ACB03CR0 7D RW RD11R00 BD RW FD FD TO DCB13DR2 3E RW ACB03CR1 7E RW RD11R01												
DCB12DR0 38 # ACB02CR3 78 RW RDI1RI B8 RW F8 DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RDI1SYN B9 RW FA DCB12DR2 3A RW ACB02CR2 7B RW RDI1IS BA RW FA DCB12DR0 3B # ACB02CR2 7B RW RDI1LT0 BB RW FB DCB13DR0 3C # ACB03CR3 7C RW RDI1LT1 BC RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1RO0 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RDI1RO1 BE RW CPU_SCR1 FE #							RDI0RO1		RW			
DCB12DR1 39 W ACB02CR0 79 RW RDI1SYN B9 RW F9 DCB12DR2 3A RW ACB02CR1 7A RW RDI1S BA RW FA DCB12CR0 3B # ACB02CR2 7B RW RDI1LT0 BB RW FB DCB13DR0 3C # ACB03CR3 7C RW RDI1LT1 BC RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1RO0 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RDI1RO1 BE RW CPU_SCR1 FE #		-					DDI4D!			CPU_F		RL
DCB12DR2 3A RW ACB02CR1 7A RW RDI1IS BA RW FA DCB12CR0 3B # ACB02CR2 7B RW RDI1IS BB RW FB DCB13DR0 3C # ACB03CR3 7C RW RDI1LT0 BB RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1R00 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RD11R01 BE RW CPU_SCR1 FE #												
DCB12CR0 3B # ACB02CR2 7B RW RDI1LT0 BB RW FB DCB13DR0 3C # ACB03CR3 7C RW RDI1LT1 BC RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1R00 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RD1R01 BE RW CPU_SCR1 FE #								-				
DCB13DR0 3C # ACB03CR3 7C RW RDI1LT1 BC RW FC DCB13DR1 3D W ACB03CR0 7D RW RDI1R00 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RD1R01 BE RW CPU_SCR1 FE #												
DCB13DR1 3D W ACB03CR0 7D RW RDI1R00 BD RW FD DCB13DR2 3E RW ACB03CR1 7E RW RDI1R01 BE RW CPU_SCR1 FE #												
DCB13DR2 3E RW ACB03CR1 7E RW RDI1RO1 BE RW CPU_SCR1 FE #												
										CPU SCR1		#
	DCB13CR0											

Blank fields are Reserved and should not be accessed.



This chapter presents the DC and AC electrical specifications of the CY8C27x43 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for $-40^{\circ}C \le T_A \le 85^{\circ}C$ and $T_J \le 100^{\circ}C$, except where noted. Specifications for devices running at greater than 12 MHz are valid for $-40^{\circ}C \le T_A \le 70^{\circ}C$ and $T_J \le 82^{\circ}C$.

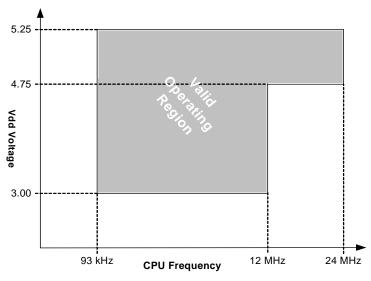


Figure 3-1. Voltage versus CPU Frequency

The following table lists the units of measure that are used in this chapter.

Table 3-1: Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	μW	micro watts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nano ampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	Ω	ohm
MHz	megahertz	pА	pico ampere
MΩ	megaohm	pF	pico farad
μA	micro ampere	рр	peak-to-peak
μF	micro farad	ppm	parts per million
μH	micro henry	ps	picosecond
μs	microsecond	sps	samples per second
μV	micro volts	σ	sigma: one standard deviation
μVrms	micro volts root-mean-square	V	volts

3.1 Absolute Maximum Ratings

Table 3-2. Absolute Maximum Ratings

Symbol	Description	Min	Тур	Max	Units	Notes
T _{STG}	Storage Temperature	-55	-	+100	°C	Higher storage temperatures will reduce data retention time.
T _A	Ambient Temperature with Power Applied	-40	-	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	-	+6.0	V	
V _{IO}	DC Input Voltage	Vss- 0.5	-	Vdd + 0.5	V	
-	DC Voltage Applied to Tri-state	Vss - 0.5	-	Vdd + 0.5	V	
I _{MIO}	Maximum Current into any Port Pin	-25	-	+50	mA	
I _{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	-	+50	mA	
ESD	Electro Static Discharge Voltage	2000	-	-	V	Human Body Model ESD
-	Latch-up Current	-	-	200	mA	

3.2 Operating Temperature

Table 3-3. Operating Temperature

Symbol	Description	Min	Тур	Max	Units	Notes
T _A	Ambient Temperature	-40	-	+85	°C	
TJ	Junction Temperature	-40	-	+100		The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 41. The user must limit the power consumption to comply with this requirement.

3.3 DC Electrical Characteristics

3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-4. DC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
Vdd	Supply Voltage	3.00	-	5.25	V	
I _{DD}	Supply Current	-	5	8	mA	Conditions are Vdd = 5.0V, $T_A = 25 \ ^{o}C$, CPU = 3 MHz, 48 MHz = Disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I _{DD3}	Supply Current	-	3.3	6.0	mA	Conditions are Vdd = $3.3V$, T _A = $25 ^{\circ}$ C, CPU = 3 MHz, 48 MHz = Disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I _{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT. ^a	-	3	6.5	μΑ	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 $^oC \leq T_A \leq ~55 ~^oC.$
I _{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature. ^a	-	4	25	μΑ	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 ^{o}C < T_A $\leq~85$ $^{o}C.$
I _{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal. ^a	-	4	7.5	μΑ	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C $\leq T_A \leq$ 55 °C.
I _{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature. ^a	-	5	26	μΑ	Conditions are with properly loaded, 1 μW max, 32.768 kHz crystal. Vdd = 3.3V, 55 oC < T_A \leq 85 $^oC.$
V_{REF}	Reference Voltage (Bandgap) for Silicon A ^b	1.275	1.300	1.325	V	Trimmed for appropriate Vdd.
V_{REF}	Reference Voltage (Bandgap) for Silicon B ^b	1.280	1.300	1.320	V	Trimmed for appropriate Vdd.

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

b. Refer to the Ordering Information chapter on page 42.

3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table	3-5. D	C GPIO	Specifications
-------	--------	--------	----------------

Symbol	Description	Min	Тур	Max	Units	Notes
R _{PU}	Pull up Resistor	4	5.6	8	kΩ	
R _{PD}	Pull down Resistor	4	5.6	8	kΩ	
V _{OH}	High Output Level	Vdd - 1.0	-	-	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V _{OL}	Low Output Level	-	-	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V _{IL}	Input Low Level	-	-	0.8	V	Vdd = 3.0 to 5.25
V _{IH}	Input High Level	2.1	-		V	Vdd = 3.0 to 5.25
V _H	Input Hysterisis	-	60	-	mV	
IIL	Input Leakage (Absolute Value)	-	1	-	nA	Gross tested to 1 µA.
C _{IN}	Capacitive Load on Pins as Input	-	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C _{OUT}	Capacitive Load on Pins as Output	-	3.5	10	pF	Package and pin dependent. Temp = 25° C.

3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input Offset Voltage (absolute value)		1			
	Power = Low, Opamp Bias = High	-	1.6	10	mV	
	Power = Medium, Opamp Bias = High	-	1.3	8	mV	
	Power = High, Opamp Bias = High	-	1.2	7.5	mV	
TCV _{OSOA}	Average Input Offset Voltage Drift	-	7.0	35.0	μV/ºC	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	-	20	-	pА	Gross tested to 1 µA.
CINOA	Input Capacitance (Port 0 Analog Pins)	-	4.5	9.5	pF	Package and pin dependent. Temp = 25 ^o C.
V _{CMOA}	Common Mode Voltage Range	0.0	-	Vdd	V	The common-mode input voltage range is mea-
	Common Mode Voltage Range (high power or high opamp bias)	0.5	-	Vdd - 0.5		sured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRR _{OA}	Common Mode Rejection Ratio		-	-	dB	Specification is applicable at high power. For all
	Power = Low	60				other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Medium	60				opanip blas), minimum is oo ab.
	Power = High	60				
G _{OLOA}	Open Loop Gain		-	-	dB	Specification is applicable at high power. For all
	Power = Low	60				other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Medium	60				opanip blas), minimum is oo ab.
	Power = High	80				
V _{OHIGHOA}	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	-	-	V	
	Power = Medium	Vdd - 0.2	-	-	V	
	Power = High	Vdd - 0.5	-	-	V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low	-	-	0.2	V	
	Power = Medium	-	-	0.2	V	
	Power = High	-	-	0.5	V	
I _{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	-	150	200	μΑ	
	Power = Low, Opamp Bias = High	-	300	400	μΑ	
	Power = Medium, Opamp Bias = Low	-	600	800	μΑ	
	Power = Medium, Opamp Bias = High	-	1200	1600	μΑ	
	Power = High, Opamp Bias = Low	-	2400	3200	μΑ	
	Power = High, Opamp Bias = High	-	4600	6400	μΑ	
PSRR _{OA}	Supply Voltage Rejection Ratio	60	-	-	dB	$\begin{array}{l} OV \leq V_{IN} \leq (Vdd - 2.25) \text{ or} \\ (Vdd - 1.25V) \leq V_{IN} \leq Vdd. \end{array}$

Table 3-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
V _{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	-	1.65	10	mV	
	Power = Medium, Opamp Bias = High	-	1.32	8	mV	
	High Power is 5 Volts Only					
TCV _{OSOA}	Average Input Offset Voltage Drift	-	7.0	35.0	μV/ºC	
I _{EBOA}	Input Leakage Current (Port 0 Analog Pins)	-	20	-	pА	Gross tested to 1 µA.
CINOA	Input Capacitance (Port 0 Analog Pins)	-	4.5	9.5	pF	Package and pin dependent. Temp = 25° C.
V _{CMOA}	Common Mode Voltage Range	0.2	-	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
CMRR _{OA}	Common Mode Rejection Ratio		-	-	dB	Specification is applicable at high power. For
	Power = Low	50				all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Medium	50				opamp blas), minimum is oo ub.
	Power = High	50				
G _{OLOA}	Open Loop Gain		-	-	dB	Specification is applicable at high power. For
	Power = Low	60				all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Medium	60				oparity bias), minimum is oo ab.
	Power = High	80				
V _{OHIGHOA}	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	-	-	V	
	Power = Medium	Vdd - 0.2	-	-	V	
	Power = High is 5V only	Vdd - 0.2	-	-	V	
V _{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low	-	-	0.2	V	
	Power = Medium	-	-	0.2	V	
	Power = High	-	-	0.2	V	
I _{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	-	150	200	μΑ	
	Power = Low, Opamp Bias = High	-	300	400	μΑ	
	Power = Medium, Opamp Bias = Low	-	600	800	μΑ	
	Power = Medium, Opamp Bias = High	-	1200	1600	μΑ	
	Power = High, Opamp Bias = Low	-	2400	3200	μΑ	
	Power = High, Opamp Bias = High		4600	6400	μΑ	
PSRR _{OA}	Supply Voltage Rejection Ratio	50	-	-	dB	$\begin{array}{l} 0V \leq V_{IN} \leq (Vdd \mbox{ - } 2.25) \mbox{ or } \\ (Vdd \mbox{ - } 1.25V) \leq V_{IN} \leq Vdd. \end{array}$

3.3.5 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq 85^{\circ}$ C, or 3.0V to 3.6V and -40°C $\leq T_A \leq 85^{\circ}$ C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-10.	DC S	witch I	Mode	Pump	(SMP)	S	pecifications
14010 0 101			in o a o		(e,	-	poontoationo

Symbol	Description	Min	Тур	Max	Units	Notes
V _{PUMP} 5V	5V Output Voltage	4.75	5.0	5.25	V	Configuration of footnote ^a . Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V _{PUMP} 3V	3V Output Voltage	3.00	3.25	3.60	V	Configuration of footnote ^a . Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I _{PUMP}	Available Output Current					Configuration of footnote ^a .
	V _{BAT} = 1.5V, V _{PUMP} = 3.25V	8	-	-	mA	SMP trip voltage is set to 3.25V.
	V_{BAT} = 1.8V, V_{PUMP} = 5.0V	5	-	-	mA	SMP trip voltage is set to 5.0V.
V _{BAT} 5V	Input Voltage Range from Battery	1.8	-	5.0	V	Configuration of footnote ^a . SMP trip voltage is set to 5.0V.
V _{BAT} 3V	Input Voltage Range from Battery	1.0	-	3.3	V	Configuration of footnote ^a . SMP trip voltage is set to 3.25V.
VBATSTART	Minimum Input Voltage from Battery to Start Pump	1.1	-	-	V	Configuration of footnote ^a .
ΔV_{PUMP_Line}	Line Regulation (over V _{BAT} range)	-	5	-	%V _O	Configuration of footnote ^a . V _O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26.
ΔV_{PUMP_Load}	Load Regulation	_	5	_	%V _O	Configuration of footnote ^a . V _O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	-	100	-	mVpp	Configuration of footnote ^a . Load is 5mA.
E ₃	Efficiency	35	50	-	%	Configuration of footnote ^a . Load is 5 mA. SMP trip voltage is set to 3.25V.
F _{PUMP}	Switching Frequency	-	1.3	-	MHz	
DC _{PUMP}	Switching Duty Cycle	-	50	-	%	

a. $L_1 = 2 \mu H$ inductor, $C_1 = 10 \mu F$ capacitor, $D_1 =$ Schottky diode. See Figure 3-2.

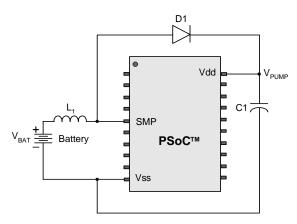


Figure 3-2. Basic Switch Mode Pump Circuit

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Symbol	Description	Min	Тур	Мах	Units	Notes
F _{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6 ^a	MHz	Trimmed. Utilizing factory trim values.
F _{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6 ^{a,b}	MHz	Trimmed. Utilizing factory trim values.
F _{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3 ^{b,c}	MHz	Trimmed. Utilizing factory trim values.
F _{48M}	Digital PSoC Block Frequency	0	48	49.2 ^{a,b,d}	MHz	Refer to the AC Digital Block Specifications below.
F _{24M}	Digital PSoC Block Frequency	0	24	24.6 ^{b, d}	MHz	
F _{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F _{32K2}	External Crystal Oscillator	-	32.768	-	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F _{PLL}	PLL Frequency	-	23.986	-	MHz	Multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	-	-	600	ps	
T _{PLLSLEW}	PLL Lock Time	0.5	-	10	ms	
T _{PLLSLEWS} . LOW	PLL Lock Time for Low Gain Setting	0.5	-	50	ms	
T _{OS}	External Crystal Oscillator Startup to 1%	-	1700	2620	ms	
T _{OSACC}	External Crystal Oscillator Startup to 100 ppm	-	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T _{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V \leq Vdd \leq 5.5V, -40 $^{\circ}C \leq T_{A} \leq 85 ^{\circ}C$.
Jitter32k	32 kHz Period Jitter	-	100		ns	
T _{XRST}	External Reset Pulse Width	10	-	-	μs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	-	50	-	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2 ^{a,c}	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	-	600		ps	
F _{MAX}	Maximum frequency of signal on row input or row output.	-	-	12.3	MHz	
T _{RAMP}	Supply Ramp Time	0	-	-	μs	

a. 4.75V < Vdd < 5.25V.

b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.

c. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

d. See the individual user module data sheets for information on maximum frequencies for user modules.

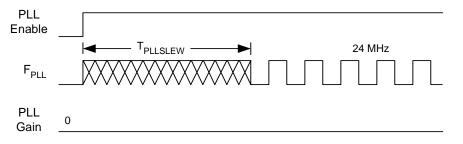


Figure 3-3. PLL Lock Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq 85^{\circ}$ C, or 3.0V to 3.6V and -40°C $\leq T_A \leq 85^{\circ}$ C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 3-20. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	-	-	3.9	μs	
	Power = Medium, Opamp Bias = High	-	-	0.72	μs	
	Power = High, Opamp Bias = High	-	-	0.62	μs	
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	-	-	5.9	μs	
	Power = Medium, Opamp Bias = High	-	-	0.92	μs	
	Power = High, Opamp Bias = High	-	-	0.72	μs	
SR _{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	-	-	V/µs	
	Power = Medium, Opamp Bias = High	1.7	-	-	V/µs	
	Power = High, Opamp Bias = High	6.5	-	-	V/µs	
SR _{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	-	-	V/µs	
	Power = Medium, Opamp Bias = High	0.5	-	-	V/µs	
	Power = High, Opamp Bias = High	4.0	-	-	V/µs	
BW _{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.75	-	-	MHz	
	Power = Medium, Opamp Bias = High	3.1	-	-	MHz	
	Power = High, Opamp Bias = High	5.4	-	-	MHz	
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	-	100	-	nV/rt-Hz	

Table 3-21. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	-	-	3.92	μs	
	Power = Low, Opamp Bias = High	-	-	0.72	μs	
T _{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	-	-	5.41	μs	
	Power = Medium, Opamp Bias = High	-	-	0.72	μs	
SR _{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	-	-	V/µs	
	Power = Medium, Opamp Bias = High	2.7	-	-	V/µs	
SR _{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	-	-	V/µs	
	Power = Medium, Opamp Bias = High	1.8	-	-	V/µs	
BW _{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	-	-	MHz	
	Power = Medium, Opamp Bias = High	2.8	-	-	MHz	
E _{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	-	100	-	nV/rt-Hz	

3.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C $\leq T_A \leq 85^{\circ}$ C, or 3.0V to 3.6V and -40°C $\leq T_A \leq 85^{\circ}$ C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Symbol	Description	Min	Тур	Max	Units	Notes
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	-	-	2.5	μs	
	Power = High	-	-	2.5	μs	
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	-	-	2.2	μs	
	Power = High	-	-	2.2	μs	
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.65	-	-	V/µs	
	Power = High	0.65	-	-	V/µs	
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.65	-	-	V/µs	
	Power = High	0.65	-	-	V/µs	
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load					
	Power = Low	0.8	-	-	MHz	
	Power = High	0.8	-	-	MHz	
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load					
	Power = Low	300	-	-	kHz	
	Power = High	300	-	-	kHz	

Table 3-24. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	-	-	3.8	μs	
	Power = High	-	-	3.8	μs	
T _{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	-	-	2.6	μs	
	Power = High	-	-	2.6	μs	
SR _{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.5	-	-	V/µs	
	Power = High	0.5	-	-	V/µs	
SR _{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.5	-	-	V/µs	
	Power = High	0.5	-	-	V/µs	
BW _{OB}	Small Signal Bandwidth, 20mV _{pp} , 3dB BW, 100pF Load					
	Power = Low	0.7	-	-	MHz	
	Power = High	0.7	-	-	MHz	
BW _{OB}	Large Signal Bandwidth, 1V _{pp} , 3dB BW, 100pF Load					
	Power = Low	200	-	-	kHz	
	Power = High	200	-	-	kHz	

3.4.6 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-25. 5V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{OSCEXT}	Frequency	0.093	-	24.6	MHz	
-	High Period	20.6	-	5300	ns	
-	Low Period	20.6	-	-	ns	
-	Power Up IMO to Switch	150	-	-	μs	

Table 3-26. 3.3V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
FOSCEXT	Frequency with CPU Clock divide by 1 ^a	0.093	-	12.3	MHz	
FOSCEXT	Frequency with CPU Clock divide by 2 or greater ^b	0.186	-	24.6	MHz	
-	High Period with CPU Clock divide by 1	41.7	-	5300	ns	
-	Low Period with CPU Clock divide by 1	41.7	-	-	ns	
-	Power Up IMO to Switch	150	-	-	μs	

a. Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.

b. If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.

3.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C \leq T_A \leq 85°C, or 3.0V to 3.6V and -40°C \leq T_A \leq 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-27. AC Programming Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
T _{RSCLK}	Rise Time of SCLK	1	-	20	ns	
T _{FSCLK}	Fall Time of SCLK	1	-	20	ns	
T _{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	-	-	ns	
T _{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	-	-	ns	
F _{SCLK}	Frequency of SCLK	0	-	8	MHz	
T _{ERASEB}	Flash Erase Time (Block)	-	10	-	ms	
T _{WRITE}	Flash Block Write Time	-	10	-	ms	
T _{DSCLK}	Data Out Delay from Falling Edge of SCLK	-	-	45	ns	Vdd > 3.6
T _{DSCLK3}	Data Out Delay from Falling Edge of SCLK	-	-	50	ns	$3.0 \leq V dd \leq 3.6$

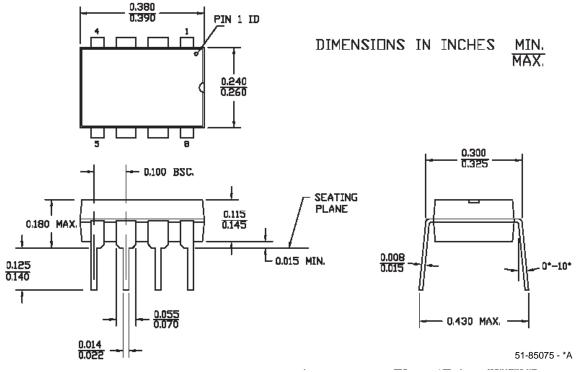
4. Packaging Information



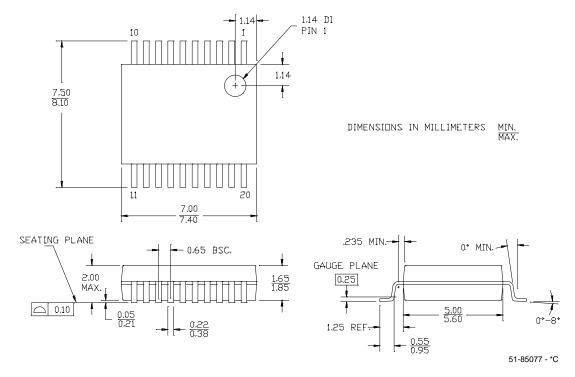
This chapter illustrates the packaging specifications for the CY8C27x43 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

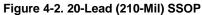
Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

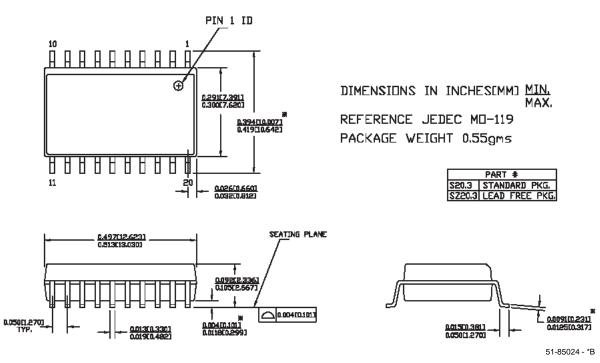
4.1 Packaging Dimensions

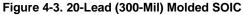












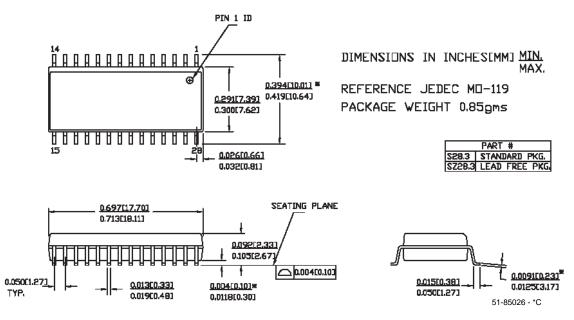


Figure 4-6. 28-Lead (300-Mil) Molded SOIC

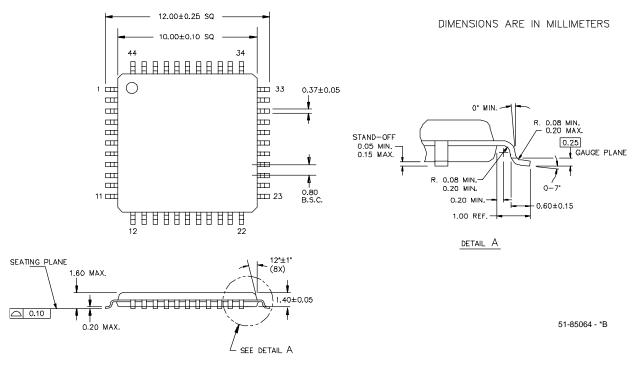


Figure 4-7. 44-Lead TQFP



The following table lists the CY8C27x43 PSoC device family's key package features and ordering codes.

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C27x43 Silicon B – These p any digital block to be the decima											
the analog reference is enhanced										, accure	
8 Pin (300 Mil) DIP	CY8C27143-24PXI	16	256	No	-40C to +85C	8	12	6	4	4	No
20 Pin (210 Mil) SSOP	CY8C27243-24PVXI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27243-24PVXIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (300 Mil) SOIC	CY8C27243-24SXI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin 300 Mil) SOIC (Tape and Reel)	CY8C27243-24SXIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
28 Pin (300 Mil) DIP	CY8C27443-24PXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C27443-24PVXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27443-24PVXIT	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (300 Mil) SOIC	CY8C27443-24SXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C27443-24SXIT	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
44 Pin TQFP	CY8C27543-24AXI	16	256	Yes	-40C to +85C	8	12	40	12	4	Yes
44 Pin TQFP (Tape and Reel)	CY8C27543-24AXIT	16	256	Yes	-40C to +85C	8	12	40	12	4	Yes
48 Pin (300 Mil) SSOP	CY8C27643-24PVXI	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8C27643-24PVXIT	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) MLF	CY8C27643-24LFXI	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) MLF (Tape and Reel)	CY8C27643-24LFXIT	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
CY8C27x43 Silicon A – Silicon	A is not recommended for r	new desi	gns.								
8 Pin (300 Mil) DIP	CY8C27143-24PI	16	256	No	-40C to +85C	8	12	6	4	4	No
20 Pin (210 Mil) SSOP	CY8C27243-24PVI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27243-24PVIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (300 Mil) SOIC	CY8C27243-24SI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin 300 Mil) SOIC (Tape and Reel)	CY8C27243-24SIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
28 Pin (300 Mil) DIP	CY8C27443-24PI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C27443-24PVI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
/ /	_	-				-	1		1		L