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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27243-24pvit

processor. The CPU utilizes an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

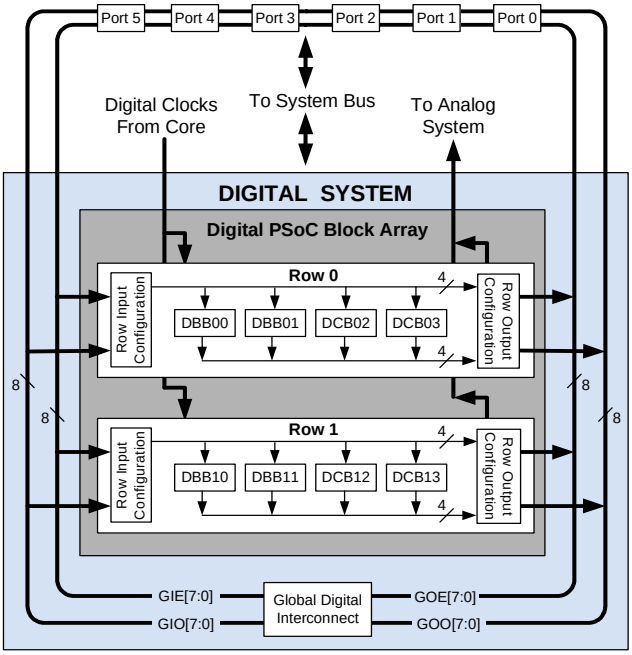
Memory encompasses 16 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of 8 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.



Digital System Block Diagram

Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 2)
- SPI master and slave (up to 2)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 2)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

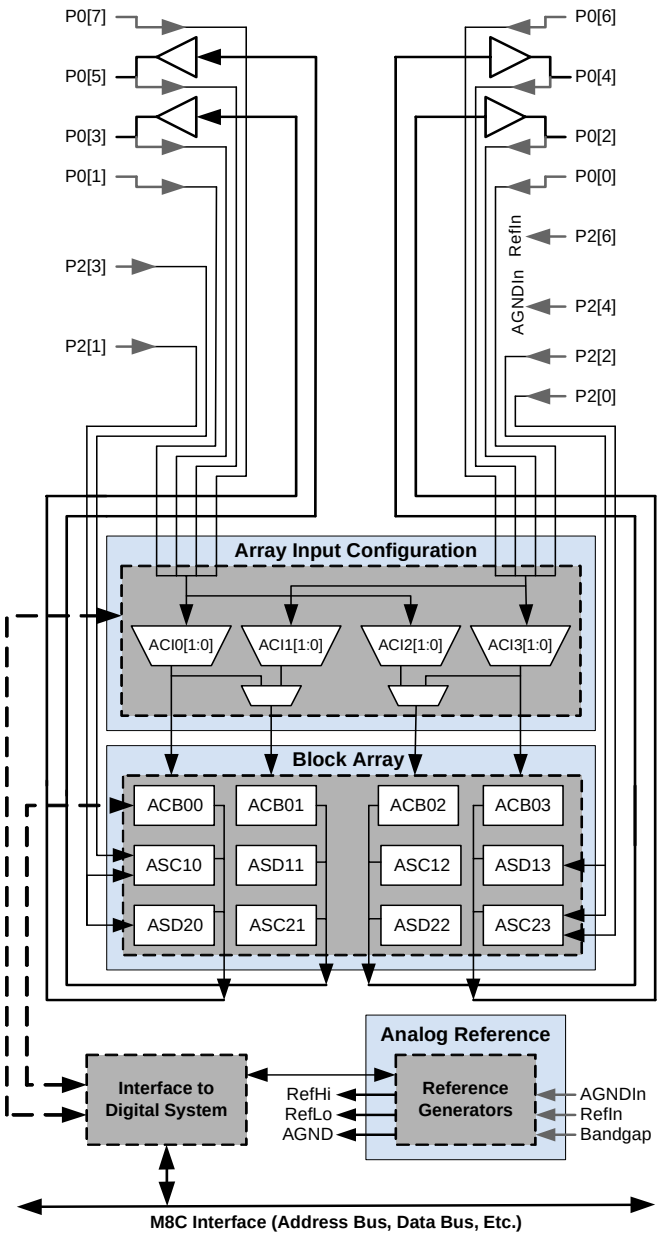
Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 3.

The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in the figure below.



Analog System Block Diagram

Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, switch mode pump, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are presented below.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- A multiply accumulate (MAC) provides a fast 8-bit multiplier with 32-bit accumulate, to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low Voltage Detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 3 analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is shown in the second row of the table.

PSoC Device Characteristics

PSoC Part Number	Digital IO	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks
CY8C29x66	up to 64	4	16	12	4	4	12
CY8C27x43	**up to 44**	**2**	**8**	**12**	**4**	**4**	**12**
CY8C24x23	up to 24	1	4	12	2	2	6
CY8C24x23A	up to 24	1	4	12	2	2	6
CY8C22x13	up to 16	1	4	8	1	1	3

PSoC Designer Software Subsystems

Device Editor

The Device Editor subsystem allows the user to select different onboard analog and digital components called user modules using the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

PSoC Designer sets up power-on initialization tables for selected PSoC block configurations and creates source code for an application framework. The framework contains software to operate the selected components and, if the project uses more than one operating configuration, contains routines to switch between different sets of PSoC block configurations at run time. PSoC Designer can print out a configuration sheet for a given project configuration for use during application programming in conjunction with the Device Data Sheet. Once the framework is generated, the user can add application-specific code to flesh out the framework. It's also possible to change the selected components and regenerate the framework.

Design Browser

The Design Browser allows users to select and import preconfigured designs into the user's project. Users can easily browse a catalog of preconfigured designs to facilitate time-to-design. Examples provided in the tools include a 300-baud modem, LIN Bus master and slave, fan controller, and magnetic card reader.

Application Editor

In the Application Editor you can edit your C language and Assembly language source code. You can also assemble, compile, link, and build.

Assembler. The macro assembler allows the assembly code to be merged seamlessly with C code. The link libraries automatically use absolute addressing or can be compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compiler. A C language compiler is available that supports Cypress MicroSystems' PSoC family devices. Even if you have never worked in the C language before, the product quickly allows you to create complete C programs for the PSoC family devices.

The embedded, optimizing C compiler provides all the features of C tailored to the PSoC architecture. It comes complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing the designer to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of the parallel or USB port. The base unit is universal and will operate with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

1. Pin Information

This chapter describes, lists, and illustrates the CY8C27x43 PSoC device pins and pinout configurations.

1.1 Pinouts

The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

1.1.1 8-Pin Part Pinout

Table 1-1. 8-Pin Part Pinout (PDIP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	IO	P0[5]	Analog column mux input and column output.
2	IO	IO	P0[3]	Analog column mux input and column output.
3	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
4	Power		Vss	Ground connection.
5	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
6	IO	IO	P0[2]	Analog column mux input and column output.
7	IO	IO	P0[4]	Analog column mux input and column output.
8	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27143 8-Pin PSoC Device

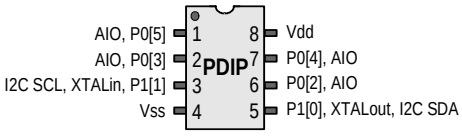
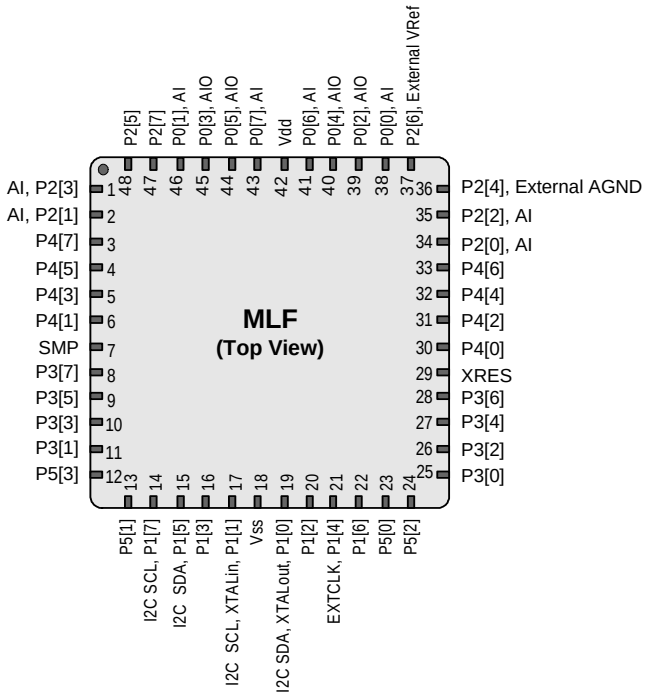


Table 1-6. 48-Pin Part Pinout (MLF*)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input.
2	IO	I	P2[1]	Direct switched capacitor block input.
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL)
15	IO		P1[5]	I2C Serial Data (SDA)
16	IO		P1[3]	
17	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK)
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34	IO	I	P2[0]	Direct switched capacitor block input.
35	IO	I	P2[2]	Direct switched capacitor block input.
36	IO		P2[4]	External Analog Ground (AGND)
37	IO		P2[6]	External Voltage Reference (VRef)
38	IO	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42	Power		Vdd	Supply voltage.
43	IO	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	IO		P2[5]	

CY8C27643 48-Pin PSoC Device



LEGEND: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to ground (Vss).

2. Register Reference

This chapter lists the registers of the CY8C27x43 PSoC device. For detailed register information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

2.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

3.3 DC Electrical Characteristics

3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-4. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.00	–	5.25	V	
I_{DD}	Supply Current	–	5	8	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, 48 MHz = Disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{DD3}	Supply Current	–	3.3	6.0	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, 48 MHz = Disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[a]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ T_A ≤ 55 °C.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[a]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < T_A ≤ 85 °C.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[a]	–	4	7.5	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, -40 °C ≤ T_A ≤ 55 °C.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[a]	–	5	26	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. Vdd = 3.3V, 55 °C < T_A ≤ 85 °C.
V_{REF}	Reference Voltage (Bandgap) for Silicon A [b]	1.275	1.300	1.325	V	Trimmed for appropriate Vdd.
V_{REF}	Reference Voltage (Bandgap) for Silicon B [b]	1.280	1.300	1.320	V	Trimmed for appropriate Vdd.

a. Standby current includes all functions (POR, LVD, WDT, Sleep Time) needed for reliable system operation. This should be compared with devices that have similar functions enabled.

b. Refer to the Ordering Information chapter on page 42.

3.3.2 DC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-5. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])).
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

Table 3-7. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value)					
	Power = Low, Opamp Bias = High	–	1.65	10	mV	
	Power = Medium, Opamp Bias = High	–	1.32	8	mV	
	High Power is 5 Volts Only					
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
$CMRR_{OA}$	Common Mode Rejection Ratio		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	50				
	Power = Medium	50				
	Power = High	50				
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
	Power = High	80				
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	–	–	V	
	Power = Medium	Vdd - 0.2	–	–	V	
	Power = High is 5V only	Vdd - 0.2	–	–	V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals)					
	Power = Low	–	–	0.2	V	
	Power = Medium	–	–	0.2	V	
	Power = High	–	–	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	µA	
	Power = Low, Opamp Bias = High	–	300	400	µA	
	Power = Medium, Opamp Bias = Low	–	600	800	µA	
	Power = Medium, Opamp Bias = High	–	1200	1600	µA	
	Power = High, Opamp Bias = Low	–	2400	3200	µA	
	Power = High, Opamp Bias = High	–	4600	6400	µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	50	–	–	dB	$0V \le V_{IN} \le (Vdd - 2.25)$ or $(Vdd - 1.25V) \le V_{IN} \le Vdd$.

3.3.5 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-10. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP} 5V	5V Output Voltage	4.75	5.0	5.25	V	Configuration of footnote [a]. Average, neglecting ripple. SMP trip voltage is set to 5.0V.
V_{PUMP} 3V	3V Output Voltage	3.00	3.25	3.60	V	Configuration of footnote [a]. Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I_{PUMP}	Available Output Current V_{BAT} = 1.5V, V_{PUMP} = 3.25V V_{BAT} = 1.8V, V_{PUMP} = 5.0V	 8 5	 – –	 – –	 mA mA	Configuration of footnote [a]. SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V.
V_{BAT}5V	Input Voltage Range from Battery	1.8	–	5.0	V	Configuration of footnote [a]. SMP trip voltage is set to 5.0V.
V_{BAT}3V	Input Voltage Range from Battery	1.0	–	3.3	V	Configuration of footnote [a]. SMP trip voltage is set to 3.25V.
$V_{BATSTART}$	Minimum Input Voltage from Battery to Start Pump	1.1	–	–	V	Configuration of footnote [a].
ΔV_{PUMP_Line}	Line Regulation (over V_{BAT} range)	–	5	–	$\%V_O$	Configuration of footnote [a]. V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26.
ΔV_{PUMP_Load}	Load Regulation	–	5	–	$\%V_O$	Configuration of footnote [a]. V_O is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26.
ΔV_{PUMP_Ripple}	Output Voltage Ripple (depends on capacitor/load)	–	100	–	mVpp	Configuration of footnote [a]. Load is 5mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote [a]. Load is 5 mA. SMP trip voltage is set to 3.25V.
F_{PUMP}	Switching Frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching Duty Cycle	–	50	–	%	

a. L_1 = 2 µH inductor, C_1 = 10 µF capacitor, D_1 = Schottky diode. See Figure 3-2.

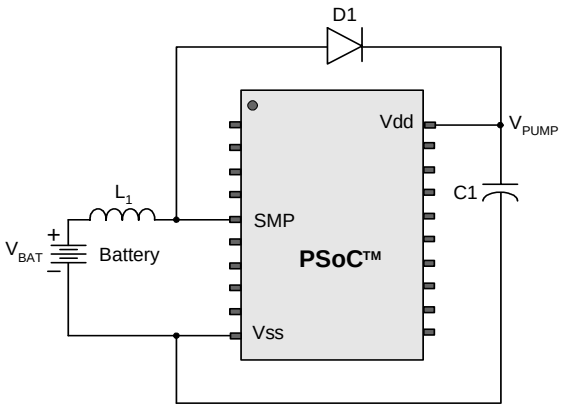


Figure 3-2. Basic Switch Mode Pump Circuit

3.3.6 DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 3-11. Silicon Revision A – 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.274	1.30	1.326	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.030	Vdd/2 - 0.004	Vdd/2 + 0.003	V
–	AGND = 2 x BandGap[a]	2 x BG - 0.043	2 x BG - 0.010	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a]	P2[4] - 0.013	P2[4]	P2[4] + 0.014	V
–	AGND = BandGap[a]	BG - 0.009	BG	BG + 0.009	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.018	1.6 x BG	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.140	Vdd/2 + BG - 0.018	Vdd/2 + BG + 0.103	V
–	RefHi = 3 x BandGap	3 x BG - 0.112	3 x BG - 0.018	3 x BG + 0.076	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6] + 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.051	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.098	V
–	RefLo = BandGap	BG - 0.082	BG + 0.023	BG + 0.129	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 3-12. Silicon Revision B – 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.030	Vdd/2	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[a]	2 x BG - 0.043	2 x BG	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[a]	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[a]	BG - 0.009	BG	BG + 0.009	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.018	1.6 x BG	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.1	Vdd/2 + BG - 0.01	Vdd/2 + BG + 0.1	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG - 0.01	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.06	2 x BG + P2[6] - 0.01	2 x BG + P2[6] + 0.06	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.06	P2[4] + BG - 0.01	P2[4] + BG + 0.06	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.06	P2[4] + P2[6] - 0.01	P2[4] + P2[6] + 0.06	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.06	3.2 x BG - 0.01	3.2 x BG + 0.06	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.051	Vdd/2 - BG + 0.01	Vdd/2 - BG + 0.06	V
–	RefLo = BandGap	BG - 0.06	BG + 0.01	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.04	2 x BG - P2[6] + 0.01	2 x BG - P2[6] + 0.04	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.01	P2[4] - BG + 0.056	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.056	P2[4] - P2[6] + 0.01	P2[4] - P2[6] + 0.056	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Table 3-13. Silicon Revision A – 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.274	1.30	1.326	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.027	Vdd/2 - 0.003	Vdd/2 + 0.002	V
–	AGND = 2 x BandGap[a]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[a]	BG - 0.009	BG	BG + 0.009	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.018	1.6 x BG	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4] - P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Note See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.

Table 3-14. Silicon Revision B – 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[a]	Vdd/2 - 0.027	Vdd/2	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[a]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4]	P2[4] + 0.009	V
–	AGND = BandGap[a]	BG - 0.009	BG	BG + 0.009	V
–	AGND = 1.6 x BandGap[a]	1.6 x BG - 0.018	1.6 x BG	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[a]	-0.034	0.000	0.034	mV
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.06	P2[4] + P2[6] - 0.01	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4] - P2[6] + 0.01	P2[4] - P2[6] + 0.048	V

a. AGND tolerance includes the offsets of the local buffer in the PSoC block.

Note See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.

3.3.7 DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-15. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

3.3.8 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register. See the *PSoC Mixed Signal Array Technical Reference Manual* for more information on the VLT_CR register.

Table 3-16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[a]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[b]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	
	Vdd Value for PUMP Trip					
V_{PUMP0}	VM[2:0] = 000b	2.96	3.02	3.08	V	
V_{PUMP1}	VM[2:0] = 001b	3.03	3.10	3.16	V	
V_{PUMP2}	VM[2:0] = 010b	3.18	3.25	3.32	V	
V_{PUMP3}	VM[2:0] = 011b	4.11	4.19	4.28	V	
V_{PUMP4}	VM[2:0] = 100b	4.55	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.63	4.73	4.82	V	
V_{PUMP6}	VM[2:0] = 110b	4.72	4.82	4.91	V	
V_{PUMP7}	VM[2:0] = 111b	4.90	5.00	5.10	V	

a. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

3.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-18. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6[a]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	Trimmed. Utilizing factory trim values.
F_{48M}	Digital PSoC Block Frequency	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications below.
F_{24M}	Digital PSoC Block Frequency	0	24	24.6[b, d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	600	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	
$T_{PLLSLEWS-LOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	–	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{osacc} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. 3.0V ≤ Vdd ≤ 5.5V, -40 ^{0}C ≤ T_A ≤ 85 ^{0}C.
Jitter32k	32 kHz Period Jitter	–	100		ns	
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.

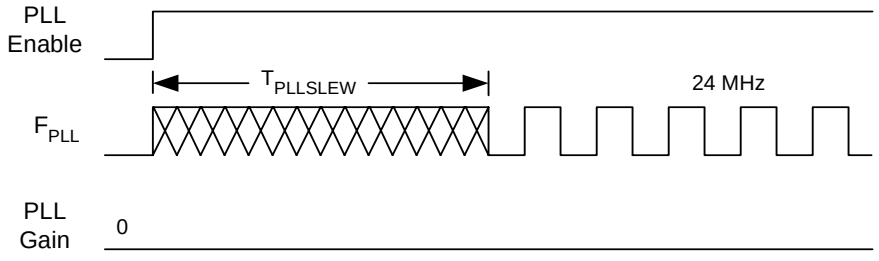


Figure 3-3. PLL Lock Timing Diagram

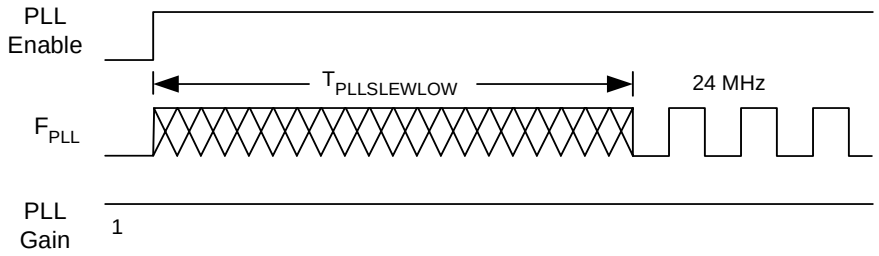


Figure 3-4. PLL Lock for Low Gain Setting Timing Diagram

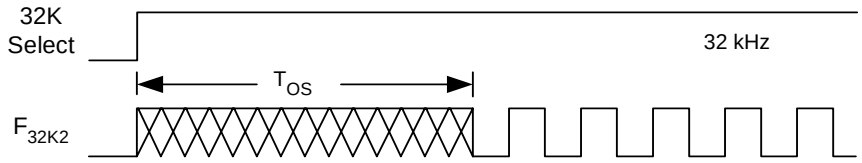


Figure 3-5. External Crystal Oscillator Startup Timing Diagram

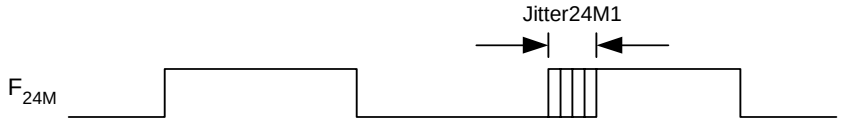


Figure 3-6. 24 MHz Period Jitter (IMO) Timing Diagram

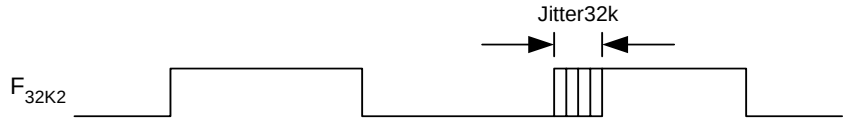


Figure 3-7. 32 kHz Period Jitter (ECO) Timing Diagram

3.4.2 AC General Purpose IO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-19. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

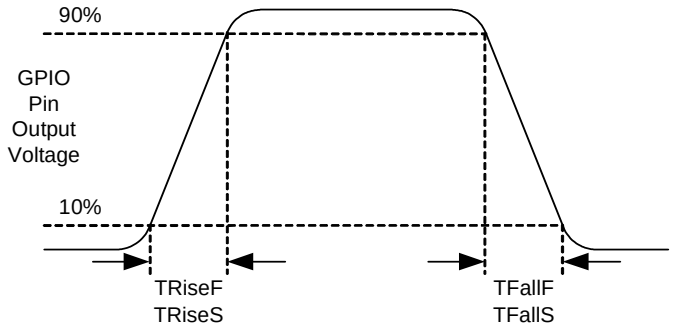


Figure 3-8. GPIO Timing Diagram

3.4.4 AC Digital Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-22. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2		4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6		3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[a]	–	–	ns	
	Disable Mode	50[a]	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	ns	
	Width of SS_ Negated Between Transmissions	50[a]	–	–	ns	
Transmitter	Maximum Input Clock Frequency [b]					
	Silicon A	–	–	16.4	MHz	Maximum data rate at 2.05 MHz due to 8 x over clocking.
	Silicon B	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency [b]					
	Silicon A	–	–	16.4	MHz	Maximum data rate at 2.05 MHz due to 8 x over clocking.
	Silicon B	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).
b. Refer to the Ordering Information chapter on page 42.

3.4.8 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-28. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set-up Time	250	–	100[a]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

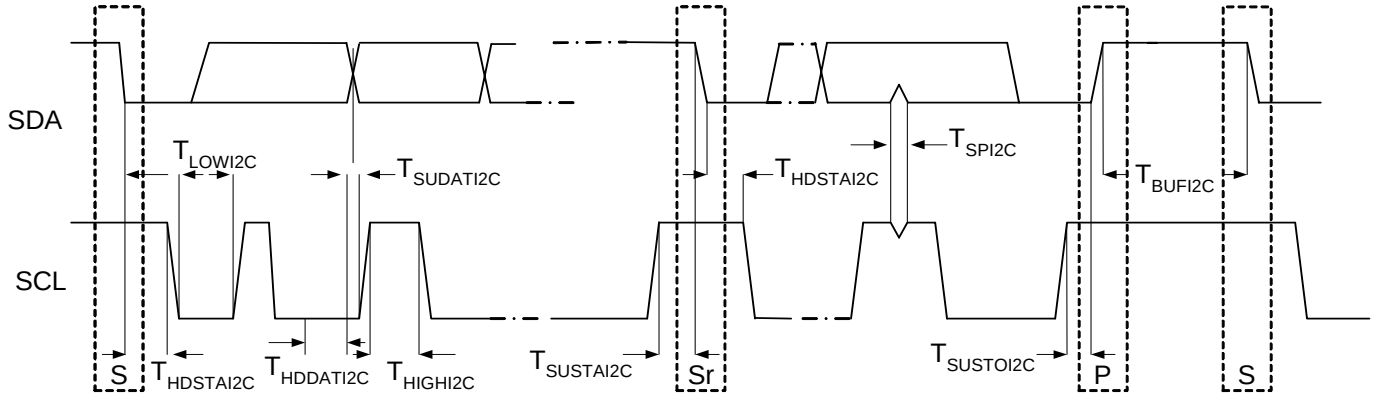


Figure 3-9. Definition for Timing for Fast/Standard Mode on the I²C Bus

4. Packaging Information

This chapter illustrates the packaging specifications for the CY8C27x43 PSoC device, along with the thermal impedances for each package and the typical package capacitance on crystal pins.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

4.1 Packaging Dimensions

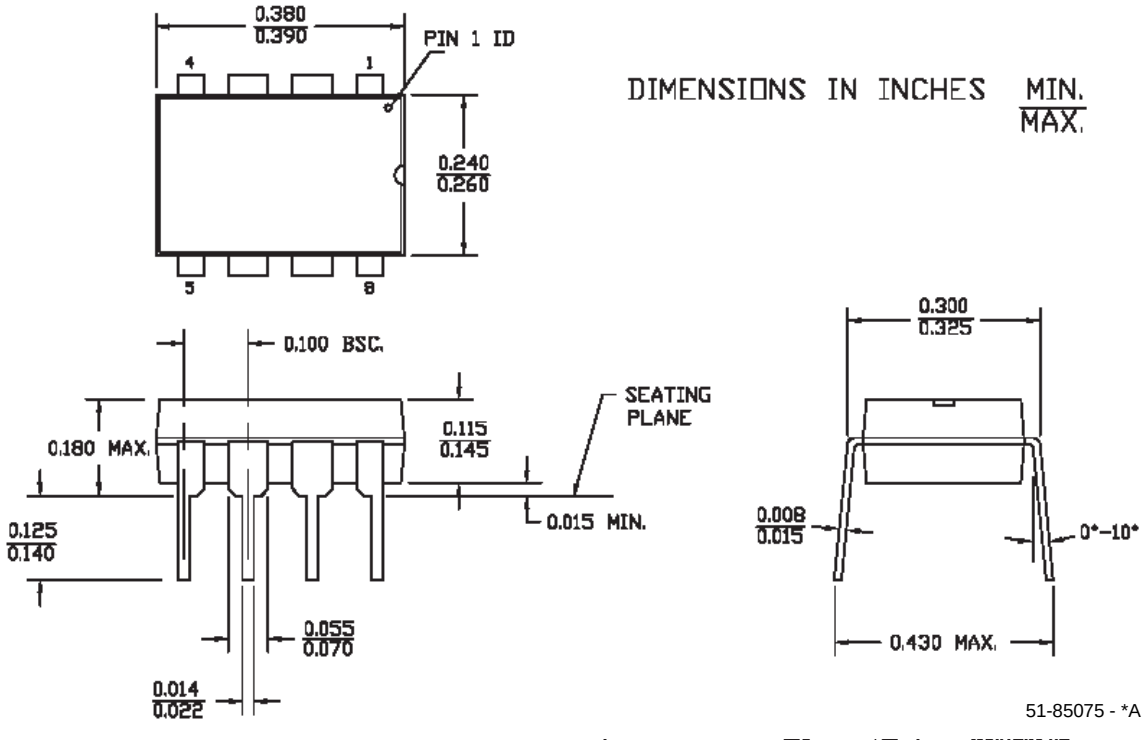


Figure 4-1. 8-Lead (300-Mil) PDIP

4.2 Thermal Impedances

Table 4-1. Thermal Impedances per Package

Package	Typical θ_{JA} *
8 PDIP	120 °C/W
20 SSOP	95 °C/W
20 SOIC	79 °C/W
28 PDIP	67 °C/W
28 SSOP	95 °C/W
28 SOIC	71 °C/W
44 TQFP	58 °C/W
48 SSOP	69 °C/W
48 MLF	18 °C/W

* $T_J = T_A + POWER \times \theta_{JA}$

4.3 Capacitance on Crystal Pins

Table 4-2: Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8 PDIP	2.8 pF
20 SSOP	2.6 pF
20 SOIC	2.5 pF
28 PDIP	3.5 pF
28 SSOP	2.8 pF
28 SOIC	2.7 pF
44 TQFP	2.6 pF
48 SSOP	3.3 pF
48 MLF	2.3 pF