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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 4x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c27443-24pvit

processor. The CPU utilizes an interrupt controller with 17 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

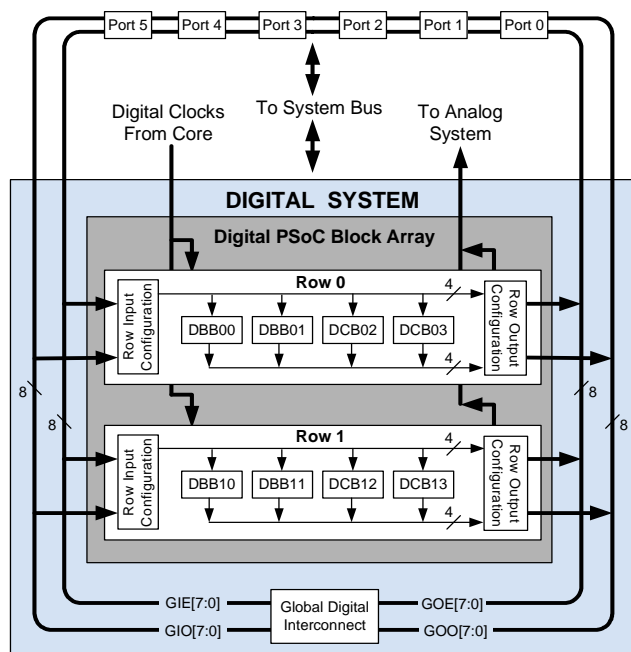
Memory encompasses 16 KB of Flash for program storage, 256 bytes of SRAM for data storage, and up to 2 KB of EEPROM emulated using the Flash. Program Flash utilizes four protection levels on blocks of 64 bytes, allowing customized software IP protection.

The PSoC device incorporates flexible internal clock generators, including a 24 MHz IMO (internal main oscillator) accurate to 2.5% over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (internal low speed oscillator) is provided for the Sleep timer and WDT. If crystal accuracy is desired, the ECO (32.768 kHz external crystal oscillator) is available for use as a Real Time Clock (RTC) and can optionally generate a crystal-accurate 24 MHz system clock using a PLL. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the PSoC device.

PSoC GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin also has the capability to generate a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System is composed of 8 digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.



Digital System Block Diagram

Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with Dead band (8 to 32 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity (up to 2)
- SPI master and slave (up to 2)
- I2C slave and master (1 available as a System Resource)
- Cyclical Redundancy Checker/Generator (8 to 32 bit)
- IrDA (up to 2)
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks can be connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled "PSoC Device Characteristics" on page 3.

The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2, 4, 6, and 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a Core Resource)
- 1.3V reference (as a System Resource)
- DTMF dialer
- Modulators
- Correlators
- Peak detectors
- Many other topologies possible

Getting Started

The quickest path to understanding the PSoC silicon is by reading this data sheet and using the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications. For in-depth information, along with detailed programming information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

For up-to-date Ordering, Packaging, and Electrical Specification information, reference the latest PSoC device data sheets on the web at <http://www.cypress.com/psoc>.

Development Kits

Development Kits are available from the following distributors: Digi-Key, Avnet, Arrow, and Future. The Cypress Online Store at <http://www.onfulfillment.com/cypressstore/> contains development kits, C compilers, and all accessories for PSoC development. Click on *PSoC (Programmable System-on-Chip)* to view a current list of available items.

Tele-Training

Free PSoC "Tele-training" is available for beginners and taught by a live marketing or application engineer over the phone. Five training classes are available to accelerate the learning curve including introduction, designing, debugging, advanced design, advanced analog, as well as application-specific classes covering topics like PSoC and the LIN bus. For days and times of the tele-training, see <http://www.cypress.com/support/training.cfm>.

Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant, go to the following Cypress support web site: <http://www.cypress.com/support/cypros.cfm>.

Technical Support

PSoC application engineers take pride in fast and accurate response. They can be reached with a 4-hour guaranteed response at <http://www.cypress.com/support/login.cfm>.

Application Notes

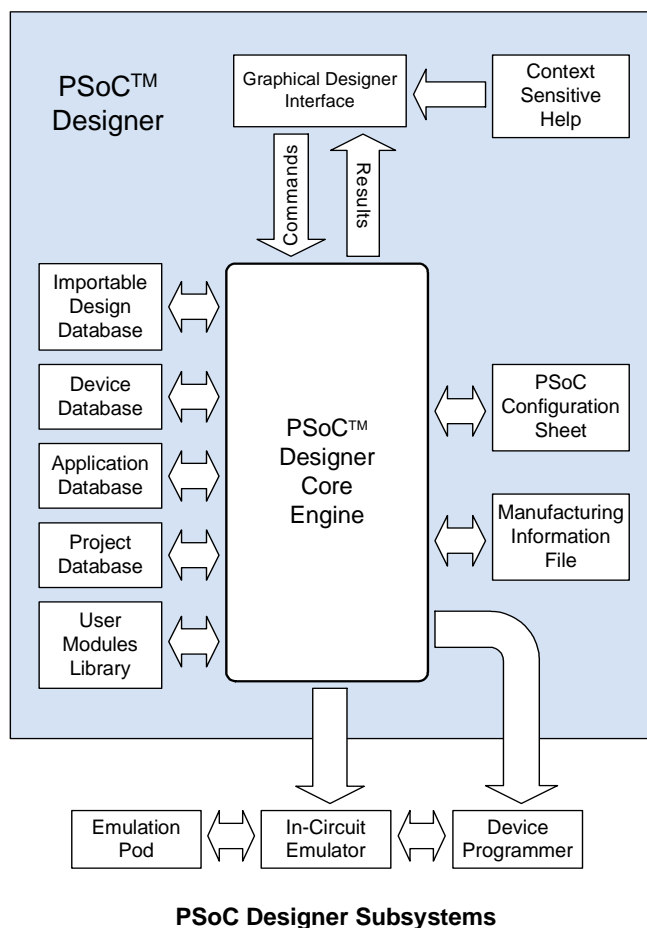
A long list of application notes will assist you in every aspect of your design effort. To locate the PSoC application notes, go to <http://www.cypress.com/design/results.cfm>.

Development Tools

The Cypress MicroSystems PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE and application runs on Windows NT 4.0, Windows 2000, Windows Millennium (Me), or Windows XP. (Reference the PSoC Designer Functional Flow diagram below.)

PSoC Designer helps the customer to select an operating configuration for the PSoC, write application code that uses the PSoC, and debug the application. This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and the CYASM macro assembler for the CPUs.

PSoC Designer also supports a high-level C language compiler developed specifically for the devices in the family.



1. Pin Information



This chapter describes, lists, and illustrates the CY8C27x43 PSoC device pins and pinout configurations.

1.1 Pinouts

The CY8C27x43 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital IO. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

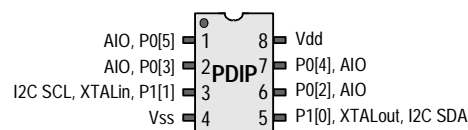
1.1.1 8-Pin Part Pinout

Table 1-1. 8-Pin Part Pinout (PDIP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	IO	P0[5]	Analog column mux input and column output.
2	IO	IO	P0[3]	Analog column mux input and column output.
3	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
4	Power		Vss	Ground connection.
5	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
6	IO	IO	P0[2]	Analog column mux input and column output.
7	IO	IO	P0[4]	Analog column mux input and column output.
8	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27143 8-Pin PSoC Device



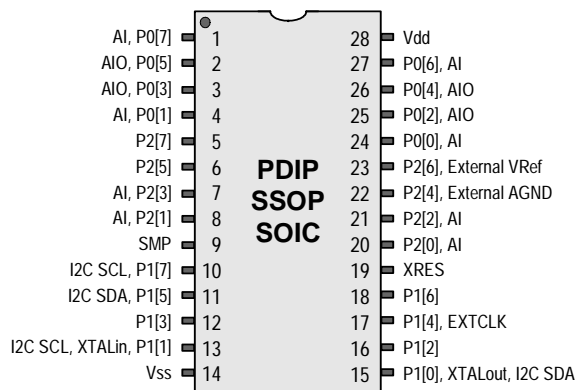
1.1.3 28-Pin Part Pinout

Table 1-3. 28-Pin Part Pinout (PDIP, SSOP, SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
10	IO		P1[7]	I2C Serial Clock (SCL)
11	IO		P1[5]	I2C Serial Data (SDA)
12	IO		P1[3]	
13	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
14	Power		Vss	Ground connection.
15	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
16	IO		P1[2]	
17	IO		P1[4]	Optional External Clock Input (EXTCLK)
18	IO		P1[6]	
19	Input		XRES	Active high external reset with internal pull down.
20	IO	I	P2[0]	Direct switched capacitor block input.
21	IO	I	P2[2]	Direct switched capacitor block input.
22	IO		P2[4]	External Analog Ground (AGND)
23	IO		P2[6]	External Voltage Reference (VRef)
24	IO	I	P0[0]	Analog column mux input.
25	IO	IO	P0[2]	Analog column mux input and column output.
26	IO	IO	P0[4]	Analog column mux input and column output.
27	IO	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27443 28-Pin PSoC Device



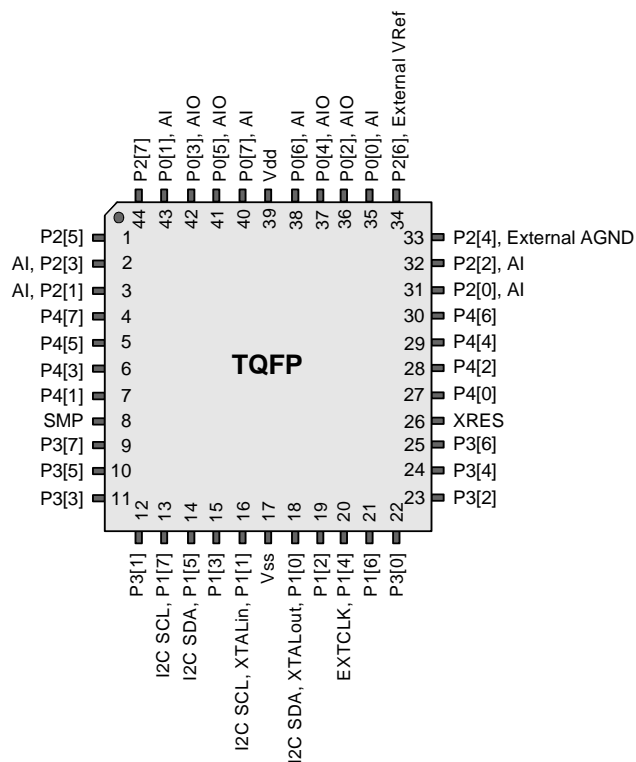
1.1.4 44-Pin Part Pinout

Table 1-4. 44-Pin Part Pinout (TQFP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO		P2[5]	
2	IO	I	P2[3]	Direct switched capacitor block input.
3	IO	I	P2[1]	Direct switched capacitor block input.
4	IO		P4[7]	
5	IO		P4[5]	
6	IO		P4[3]	
7	IO		P4[1]	
8	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
9	IO		P3[7]	
10	IO		P3[5]	
11	IO		P3[3]	
12	IO		P3[1]	
13	IO		P1[7]	I2C Serial Clock (SCL)
14	IO		P1[5]	I2C Serial Data (SDA)
15	IO		P1[3]	
16	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
17	Power		Vss	Ground connection.
18	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
19	IO		P1[2]	
20	IO		P1[4]	Optional External Clock Input (EXTCLK)
21	IO		P1[6]	
22	IO		P3[0]	
23	IO		P3[2]	
24	IO		P3[4]	
25	IO		P3[6]	
26	Input		XRES	Active high external reset with internal pull down.
27	IO		P4[0]	
28	IO		P4[2]	
29	IO		P4[4]	
30	IO		P4[6]	
31	IO	I	P2[0]	Direct switched capacitor block input.
32	IO	I	P2[2]	Direct switched capacitor block input.
33	IO		P2[4]	External Analog Ground (AGND)
34	IO		P2[6]	External Voltage Reference (VRef)
35	IO	I	P0[0]	Analog column mux input.
36	IO	IO	P0[2]	Analog column mux input and column output.
37	IO	IO	P0[4]	Analog column mux input and column output.
38	IO	I	P0[6]	Analog column mux input.
39	Power		Vdd	Supply voltage.
40	IO	I	P0[7]	Analog column mux input.
41	IO	IO	P0[5]	Analog column mux input and column output.
42	IO	IO	P0[3]	Analog column mux input and column output.
43	IO	I	P0[1]	Analog column mux input.
44	IO		P2[7]	

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27543 44-Pin PSoC Device



1.1.5 48-Pin Part Pinouts

Table 1-5. 48-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P0[7]	Analog column mux input.
2	IO	IO	P0[5]	Analog column mux input and column output.
3	IO	IO	P0[3]	Analog column mux input and column output.
4	IO	I	P0[1]	Analog column mux input.
5	IO		P2[7]	
6	IO		P2[5]	
7	IO	I	P2[3]	Direct switched capacitor block input.
8	IO	I	P2[1]	Direct switched capacitor block input.
9	IO		P4[7]	
10	IO		P4[5]	
11	IO		P4[3]	
12	IO		P4[1]	
13	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
14	IO		P3[7]	
15	IO		P3[5]	
16	IO		P3[3]	
17	IO		P3[1]	
18	IO		P5[3]	
19	IO		P5[1]	
20	IO		P1[7]	I2C Serial Clock (SCL)
21	IO		P1[5]	I2C Serial Data (SDA)
22	IO		P1[3]	
23	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
24	Power		Vss	Ground connection.
25	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
26	IO		P1[2]	
27	IO		P1[4]	Optional External Clock Input (EXTCLK)
28	IO		P1[6]	
29	IO		P5[0]	
30	IO		P5[2]	
31	IO		P3[0]	
32	IO		P3[2]	
33	IO		P3[4]	
34	IO		P3[6]	
35	Input		XRES	Active high external reset with internal pull down.
36	IO		P4[0]	
37	IO		P4[2]	
38	IO		P4[4]	
39	IO		P4[6]	
40	IO	I	P2[0]	Direct switched capacitor block input.
41	IO	I	P2[2]	Direct switched capacitor block input.
42	IO		P2[4]	External Analog Ground (AGND)
43	IO		P2[6]	External Voltage Reference (VRef)
44	IO	I	P0[0]	Analog column mux input.
45	IO	IO	P0[2]	Analog column mux input and column output.
46	IO	IO	P0[4]	Analog column mux input and column output.
47	IO	I	P0[6]	Analog column mux input.
48	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

CY8C27643 48-Pin PSoC Device

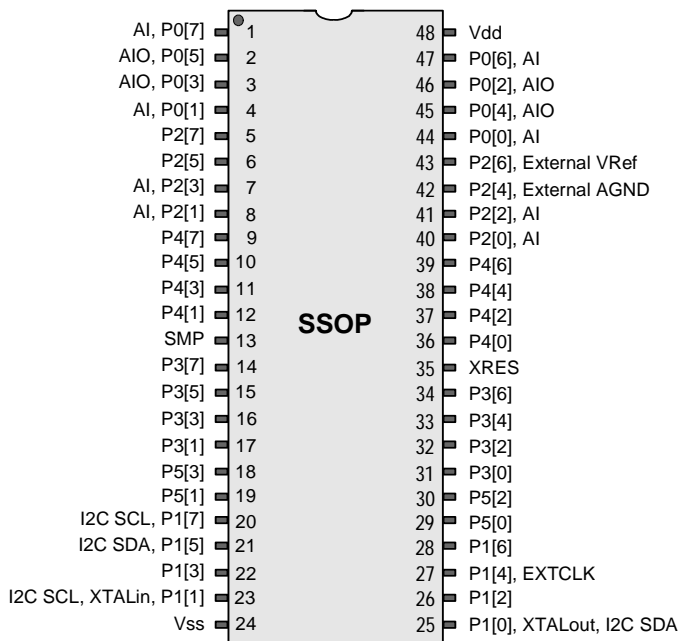


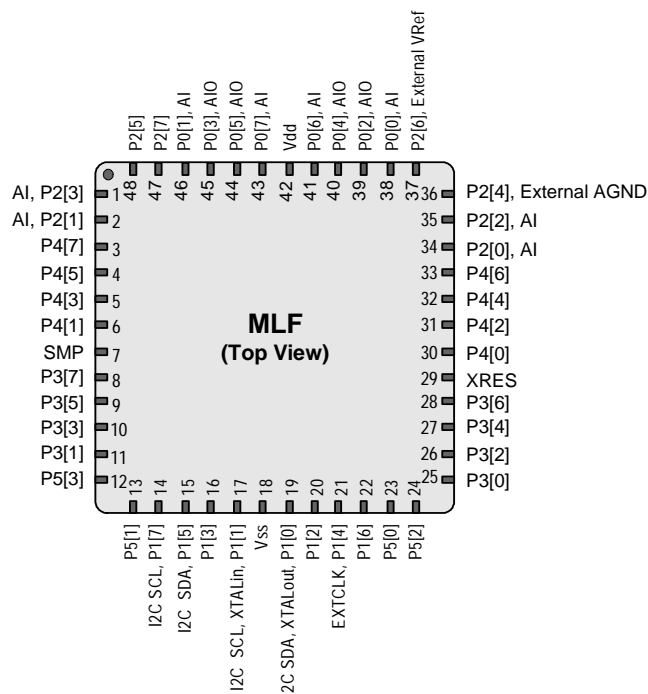
Table 1-6. 48-Pin Part Pinout (MLF*)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	IO	I	P2[3]	Direct switched capacitor block input.
2	IO	I	P2[1]	Direct switched capacitor block input.
3	IO		P4[7]	
4	IO		P4[5]	
5	IO		P4[3]	
6	IO		P4[1]	
7	Power		SMP	Switch Mode Pump (SMP) connection to external components required.
8	IO		P3[7]	
9	IO		P3[5]	
10	IO		P3[3]	
11	IO		P3[1]	
12	IO		P5[3]	
13	IO		P5[1]	
14	IO		P1[7]	I2C Serial Clock (SCL)
15	IO		P1[5]	I2C Serial Data (SDA)
16	IO		P1[3]	
17	IO		P1[1]	Crystal Input (XTALin), I2C Serial Clock (SCL)
18	Power		Vss	Ground connection.
19	IO		P1[0]	Crystal Output (XTALout), I2C Serial Data (SDA)
20	IO		P1[2]	
21	IO		P1[4]	Optional External Clock Input (EXTCLK)
22	IO		P1[6]	
23	IO		P5[0]	
24	IO		P5[2]	
25	IO		P3[0]	
26	IO		P3[2]	
27	IO		P3[4]	
28	IO		P3[6]	
29	Input		XRES	Active high external reset with internal pull down.
30	IO		P4[0]	
31	IO		P4[2]	
32	IO		P4[4]	
33	IO		P4[6]	
34	IO	I	P2[0]	Direct switched capacitor block input.
35	IO	I	P2[2]	Direct switched capacitor block input.
36	IO		P2[4]	External Analog Ground (AGND)
37	IO		P2[6]	External Voltage Reference (VRef)
38	IO	I	P0[0]	Analog column mux input.
39	IO	IO	P0[2]	Analog column mux input and column output.
40	IO	IO	P0[4]	Analog column mux input and column output.
41	IO	I	P0[6]	Analog column mux input.
42	Power		Vdd	Supply voltage.
43	IO	I	P0[7]	Analog column mux input.
44	IO	IO	P0[5]	Analog column mux input and column output.
45	IO	IO	P0[3]	Analog column mux input and column output.
46	IO	I	P0[1]	Analog column mux input.
47	IO		P2[7]	
48	IO		P2[5]	

LEGEND: A = Analog, I = Input, and O = Output.

* The MLF package has a center pad that must be connected to ground (Vss).

CY8C27643 48-Pin PSoC Device



2. Register Reference



This chapter lists the registers of the CY8C27x43 PSoC device. For detailed register information, reference the *PSoC™ Mixed Signal Array Technical Reference Manual*.

2.1 Register Conventions

The register conventions specific to this section are listed in the following table.

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XO1 bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XO1 bit is set the user is in bank 1.

Note In the following register mapping tables, blank fields are reserved and should not be accessed.

Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASC10CR0	80	RW		C0	
PRT0DM1	01	RW		41		ASC10CR1	81	RW		C1	
PRT0IC0	02	RW		42		ASC10CR2	82	RW		C2	
PRT0IC1	03	RW		43		ASC10CR3	83	RW		C3	
PRT1DM0	04	RW		44		ASD11CR0	84	RW		C4	
PRT1DM1	05	RW		45		ASD11CR1	85	RW		C5	
PRT1IC0	06	RW		46		ASD11CR2	86	RW		C6	
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW		48		ASC12CR0	88	RW		C8	
PRT2DM1	09	RW		49		ASC12CR1	89	RW		C9	
PRT2IC0	0A	RW		4A		ASC12CR2	8A	RW		CA	
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW		CB	
PRT3DM0	0C	RW		4C		ASD13CR0	8C	RW		CC	
PRT3DM1	0D	RW		4D		ASD13CR1	8D	RW		CD	
PRT3IC0	0E	RW		4E		ASD13CR2	8E	RW		CE	
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW		50		ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW		51		ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW		52		ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW		54		ASC21CR0	94	RW		D4	
PRT5DM1	15	RW		55		ASC21CR1	95	RW		D5	
PRT5IC0	16	RW		56		ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18			58		ASD22CR0	98	RW		D8	
	19			59		ASD22CR1	99	RW		D9	
	1A			5A		ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C			5C		ASC23CR0	9C	RW		DC	
	1D			5D		ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E			5E		ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW		6C			AC			EC	
DCB03IN	2D	RW		6D			AD			ED	
DCB03OU	2E	RW		6E			AE			EE	
	2F			6F			AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW		FA	
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Cap PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block. Typical parameters apply to 5V at 25°C and are for design guidance only.

Table 3-6. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High	–	1.6	10	mV	
	Power = Medium, Opamp Bias = High	–	1.3	8	mV	
	Power = High, Opamp Bias = High	–	1.2	7.5	mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	$\mu\text{V}/^{\circ}\text{C}$	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 μA .
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C .
V_{CMOA}	Common Mode Voltage Range	0.0	–	Vdd	V	The common-mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
	Common Mode Voltage Range (high power or high opamp bias)	0.5	–	Vdd - 0.5	V	
CMRR_{OA}	Common Mode Rejection Ratio		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
G_{OLOA}	Open Loop Gain		–	–	dB	Specification is applicable at high power. For all other bias modes (except high power, high opamp bias), minimum is 60 dB.
	Power = Low	60				
	Power = Medium	60				
V_{OHIGHOA}	High Output Voltage Swing (internal signals)					
	Power = Low	Vdd - 0.2	–	–	V	
	Power = Medium	Vdd - 0.2	–	–	V	
V_{OLOWA}	Low Output Voltage Swing (internal signals)					
	Power = Low	–	–	0.2	V	
	Power = Medium	–	–	0.2	V	
I_{SOA}	Supply Current (including associated AGND buffer)					
	Power = Low, Opamp Bias = Low	–	150	200	μA	
	Power = Low, Opamp Bias = High	–	300	400	μA	
PSRR_{OA}	Power = Medium, Opamp Bias = Low	–	600	800	μA	
	Power = Medium, Opamp Bias = High	–	1200	1600	μA	
	Power = High, Opamp Bias = Low	–	2400	3200	μA	
PSRR_{OA}	Power = High, Opamp Bias = High	–	4600	6400	μA	
	Supply Voltage Rejection Ratio	60	–	–	dB	

3.3.5 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-10. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{\text{PUMP } 5\text{V}}$	5V Output Voltage	4.75	5.0	5.25	V	Configuration of footnote ^a . Average, neglecting ripple. SMP trip voltage is set to 5.0V.
$V_{\text{PUMP } 3\text{V}}$	3V Output Voltage	3.00	3.25	3.60	V	Configuration of footnote ^a . Average, neglecting ripple. SMP trip voltage is set to 3.25V.
I_{PUMP}	Available Output Current $V_{\text{BAT}} = 1.5\text{V}$, $V_{\text{PUMP}} = 3.25\text{V}$ $V_{\text{BAT}} = 1.8\text{V}$, $V_{\text{PUMP}} = 5.0\text{V}$	8 5	— —	— —	mA mA	Configuration of footnote ^a . SMP trip voltage is set to 3.25V. SMP trip voltage is set to 5.0V.
$V_{\text{BAT}5\text{V}}$	Input Voltage Range from Battery	1.8	—	5.0	V	Configuration of footnote ^a . SMP trip voltage is set to 5.0V.
$V_{\text{BAT}3\text{V}}$	Input Voltage Range from Battery	1.0	—	3.3	V	Configuration of footnote ^a . SMP trip voltage is set to 3.25V.
V_{BATSTART}	Minimum Input Voltage from Battery to Start Pump	1.1	—	—	V	Configuration of footnote ^a .
$\Delta V_{\text{PUMP_Line}}$	Line Regulation (over V_{BAT} range)	—	5	—	% V_O	Configuration of footnote ^a . V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26 .
$\Delta V_{\text{PUMP_Load}}$	Load Regulation	—	5	—	% V_O	Configuration of footnote ^a . V_O is the “Vdd Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-16 on page 26 .
$\Delta V_{\text{PUMP_Ripple}}$	Output Voltage Ripple (depends on capacitor/load)	—	100	—	mVpp	Configuration of footnote ^a . Load is 5mA.
E_3	Efficiency	35	50	—	%	Configuration of footnote ^a . Load is 5 mA. SMP trip voltage is set to 3.25V.
F_{PUMP}	Switching Frequency	—	1.3	—	MHz	
DC_{PUMP}	Switching Duty Cycle	—	50	—	%	

a. $L_1 = 2\text{ }\mu\text{H}$ inductor, $C_1 = 10\text{ }\mu\text{F}$ capacitor, $D_1 = \text{Schottky diode}$. See Figure 3-2.

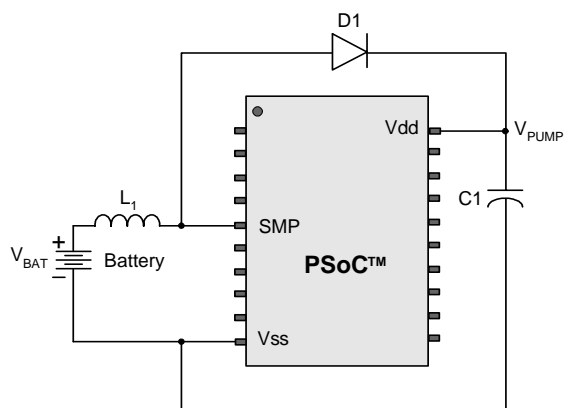


Figure 3-2. Basic Switch Mode Pump Circuit

3.3.9 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying V_{ilp} to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying V_{ihp} to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	$V_{SS} + 0.75$	V	
V_{OHV}	Output High Voltage During Programming or Verify	$V_{DD} - 1.0$	–	V_{DD}	V	
Flash _{ENPB}	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
Flash _{ENT}	Flash Endurance (total) ^a	1,800,000	–	–	–	Erase/write cycles.
Flash _{DR}	Flash Data Retention	10	–	–	Years	

- a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at <http://www.cypress.com> under Application Notes for more information.

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-18. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO}	Internal Main Oscillator Frequency	23.4	24	24.6 ^a	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6 ^{a,b}	MHz	Trimmed. Utilizing factory trim values.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3 ^{b,c}	MHz	Trimmed. Utilizing factory trim values.
$F_{48\text{M}}$	Digital PSoC Block Frequency	0	48	49.2 ^{a,b,d}	MHz	Refer to the AC Digital Block Specifications below.
$F_{24\text{M}}$	Digital PSoC Block Frequency	0	24	24.6 ^{b,d}	MHz	
$F_{32\text{K1}}$	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
$F_{32\text{K2}}$	External Crystal Oscillator	—	32.768	—	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	—	23.986	—	MHz	Multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	—	—	600	ps	
T_{PLLSLEW}	PLL Lock Time	0.5	—	10	ms	
$T_{\text{PLLSLEWS-LOW}}$	PLL Lock Time for Low Gain Setting	0.5	—	50	ms	
T_{OS}	External Crystal Oscillator Startup to 1%	—	1700	2620	ms	
T_{OSACC}	External Crystal Oscillator Startup to 100 ppm	—	2800	3800	ms	The crystal oscillator frequency is within 100 ppm of its final value by the end of the T_{OSACC} period. Correct operation assumes a properly loaded 1 uW maximum drive level 32.768 kHz crystal. $3.0\text{V} \leq V_{\text{DD}} \leq 5.5\text{V}$, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$.
Jitter32k	32 kHz Period Jitter	—	100	—	ns	
T_{XRST}	External Reset Pulse Width	10	—	—	μs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	—	50	—	kHz	
F_{out48M}	48 MHz Output Frequency	46.8	48.0	49.2 ^{a,c}	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO)	—	600	—	ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	—	—	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	—	—	μs	

a. $4.75\text{V} < V_{\text{DD}} < 5.25\text{V}$.

b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.

c. $3.0\text{V} < V_{\text{DD}} < 3.6\text{V}$. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.

d. See the individual user module data sheets for information on maximum frequencies for user modules.

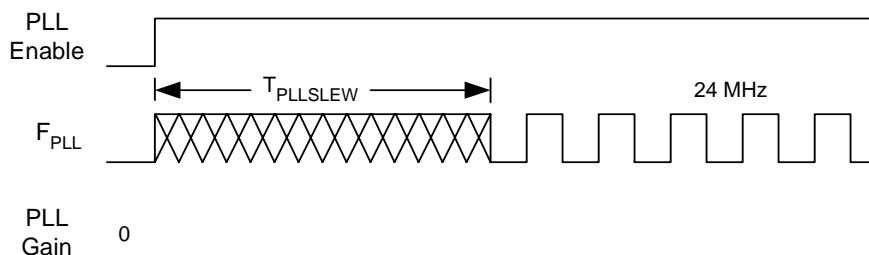


Figure 3-3. PLL Lock Timing Diagram

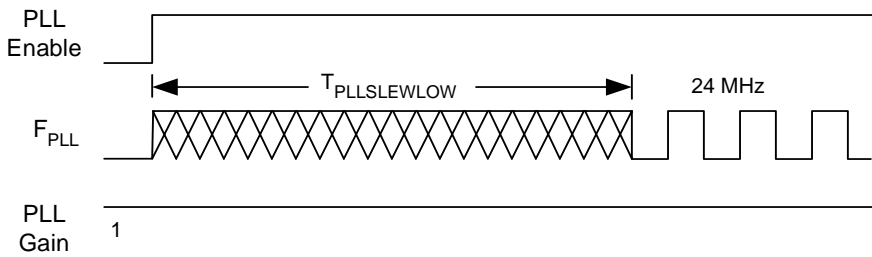


Figure 3-4. PLL Lock for Low Gain Setting Timing Diagram

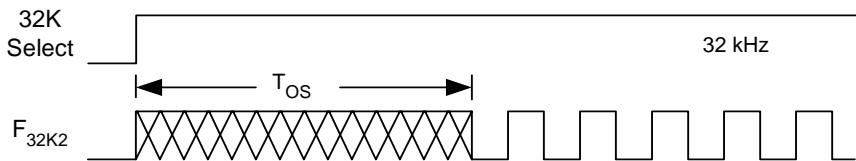


Figure 3-5. External Crystal Oscillator Startup Timing Diagram



Figure 3-6. 24 MHz Period Jitter (IMO) Timing Diagram

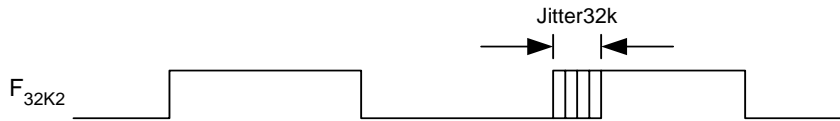


Figure 3-7. 32 kHz Period Jitter (ECO) Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 3-20. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	3.9	μs	
	Power = Medium, Opamp Bias = High	—	—	0.72	μs	
	Power = High, Opamp Bias = High	—	—	0.62	μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	5.9	μs	
	Power = Medium, Opamp Bias = High	—	—	0.92	μs	
	Power = High, Opamp Bias = High	—	—	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.15	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	1.7	—	—	V/ μs	
	Power = High, Opamp Bias = High	6.5	—	—	V/ μs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.01	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	0.5	—	—	V/ μs	
	Power = High, Opamp Bias = High	4.0	—	—	V/ μs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.75	—	—	MHz	
	Power = Medium, Opamp Bias = High	3.1	—	—	MHz	
	Power = High, Opamp Bias = High	5.4	—	—	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	—	100	—	nV/rt-Hz	

Table 3-21. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	3.92	μs	
	Power = Low, Opamp Bias = High	—	—	0.72	μs	
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	—	—	5.41	μs	
	Power = Medium, Opamp Bias = High	—	—	0.72	μs	
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.31	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	2.7	—	—	V/ μs	
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain)					
	Power = Low, Opamp Bias = Low	0.24	—	—	V/ μs	
	Power = Medium, Opamp Bias = High	1.8	—	—	V/ μs	
BW_{OA}	Gain Bandwidth Product					
	Power = Low, Opamp Bias = Low	0.67	—	—	MHz	
	Power = Medium, Opamp Bias = High	2.8	—	—	MHz	
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	—	100	—	nV/rt-Hz	

3.4.5 AC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-23. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.5	μs	
	Power = High	–	–	2.5	μs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.2	μs	
	Power = High	–	–	2.2	μs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/ μs	
	Power = High	0.65	–	–	V/ μs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.65	–	–	V/ μs	
	Power = High	0.65	–	–	V/ μs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp} , 3dB BW, 100pF Load					
	Power = Low	0.8	–	–	MHz	
	Power = High	0.8	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp} , 3dB BW, 100pF Load					
	Power = Low	300	–	–	kHz	
	Power = High	300	–	–	kHz	

Table 3-24. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	3.8	μs	
	Power = High	–	–	3.8	μs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load					
	Power = Low	–	–	2.6	μs	
	Power = High	–	–	2.6	μs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load					
	Power = Low	0.5	–	–	V/ μs	
	Power = High	0.5	–	–	V/ μs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load					
	Power = Low	0.5	–	–	V/ μs	
	Power = High	0.5	–	–	V/ μs	
BW_{OB}	Small Signal Bandwidth, 20mV_{pp} , 3dB BW, 100pF Load					
	Power = Low	0.7	–	–	MHz	
	Power = High	0.7	–	–	MHz	
BW_{OB}	Large Signal Bandwidth, 1V_{pp} , 3dB BW, 100pF Load					
	Power = Low	200	–	–	kHz	
	Power = High	200	–	–	kHz	

3.4.8 AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 3.0V to 3.6V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 3-28. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
$F_{\text{SCL}2\text{C}}$	SCL Clock Frequency	0	100	0	400	kHz	
$T_{\text{HDSTA}2\text{C}}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	—	0.6	—	μs	
$T_{\text{LOW}2\text{C}}$	LOW Period of the SCL Clock	4.7	—	1.3	—	μs	
$T_{\text{HIGH}2\text{C}}$	HIGH Period of the SCL Clock	4.0	—	0.6	—	μs	
$T_{\text{SUSTA}2\text{C}}$	Set-up Time for a Repeated START Condition	4.7	—	0.6	—	μs	
$T_{\text{HDDAT}2\text{C}}$	Data Hold Time	0	—	0	—	μs	
$T_{\text{SUDAT}2\text{C}}$	Data Set-up Time	250	—	100 ^a	—	ns	
$T_{\text{SUSTOI}2\text{C}}$	Set-up Time for STOP Condition	4.0	—	0.6	—	μs	
$T_{\text{BUF}2\text{C}}$	Bus Free Time Between a STOP and START Condition	4.7	—	1.3	—	μs	
$T_{\text{SPI}2\text{C}}$	Pulse Width of spikes are suppressed by the input filter.	—	—	0	50	ns	

- a. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $t_{\text{SU:DAT}} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{\text{rmax}} + t_{\text{SU:DAT}} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

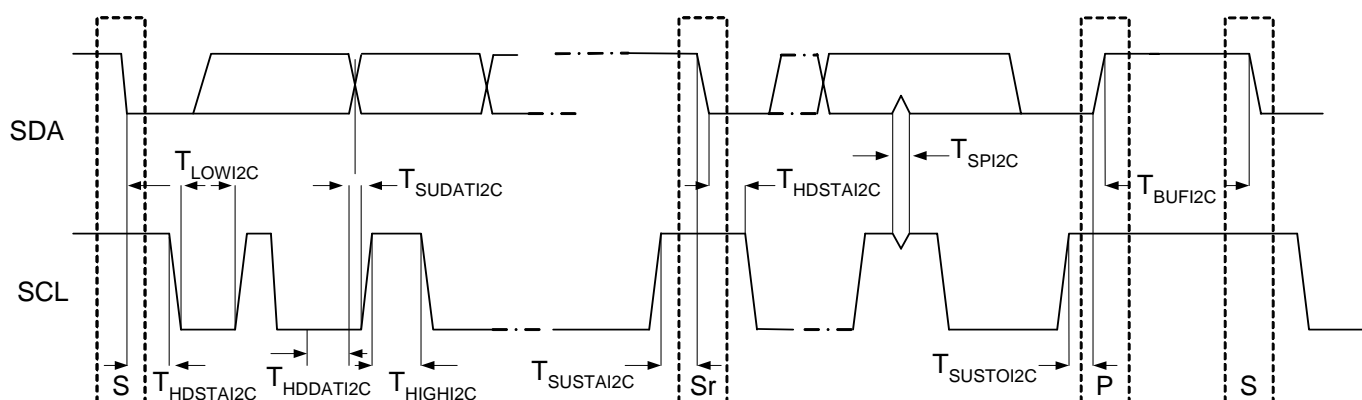


Figure 3-9. Definition for Timing for Fast/Standard Mode on the I²C Bus

4.2 Thermal Impedances

Table 4-1. Thermal Impedances per Package

Package	Typical θ_{JA} *
8 PDIP	120 °C/W
20 SSOP	95 °C/W
20 SOIC	79 °C/W
28 PDIP	67 °C/W
28 SSOP	95 °C/W
28 SOIC	71 °C/W
44 TQFP	58 °C/W
48 SSOP	69 °C/W
48 MLF	18 °C/W

* $T_J = T_A + \text{POWER} \times \theta_{JA}$

4.3 Capacitance on Crystal Pins

Table 4-2: Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
8 PDIP	2.8 pF
20 SSOP	2.6 pF
20 SOIC	2.5 pF
28 PDIP	3.5 pF
28 SSOP	2.8 pF
28 SOIC	2.7 pF
44 TQFP	2.6 pF
48 SSOP	3.3 pF
48 MLF	2.3 pF

5. Ordering Information



The following table lists the CY8C27x43 PSoC device family's key package features and ordering codes.

Table 5-1. CY8C27x43 PSoC Device Family Key Features and Ordering Information

Package	Ordering Code	Flash (Kbytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks (Rows of 4)	Analog Blocks (Columns of 3)	Digital IO Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C27x43 Silicon B – These parts are lead free and offer the following improvements. The DEC_CR1 register selections are enhanced to allow any digital block to be the decimator clock source, the ECO EX and ECO EXW bits in the CPU_SCR1 register are readable, and the accuracy of the analog reference is enhanced (see the Electrical Specifications chapter). All silicon A errata are fixed in silicon B.											
8 Pin (300 Mil) DIP	CY8C27143-24PXI	16	256	No	-40C to +85C	8	12	6	4	4	No
20 Pin (210 Mil) SSOP	CY8C27243-24PVXI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27243-24PVXIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (300 Mil) SOIC	CY8C27243-24SXI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin 300 Mil) SOIC (Tape and Reel)	CY8C27243-24SXIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
28 Pin (300 Mil) DIP	CY8C27443-24PXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C27443-24PVXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27443-24PVXIT	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (300 Mil) SOIC	CY8C27443-24SXI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (300 Mil) SOIC (Tape and Reel)	CY8C27443-24SXIT	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
44 Pin TQFP	CY8C27543-24AXI	16	256	Yes	-40C to +85C	8	12	40	12	4	Yes
44 Pin TQFP (Tape and Reel)	CY8C27543-24AXIT	16	256	Yes	-40C to +85C	8	12	40	12	4	Yes
48 Pin (300 Mil) SSOP	CY8C27643-24PVXI	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (300 Mil) SSOP (Tape and Reel)	CY8C27643-24PVXIT	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) MLF	CY8C27643-24LFXI	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
48 Pin (7x7) MLF (Tape and Reel)	CY8C27643-24LFXIT	16	256	Yes	-40C to +85C	8	12	44	12	4	Yes
CY8C27x43 Silicon A – Silicon A is not recommended for new designs.											
8 Pin (300 Mil) DIP	CY8C27143-24PI	16	256	No	-40C to +85C	8	12	6	4	4	No
20 Pin (210 Mil) SSOP	CY8C27243-24PVI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (210 Mil) SSOP (Tape and Reel)	CY8C27243-24PVIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin (300 Mil) SOIC	CY8C27243-24SI	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
20 Pin 300 Mil) SOIC (Tape and Reel)	CY8C27243-24SIT	16	256	Yes	-40C to +85C	8	12	16	8	4	Yes
28 Pin (300 Mil) DIP	CY8C27443-24PI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes
28 Pin (210 Mil) SSOP	CY8C27443-24PVI	16	256	Yes	-40C to +85C	8	12	24	12	4	Yes

6. Sales and Service Information



To obtain information about Cypress Microsystems or PSoC sales and technical support, reference the following information or go to the section titled "Getting Started" on page 4 in this document.

Cypress Microsystems

2700 162nd Street SW
Building D
Lynnwood, WA 98037
Phone: 800.669.0557
Facsimile: 425.787.4641

Web Sites: Company Information – <http://www.cypress.com>
Sales – http://www.cypress.com/aboutus/sales_locations.cfm
Technical Support – <http://www.cypress.com/support/login.cfm>

6.1 Revision History

Table 6-1. CY8C27x43 Data Sheet Revision History

Document Title: CY8C27143, CY8C27243, CY8C27443, CY8C27543, and CY8C27643 PSoC Mixed Signal Array Final Data Sheet				
Document Number: 38-12012				
Revision	ECN #	Issue Date	Origin of Change	Description of Change
**	127087	7/01/2003	New Silicon.	New document (Revision **).
*A	128780	7/29/2003	Engineering and NWJ.	New electrical spec additions, fix of Core Architecture links, corrections to some text, tables, drawings, and format.
*B	128992	8/14/2003	NWJ	Interrupt controller table fixed, refinements to Electrical Spec section and Register chapter.
*C	129283	8/28/2003	NWJ	Significant changes to the Electrical Specifications section.
*D	129442	9/09/2003	NWJ	Changes made to Electrical Spec section. Added 20/28-Lead SOIC packages and pinouts.
*E	130129	10/13/2003	NWJ	Revised document for Silicon Revision A.
*F	130651	10/28/2003	NWJ	Refinements to Electrical Specification section and I2C chapter.
*G	131298	11/18/2003	NWJ	Revisions to GDI, RDI, and Digital Block chapters. Revisions to AC Digital Block Spec and miscellaneous register changes.
*H	229416	See ECN	SFV	New data sheet format and organization. Reference the <i>PSoC Mixed Signal Array Technical Reference Manual</i> for additional information. Title change.
*I	247529	See ECN	SFV	Added Silicon B information to this data sheet.
Distribution: External Public Posting: None				

6.2 Copyrights and Code Protection

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