Infineon Technologies - MB91F522BSBPMC1-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	44
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 26x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522bsbpmc1-gte1

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
19 *1	24 *1	29 *1	35 *1	41	51	P057	-	G	General-purpose I/O port
						RDY *2, *3, *4, *5	-		External bus/Ready input (0)
						SCK10_1	-		Multi-function serial ch.10 clock I/O (1)
						AN42	-		ADC analog 42 input
						ICU8_0	-		Input capture ch.8 input (0)
						TRG0_2	-		PPG trigger 0 input (2)
						PPG1_1	-		PPG ch.1 output (1)
						ICU1_1	-		Input capture ch.1 input (1)
						TIN6_1	-		Reload timer ch.6 event input (1)
-	-	-	-	44	54	P142	-	F	General-purpose I/O port
						SCK10_0 / SCL10	-		Multi-function serial ch.10 clock I/O (0)/ I^2C bus serial clock I/O
						PPG38_0	-		PPG ch.38 output (0)
						TIN7_1	-		Reload timer ch.7 event input (1)
-	-	-	-	45	55	P143	-	F	General-purpose I/O port
						SOT10_0 /SDA10	-		Multi-function serial ch.10 serial data output (0)/ I^2C bus serial data I/O
						PPG39_0	-		PPG ch.39 output (0)
						TOT4_1	-		Reload timer ch.4 output (1)
-	-	-	-	-	56	P182	-	A	General-purpose I/O port
						PPG42_0	-		PPG ch.42 output (0)
-	-	32	38	46	57	P060	-	A	General-purpose I/O port
						SCS10_0	-		Serial chip select 10 I/O (0)
						PPG2_1	-		PPG ch.2 output (1)
						ICU2_1	-		Input capture ch.2 input (1)
						TOT5_1	-		Reload timer ch.5 output (1)
						INT13_0	-		INT13 External interrupt input (0)
22	27	33	39	47	58	P061	-	B	General-purpose I/O port
						SOT10_1	-		Multi-function serial ch.10 serial data output (1)
						AN41	-		ADC analog 41 input
						ICU6_0	-		Input capture ch.6 input (0)
						PPG3_1	-		PPG ch.3 output (1)
						ICU3_1	-		Input capture ch.3 input (1)
						TOT6_1	-		Reload timer ch.6 output (1)
						INT13_1	-		INT13 External interrupt input (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0001F8_H$	TMRLRA6 [R/W] H XXXXXXXX XXXXXXXX		TMR6 [R] H XXXXXXXX XXXXXXXX		Reload Timer 6
$0001FC_H$	TMRLRB6 [R/W] H XXXXXXXX XXXXXXXX		TMCSR6 [R/W] B, H,W 00000000 0-000000		
000200_H to 000238_H	—	—	—	—	Reserved
$00023C_H$	DACR0 [R/W] B,H,W -------0	DADR0 [R/W] B,H,W XXXXXXXX	DACR1 [R/W] B,H,W -------0	DADR1 [R/W] B,H,W XXXXXXXX	DA Converter
000240_H	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 3 32-bit FRT
000244_H	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000248_H	TCCSH3 [R/W] B,H,W 0-----00	TCCSL3 [R/W] B,H,W -1-00000	—	—	
$00024C_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run Timer 4 32-bit FRT
000250_H	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000254_H	TCCSH4 [R/W] B,H,W 0-----00	TCCSL4 [R/W] B,H,W -1-00000	—	—	
000258_H to $0002C0_H$	—	—	—	—	Reserved
$0002C4_H$ to $0002FC_H$	—	—	—	—	Reserved
000300_H to $00030C_H$	—	—	—	—	Reserved
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only CPU core can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000C4C_H$	DDAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA Controller [S]
$000C50_H$	DCCR5 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C54_H$	DCSR5 [R/W] H 0------- -----000		DTCR5 [R/W] H 00000000 00000000		
$000C58_H$	DSAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6 [R/W] H 0------- -----000		DTCR6 [R/W] H 00000000 00000000		
$000C68_H$	DSAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7 [R/W] H 0------- -----000		DTCR7 [R/W] H 00000000 00000000		
$000C78_H$	DSAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$	DCCR8 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C84_H$	DCSR8 [R/W] H 0------- -----000		DTCR8 [R/W] H 00000000 00000000		
$000C88_H$	DSAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C8C_H$	DDAR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C90_H$	DCCR9 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C94_H$	DCSR9 [R/W] H 0------- -----000		DTCR9 [R/W] H 00000000 00000000		
$000C98_H$	DSAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C9C_H$	DDAR9 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000E3C$_H$	—	—	—	—	Reserved
000E40$_H$	PDDR00 [R] B,H,W XXXXXXXX	PDDR01 [R] B,H,W XXXXXXXX	PDDR02 [R] B,H,W XXXXXXXX	PDDR03 [R] B,H,W XXXXXXXX	Port Direct Read Register
000E44$_H$	PDDR04 [R] B,H,W XXXXXXXX	PDDR05 [R] B,H,W XXXXXXXX	PDDR06 [R] B,H,W XXXXXXXX	PDDR07 [R] B,H,W XXXXXXXX	
000E48$_H$	PDDR08 [R] B,H,W XXXXXXXX	PDDR09 [R] B,H,W XXXXXXXX	PDDR10 [R] B,H,W XXXXXXXX	PDDR11 [R] B,H,W XXXXXXXX	
000E4C$_H$	PDDR12 [R] B,H,W XXXXXXXX	PDDR13 [R] B,H,W -XXXXXXX	PDDR14 [R] B,H,W ---XXX--	PDDR15 [R] B,H,W --XXXXXX	
000E50$_H$	—	—	—	—	
000E54$_H$	—	—	—	—	
000E58$_H$	PDDR16 [R] B,H,W XXXXXXXX	PDDR17 [R] B,H,W XXXXXXXX	PDDR18 [R] B,H,W XXXXXXXX	PDDR19 [R] B,H,W XXXXXXXX	
000E5C$_H$	—	—	—	—	Reserved
000E60$_H$	EPFR00 [R/W] B,H,W 00000000	EPFR01 [R/W] B,H,W -0-0-000	EPFR02 [R/W] B,H,W ----0000	EPFR03 [R/W] B,H,W ---000-0	Extended Port Function Register
000E64$_H$	EPFR04 [R/W] B,H,W ----00-0	EPFR05 [R/W] B,H,W ----0000	EPFR06 [R/W] B,H,W ----000-	EPFR07 [R/W] B,H,W ---00000	
000E68$_H$	EPFR08 [R/W] B,H,W ---00000	EPFR09 [R/W] B,H,W -----00-	EPFR10 [R/W] B,H,W ----0000	EPFR11 [R/W] B,H,W ----0000	
000E6C$_H$	EPFR12 [R/W] B,H,W ----0000	EPFR13 [R/W] B,H,W ------00	EPFR14 [R/W] B,H,W ------00	EPFR15 [R/W] B,H,W -----000	
000E70$_H$	—	—	—	—	
000E74$_H$	—	—	—	—	
000E78$_H$	—	—	EPFR26 [R/W] B,H,W 00000000	EPFR27 [R/W] B,H,W ---0----	
000E7C$_H$	EPFR28 [R/W] B,H,W --000-0-	EPFR29 [R/W] B,H,W 00000000	—	—	
000E80$_H$	—	EPFR33 [R/W] B,H,W -----00-	EPFR34 [R/W] B,H,W -----00-	EPFR35 [R/W] B,H,W ---00000	
000E84$_H$	EPFR36 [R/W] B,H,W ----000-	—	—	—	
000E88$_H$	—	—	EPFR42 [R/W] B,H,W ------00	EPFR43 [R/W] B,H,W 0--0000-	
000E8C$_H$	EPFR44 [R/W] B,H,W -00---0-	EPFR45 [R/W] B,H,W -0000000	—	—	
000E90$_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001AD0_H$	PCN6 [R/W] B,H,W 00000000 000000-0		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$001AD4_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PTMR6 [R] H,W 11111111 11111111		
$001AD8_H$	PCN206 [R/W] B,H,W --000000 -----110		PSDR6 [R/W] H,W 00000000 00000000		
$001ADC_H$	PTPC6 [R/W] H,W 00000000 00000000		—	—	
$001AE0_H$	PCN7 [R/W] B,H,W 00000000 000000-0		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$001AE4_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PTMR7 [R] H,W 11111111 11111111		
$001AE8_H$	PCN207 [R/W] B,H,W --000000 -----110		PSDR7 [R/W] H,W 00000000 00000000		
$001AEC_H$	PTPC7 [R/W] H,W 00000000 00000000		—	—	
$001AF0_H$	PCN8 [R/W] B,H,W 00000000 000000-0		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$001AF4_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PTMR8 [R] H,W 11111111 11111111		
$001AF8_H$	PCN208 [R/W] B,H,W --000000 -----110		PSDR8 [R/W] H,W 00000000 00000000		
$001AFC_H$	PTPC8 [R/W] H,W 00000000 00000000		—	—	
$001B00_H$	PCN9 [R/W] B,H,W 00000000 000000-0		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$001B04_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PTMR9 [R] H,W 11111111 11111111		
$001B08_H$	PCN209 [R/W] B,H,W --000000 -----110		PSDR9 [R/W] H,W 00000000 00000000		
$001B0C_H$	PTPC9 [R/W] H,W 00000000 00000000		—	—	
$001B10_H$	PCN10 [R/W] B,H,W 00000000 000000-0		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$001B14_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PTMR10 [R] H,W 11111111 11111111		
$001B18_H$	PCN210 [R/W] B,H,W --000000 -----110		PSDR10 [R/W] H,W 00000000 00000000		PPG10
$001B1C_H$	PTPC10 [R/W] H,W 00000000 00000000		—	—	
$001B20_H$	PCN11 [R/W] B,H,W 00000000 000000-0		PCSR11 [W] H,W XXXXXXXX XXXXXXXX		PPG11

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				RAM/ diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		RAM/ diagnosis Backup RAM
003044_H	TSRCRA [R/W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $005FFC_H$	Backup-RAM				Backup RAM area

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

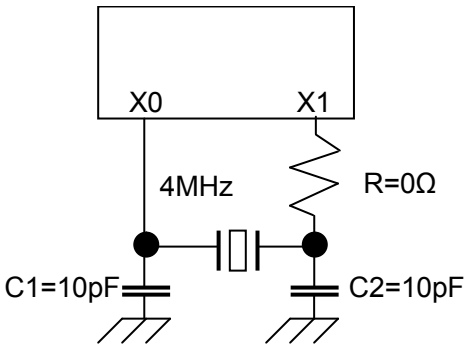
Interrupt vector
64 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexa decimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
-	22	16	ICR06	$3A4_H$	$000FFFA4_H$	-*6
-	23	17	ICR07	$3A0_H$	$000FFFA0_H$	-*6
-	24	18	ICR08	$39C_H$	$000FFF9C_H$	-*6
-	25	19	ICR09	398_H	$000FFF98_H$	-*6
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11

Oscillation clock frequency vs. Internal operation clock frequency

		Internal operation clock frequency							
			PLL clock						
		Main Clock	Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 19	Multiplied by 20
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	76MHz	80MHz

・Example of oscillation circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

AC characteristics are specified by the following measurement reference voltage values.

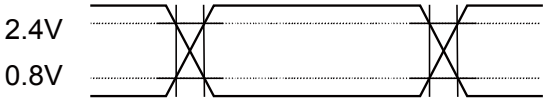
● Input Signal Waveform

Hysteresis Input Pin (Automotive)

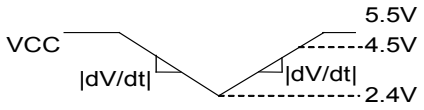
Hysteresis Input Pin (CMOS schmitt)

● Output Signal Waveform

Output Pin



・Maximum ramp rate guaranteed to not generate power-on reset



(4-1-5) Bit setting: SMR:MD2=0, SMR:MD1=1, SMR:MD0=0,
When Serial chip select is used : SCSCR:CSEN=1,
Serial clock output mark level "H" : SMR,SCSFR:SCINV=0,
Serial chip select Inactive level "H" : SCSCR,SCSFR:CSLVL=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↓ setup time	t_{CSSI}	SCK1, SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	t_{CSSU}-50 *1	t_{CSSU}+0 *1	ns	Internal shift clock mode output pin : C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSSU}-50 *1	t_{CSSU}+300 *1	ns	
SCK↑→SCS↑ hold time	t_{CSHI}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSHD}-10 *2	t_{CSHD}+50 *2	ns	
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		t_{CSHD}-300 *2	t_{CSHD}+50 *2	ns	
SCS deselect time	t_{CSDI}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		t_{CSDS}-50 *3	t_{CSDS}+50 *3	ns	

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↓→SCK↑ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↑ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↓→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11		-	40	ns	
		SCS3, SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↑→SOT delay time	t_{DEE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↓ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock
*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock
*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
SCS↑→SCK↓ setup time	t_{CSSE}	SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$+30	-	ns	External shift clock mode output pin: C_L=50pF
SCK↑→SCS↓ hold time	t_{CSHE}			+0	-	ns	
SCS deselect time	t_{CSDE}	SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11		$3t_{CPP}$+30	-	ns	
SCS↑→SOT delay time	t_{DSE}	SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11		-	40	ns	
		SCS3 , SCS40 to SCS43 SOT3 , SOT4		-	300	ns	
SCS↓→SOT delay time	t_{DEE}	SCS1 to ~SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11	-	+0	-	ns	External shift clock mode output pin: C_L=50pF
SCK↓→SCS↑ clock switch time	t_{SCC}	SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11	-	$3t_{CPP}$-10	$3t_{CPP}$+50	ns	Internal shift clock mode Round operation output pin: C_L=50pF
		SCK3 , SCK4 SCS3 , SCS40 to SCS43		$3t_{CPP}$-300	$3t_{CPP}$+50	ns	

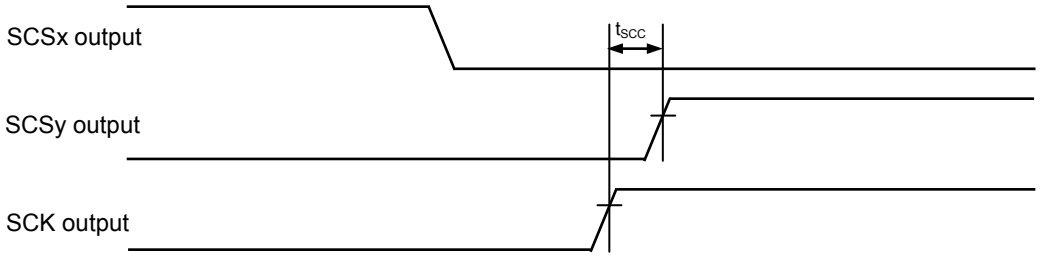
*1: t_{CSSU} =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: t_{CSHD}=SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: t_{CSDS}=SCSTR:CSDS15-0×Serial chip select timing operating clock

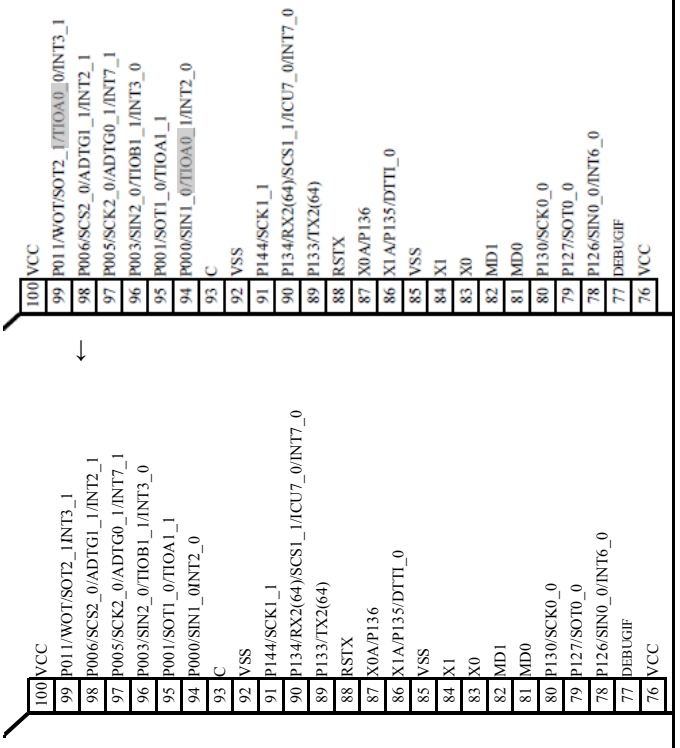
Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3.



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

Page	Section	Change Results
184	■ELECTRICAL CHARACTERISTICS 5.A/D Converter (1) 12-bit A/D Converter Electrical Characteristics	Added the following description. Parameter : Power supply current I_A AVCC*3 *3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter.
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter.
187	■ELECTRICAL CHARACTERISTICS 6.Flash memory	Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing Tj<+105°C"
188	■ELECTRICAL CHARACTERISTICS 7.D/A Converter	Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV_{CC} Symbol IAH Pin name AV_{CC} ↓ Symbol IA Pin name AVCC Symbol IAH Pin name AVCC
190	■EXAMPLE CHARACTERISTICS	Corrected the following description. Watch mode
192	■ORDERING INFORMATION	Corrected the following description. ■ORDERING INFORMATION ↓ ■ORDERING INFORMATION MB91F52xxxB*1 Package ↓ Package*2
198	■ORDERING INFORMATION	Added the following description. *1: It is only supported for customers who have already adopted it now. We do not recommend adopting new products.
198	■ORDERING INFORMATION	Corrected the following description. For details of the package, see "■ PACKAGE DIMENSIONS ". ↓ *2: For details of the package, see "■ PACKAGE DIMENSIONS ".
199 to 205	■ORDERING INFORMATION	Added the following description. ■ORDERING INFORMATION MB91F52xxxC
-	-	Company name and layout design change

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	- Top  ↓
15	■Pin Assignment MB91F52xF	The following note added on the bottom left of Figure. * In a single clock product, pin 86 and pin 87 are the general-purpose ports.
16	■Pin Assignment MB91F52xJ	The following note added on the bottom left of Figure. * In a single clock product, pin 102 and pin 103 are the general-purpose ports.
17	■Pin Assignment MB91F52xK	The following note added on the bottom left of Figure. * In a single clock product, pin 121 and pin 122 are the general-purpose ports.
18	■Pin Assignment MB91F52xL	The following note added on the bottom left of Figure. * In a single clock product, pin 149 and pin 150 are the general-purpose ports.
19 to 35	■PIN Description	A List of "Pin Description" modified. I/O Circuit types[*1] | Function[*2] ↓ I/O Circuit types[*8] | Function[*9]

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>22, 23</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>28</td><td>P175
TRG9_1</td></tr>
<tr><td>11 *1</td><td>13 *1</td><td>17 *1</td><td>20 *1</td><td>23</td><td>29</td><td>P040
A10 *2, *3, *4, *5
PPG23_1
TOT7_0
AIN1_0
SIN0_1</td></tr>
<tr><td>12 *1</td><td>14 *1</td><td>18 *1</td><td>21 *1</td><td>24</td><td>30</td><td>P041
A11 *2, *3, *4, *5
SIN9_0
ICU9_1
BIN1_0
INT12_0</td></tr>
<tr><td>13 *1</td><td>15 *1</td><td>19 *1</td><td>22 *1</td><td>25</td><td>31</td><td>P042
A12 *2, *3, *4, *5
SOT9_0
AN47
ICU8_1
TRG0_1
ZIN1_0</td></tr>
<tr><td>-</td><td>-</td><td>20 *1</td><td>23 *1</td><td>26</td><td>32</td><td>P043
A13 *4, *5
ICU7_1
TRG1_1</td></tr>
<tr><td>-</td><td>16 *1</td><td>21 *1</td><td>24 *1</td><td>27</td><td>33</td><td>P044
A14 *3, *4, *5
SCS9_0
ICU6_1
TRG2_1</td></tr>
<tr><td>14 *1</td><td>17 *1</td><td>22 *1</td><td>25 *1</td><td>28</td><td>34</td><td>P045
A15 *2, *3, *4, *5
SCK9_0
AN46
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TOT1_2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>26 *1</td><td>29</td><td>35</td><td>P046
A16 *5
ICU4_1
TRG4_1</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>36</td><td>P176
TRG10_0</td></tr>
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<tr><td>34, 35</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
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<tr><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">-</td><td rowspan="4">113 *1</td><td rowspan="4">133</td><td rowspan="4">161</td><td>P002</td></tr>
<tr><td>D18 *5</td></tr>
<tr><td>SCK1_0</td></tr>
<tr><td>TIOB0_1</td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">76 *1</td><td rowspan="5">96 *1</td><td rowspan="5">114 *1</td><td rowspan="5">134</td><td rowspan="5">162</td><td>P003</td></tr>
<tr><td>D19 *3, *4, *5</td></tr>
<tr><td>SIN2_0</td></tr>
<tr><td>TIOB1_1</td></tr>
<tr><td>INT3_0</td></tr>
<tr><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">-</td><td rowspan="3">135</td><td rowspan="3">163</td><td>P004</td></tr>
<tr><td>D20</td></tr>
<tr><td>SOT2_0</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">164</td><td>P164</td></tr>
<tr><td>PPG32_1</td></tr>
<tr><td rowspan="7">61 *1</td><td rowspan="7">77 *1</td><td rowspan="7">97 *1</td><td rowspan="7">115 *1</td><td rowspan="7">136 *1</td><td rowspan="7">165 *1</td><td>P005</td></tr>
<tr><td>D21 *2, *3, *4, *5</td></tr>
<tr><td>SCK2_0 *2</td></tr>
<tr><td>ADTG0_1</td></tr>
<tr><td>INT7_1</td></tr>
<tr><td>RX2(64) *4, *5, *6, *7</td></tr>
<tr><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">-</td><td rowspan="2">166</td><td>P165</td></tr>
<tr><td>PPG33_1</td></tr>
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<tr><td>D22 *2, *3, *4, *5</td></tr>
<tr><td>SCS2_0 *2</td></tr>
<tr><td>ADTG1_1</td></tr>
<tr><td>INT2_1</td></tr>
<tr><td>TX2(64) *4, *5, *6, *7</td></tr>
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<tr><td>D23 *5</td></tr>
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<tr><td>PPG34_1</td></tr>
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<tr><td>D24 *5</td></tr>
<tr><td rowspan="7">63 *1</td><td rowspan="7">79 *1</td><td rowspan="7">99 *1</td><td rowspan="7">119 *1</td><td rowspan="7">140</td><td rowspan="7">171</td><td>P011</td></tr>
<tr><td>WOT</td></tr>
<tr><td>D25 *2, *3, *4, *5</td></tr>
<tr><td>SOT2_1 *2</td></tr>
<tr><td>TIOA0_0 *2, *3, *4</td></tr>
<tr><td>INT3_1</td></tr>
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Revision	ECN	Orig. of Change	Submission Date	Description of Change
				(1) 12-bit A/D Converter Electrical Characteristics: Added the value of "Total error". Total error value Min – Typ – Max ±12 LSB Corrected the value of "Zero transition voltage". Min AVRL+0.5LSB-20mV Max AVRL+0.5LSB+20mV ↓ Min AVRL-11.5LSB Max AVRL+12.5LSB Corrected the value of "Full-scale transition voltage". Min AVRH-1.5LSB-20mV Max AVRH-1.5LSB+20mV ↓ Min AVRH-13.5LSB Max AVRH+10.5LSB Added the following description. Parameter : Power supply current I_A AVCC*3 *3: The power supply current described only current value on A/D converter. The total AVcc current value must be calculated the power supply current for A/D converter and D/A converter. Electrical Characteristics 7.D/A Converter: Added the following description. Parameter : Power supply current *1 *1: The power supply current described only current value on D/A converter.The total Avcc current value must be calculated the power supply current for D/A converter and A/D converter. Electrical Characteristics 6.Flash memory: Parameter: Erase cycle*2/Data retain time Deleted the following description. Remarks : "Temperature at writing/erasing Tj<+105°C" Electrical Characteristics 7.D/A Converter: Corrected the following description. Parameter : Power supply current Symbol IA Pin name AV_{CC} Symbol IAH Pin name AV_{CC} ↓ Symbol IA Pin name AVCC Symbol IAH Pin name AVCC Example Characteristics Corrected the following description. Watch mode Ordering Information Corrected the following description. • ORDERING INFORMATION ↓ • ORDERING INFORMATION MB91F52xxxB[*1]

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