Infineon Technologies - MB91F522DSCPMC-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 1x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522dscpmc-gte1

- D/A converter (R-2R type)
  - 8-bit resolution : 2ch
- External interrupt input: 8 channels × 2 units total 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- Multi-function serial communication (built-in transmission/reception FIFO memory) : Max.12 channels
  - 5V tolerant input: 4 channels ch.6, ch.8, ch.9, ch.11 CMOS hysteresis input
    < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detection functions provided
  - DMA transfer support
    <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 16, 20, 24, 32-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detection function is provided
  - DMA transfer support
  - Serial chip select SPI function
    <LIN (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - LIN protocol revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support
  - Hard assist function
    < I^2C >
  - 2 channels ch.3 , ch.4 Standard mode/fast mode supported.
  - 6 channels ch.5 to ch.8, ch.10, ch.11 Standard mode supported.
  - Full-duplex double buffering system, 64-step transmission FIFO memory, 64-step reception FIFO memory
  - Standard mode (Max. 100kbps) / fast mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 128-transmission/reception message buffering :
    1 channel (ch.0),
    64-transmission/reception message buffering :
    2 channels (ch.1 and ch.2)
- PPG: 16-bit × Max. 48 channels
  - LED drive output 4 channels 11ch to 14ch
  - Reload timer : 16-bit × Max.8 channels
  - Free-run timer :
    16-bit × 3 channels
    32-bit × Max 3 channels
- Input capture :
  16-bit × 4 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Output compare :
  16-bit × 6 channels (linked to the free-run timer)
  32-bit × Max 6 channels (linked to the free-run timer)
- Waveform generator : 6 channels
- Up/Down counter
  - 8/16-bit Up/Down counter × 2 channels
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main or sub oscillation frequency can be selected for the operation clock
- Calibration: Real-time clock (RTC) of the subclock drive
  - The main clock to sub clock ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (by damaged quartz, etc.) of suboscillation (32kHz) (dual clock products) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
  - Initial value ON/OFF can be selected by the part number.
- Base timer : Max.2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascade mode
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog (possible to set the valid range for counter clearing)
- NMI (non-maskable interrupt)
- Interrupt controller
- Interrupt request batch read
  - The interrupt existence from two or more peripherals can be read by a series of register.
- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode

- Power-on reset
- Low-voltage detection reset (independently monitor the external power supply and the internal power supply)
  - The external power supply can select initial value ON/OFF by the part number.
- Device Package : 176/144/120/100/80/64
- CMOS 90nm Technology
- Power supplies
  - 5V Power supply
  - The internal 1.2V is generated from 5V with the voltage step-down circuit

1. Product Lineup

Product lineup comparison 64 pins

	MB91F522B	MB91F523B	MB91F524B	MB91F525B	MB91F526B
System Clock	On chip PLL Clock multiple method				
Minimum instruction execution time	12.5ns (80MHz)				
Flash Capacity (Program)	(256+64)KB	(384+64)KB	(512+64)KB	(768+64)KB	(1024+64)KB
Flash Capacity (Data)	64KB				
RAM Capacity	(48+8)KB		(64+8)KB	(96+8)KB	(128+8)KB
External BUS I/F (22address/16data/4cs)	None				
DMA Transfer	16ch				
16-bit Base Timer	None				
Free-run Timer	16bit×3ch, 32bit×1ch				
Input capture	16bit×4ch, 32bit×5ch				
Output Compare	16bit×6ch, 32bit×4ch				
16-bit Reload Timer	7ch				
PPG	16bit×21ch				
Up/down Counter	2ch				
Clock Supervisor	Yes				
External Interrupt	8ch×2units				
A/D converter	12bit×13ch (1unit), 12bit×13ch (1unit)				
D/A converter (8bit)	1ch				
Multi-Function Serial Interface	8ch[*1]				
CAN	64msg×2ch/128msg×1ch				
Hardware Watchdog Timer	Yes				
CRC Formation	Yes				
Low-voltage detection reset	Yes				
Flash Security	Yes				
ECC Flash/WorkFlash	Yes				
ECC RAM	Yes				
Memory Protection Function (MPU)	Yes				
Floating point arithmetic (FPU)	Yes				
Real Time Clock (RTC)	Yes				
General-purpose port (#GPIOs)	44 ports				
SSCG	Yes				
Sub clock	Yes				
CR oscillator	Yes				
OCD (On Chip Debug)	Yes				
TPU (Timing Protection Unit)	Yes				
Key code register	Yes				
Waveform generator	6ch				
NMI request function	Yes				
Operation guaranteed temperature (T_A)	-40°C to +125°C				
Power supply	2.7V to 5.5V [*2]				
Package	LQD064				

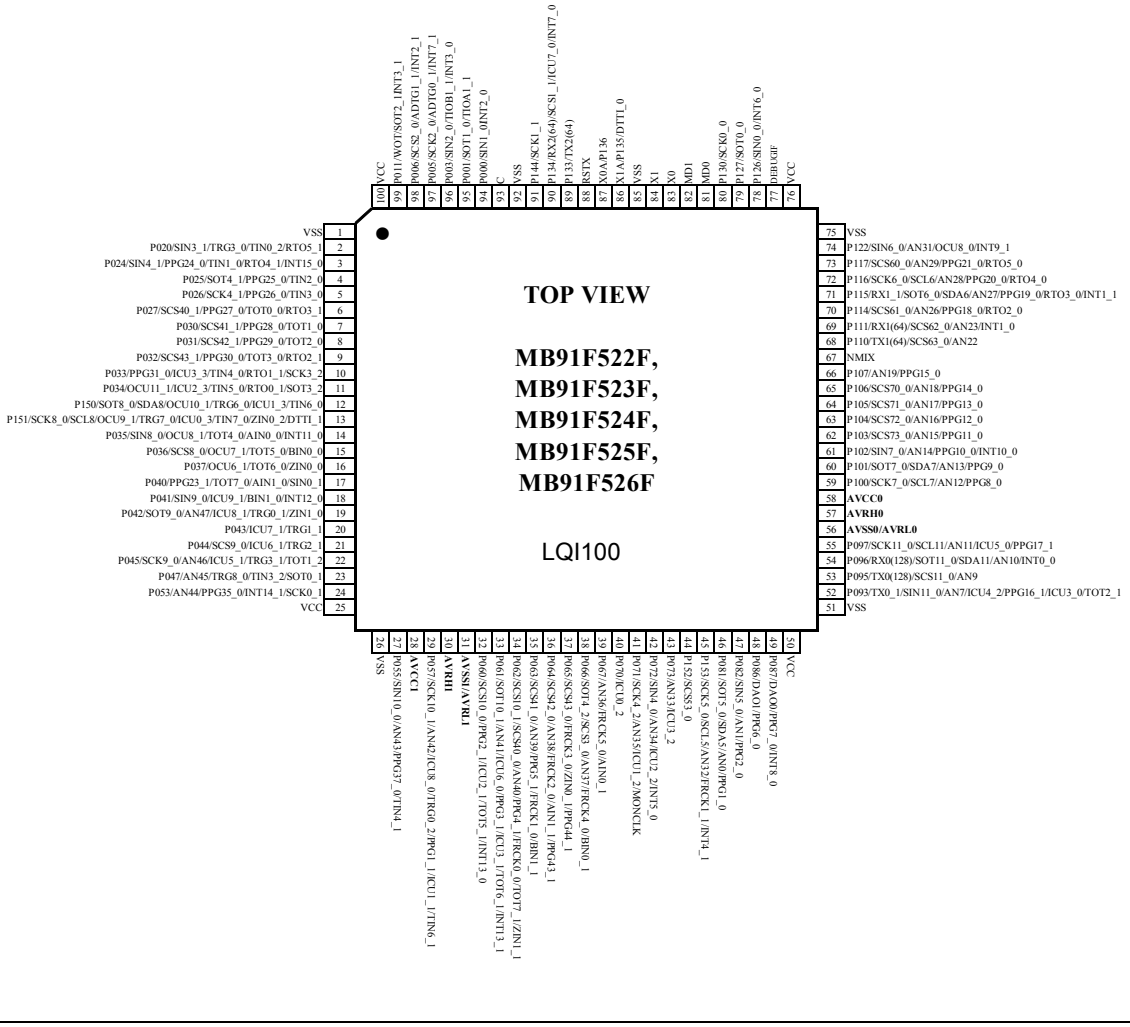
*1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

MB91F52xF

MB91F522F, MB91F523F, MB91F524F, MB91F525F, MB91F526F

(TOP VIEW)

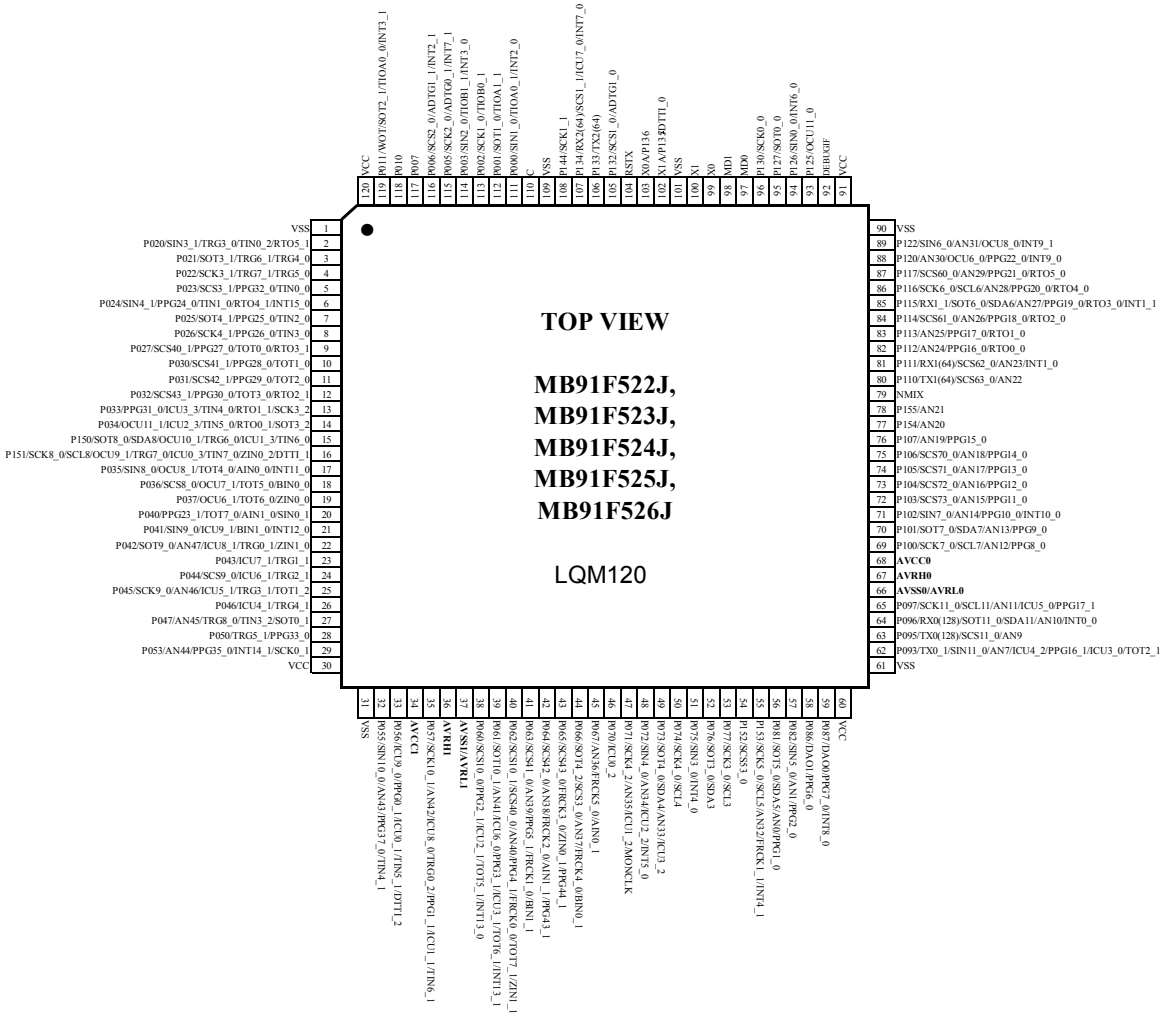


* In a single clock product, pin 86 and pin 87 are the general-purpose ports.

MB91F52xJ

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J

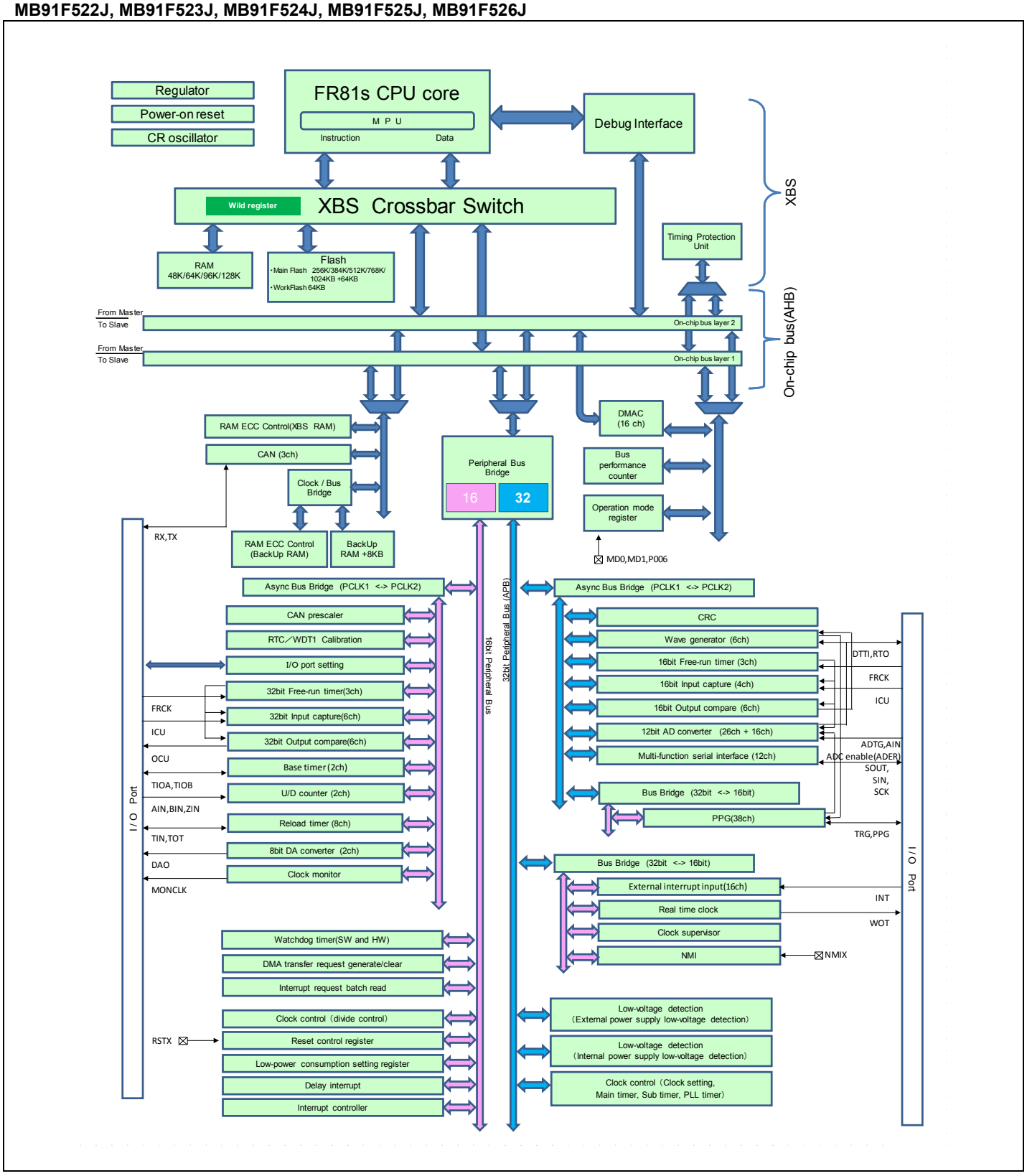
(TOP VIEW)



* In a single clock product, pin 102 and pin 103 are the general-purpose ports.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
9 *1	11 *1	14 *1	17 *1	20	24	P035	-	I	General-purpose I/O port
						A07 *2, *3, *4, *5	-		External bus/Address bit7 output
						SIN8_0 *2, *3	-		Multi-function serial ch.8 serial data input (0)
						OCU8_1	-		Output compare ch.8 output (1)
						TOT4_0	-		Reload timer ch.4 output (0)
						AIN0_0	-		U/D counter ch.0 AIN input (0)
						INT11_0	-		INT11 External interrupt input (0)
10 *1	12 *1	15 *1	18 *1	21	25	P036	-	A	General-purpose I/O port
						A08 *2, *3, *4, *5	-		External bus/Address bit8 output (0)
						SCS8_0 *2, *3	-		Serial chip select 8 I/O (0)
						OCU7_1	-		Output compare ch.7 output (1)
						TOT5_0	-		Reload timer ch.5 output (0)
						BIN0_0	-		U/D counter ch.0 BIN input (0)
-	-	16 *1	19 *1	22	26	P037	-	A	General-purpose I/O port
						A09 *4, *5	-		External bus/Address bit9 output (0)
						OCU6_1	-		Output compare ch.6 output (1)
						TOT6_0	-		Reload timer ch.6 output (0)
						ZIN0_0	-		U/D counter ch.0 ZIN input (0)
-	-	-	-	-	27	P174	-	A	General-purpose I/O port
						TRG8_1	-		PPG trigger 8 input (1)
-	-	-	-	-	28	P175	-	A	General-purpose I/O port
						TRG9_1	-		PPG trigger 9 input (1)
11 *1	13 *1	17 *1	20 *1	23	29	P040	-	A	General-purpose I/O port
						A10 *2, *3, *4, *5	-		External bus/Address bit10 output (0)
						PPG23_1	-		PPG ch.23 output (1)
						TOT7_0	-		Reload timer ch.7 output (0)
						AIN1_0	-		U/D counter ch.1 AIN input (0)
						SIN0_1	-		Multi-function serial ch.0 serial data input (1)
12 *1	14 *1	18 *1	21 *1	24	30	P041	-	I	General-purpose I/O port
						A11 *2, *3, *4, *5	-		External bus/Address bit11 output (0)
						SIN9_0	-		Multi-function serial ch.9 serial data input (0)
						ICU9_1	-		Input capture ch.9 input (1)
						BIN1_0	-		U/D counter ch.1 BIN input (0)
						INT12_0	-		INT12 External interrupt input (0)

MB91F522J, MB91F523J, MB91F524J, MB91F525J, MB91F526J



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	Multi-UART7 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001C24_H$	PDUT27 [W] H,W XXXXXXXX XXXXXXXX		PTMR27 [R] H,W 11111111 11111111		PPG27
$001C28_H$	PCN227 [R/W] B,H,W --000000 -----110		PSDR27 [R/W] H,W 00000000 00000000		
$001C2C_H$	PTPC27 [R/W] H,W 00000000 00000000		—	—	PPG27
$001C30_H$	PCN28 [R/W] B,H,W 00000000 000000-0		PCSR28 [W] H,W XXXXXXXX XXXXXXXX		PPG28
$001C34_H$	PDUT28 [W] H,W XXXXXXXX XXXXXXXX		PTMR28 [R] H,W 11111111 11111111		
$001C38_H$	PCN228 [R/W] B,H,W --000000 -----110		PSDR28 [R/W] H,W 00000000 00000000		
$001C3C_H$	PTPC28 [R/W] H,W 00000000 00000000		—	—	
$001C40_H$	PCN29 [R/W] B,H,W 00000000 000000-0		PCSR29 [W] H,W XXXXXXXX XXXXXXXX		PPG29
$001C44_H$	PDUT29 [W] H,W XXXXXXXX XXXXXXXX		PTMR29 [R] H,W 11111111 11111111		
$001C48_H$	PCN229 [R/W] B,H,W --000000 -----110		PSDR29 [R/W] H,W 00000000 00000000		
$001C4C_H$	PTPC29 [R/W] H,W 00000000 00000000		—	—	
$001C50_H$	PCN30 [R/W] B,H,W 00000000 000000-0		PCSR30 [W] H,W XXXXXXXX XXXXXXXX		PPG30
$001C54_H$	PDUT30 [W] H,W XXXXXXXX XXXXXXXX		PTMR30 [R] H,W 11111111 11111111		
$001C58_H$	PCN230 [R/W] B,H,W --000000 -----110		PSDR30 [R/W] H,W 00000000 00000000		
$001C5C_H$	PTPC30 [R/W] H,W 00000000 00000000		—	—	
$001C60_H$	PCN31 [R/W] B,H,W 00000000 000000-0		PCSR31 [W] H,W XXXXXXXX XXXXXXXX		PPG31
$001C64_H$	PDUT31 [W] H,W XXXXXXXX XXXXXXXX		PTMR31 [R] H,W 11111111 11111111		
$001C68_H$	PCN231 [R/W] B,H,W --000000 -----110		PSDR31 [R/W] H,W 00000000 00000000		
$001C6C_H$	PTPC31 [R/W] H,W 00000000 00000000		—	—	
$001C70_H$	PCN32 [R/W] B,H,W 00000000 000000-0		PCSR32 [W] H,W XXXXXXXX XXXXXXXX		PPG32
$001C74_H$	PDUT32 [W] H,W XXXXXXXX XXXXXXXX		PTMR32 [R] H,W 11111111 11111111		

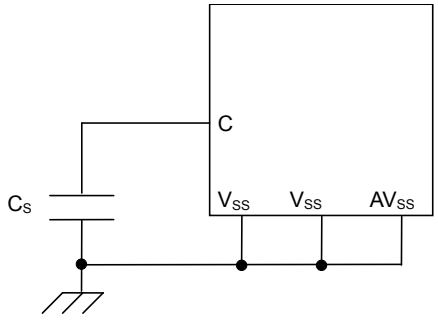
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				
002100$_H$	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104$_H$	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108$_H$	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210C$_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110$_H$	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114$_H$	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118$_H$	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C$_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120$_H$	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124$_H$	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128$_H$	—	—	—	—	
00212C$_H$	—	—	—	—	
002130$_H$, 002134$_H$	Reserved (IF1 data mirror)				CAN1 (64msb)
002138$_H$	—	—	—	—	
00213C$_H$	—	—	—	—	
002140$_H$	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144$_H$	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148$_H$	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

100 pins

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Reset	0	0	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	1	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	2	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	3	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	4	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	5	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	6	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	7	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	8	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	9	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request Error generation during internal bus diagnosis XBS RAM double-bit error generation Backup RAM double-bit error generation TPU violation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15 External low-voltage detection interrupt	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1*7
Reload timer 0/1/4/5	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2*2
Reload timer 2/3/6/7	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3*2
Multi-function serial interface ch.0 (reception completed) Multi-function serial interface ch.0 (status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*1
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5*1
Multi-function serial interface ch.1 (reception completed) Multi-function serial interface ch.1 (status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*1
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7*1
Multi-function serial interface ch.2 (reception completed) Multi-function serial interface ch.2 (status)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8*1
Multi-function serial interface ch.2 (transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9*1
Multi-function serial interface ch.3 (reception completed) Multi-function serial interface ch.3 (status)	26	1A	ICR10	394_H	$000FFF94_H$	10*1

minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.
*2: See the following diagram for details on the connection of smoothing capacitor C_S.
*3: When it is used under this condition, contact your sales representative.

· C Pin Connection Diagram



<WARNING>

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

AC Characteristics

(1) Main Clock Timing

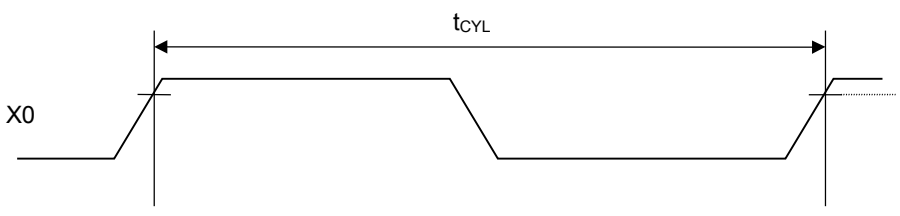
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS} =AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1		-	4	16	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		62.5	250	-	ns	
Internal operating clock frequency*1	F_{CP}	-		2	-	80	MHz	CPU clock
	F_{CPP}			1		40		Peripheral bus clock
	F_{CPT}			1		40		External bus clock (When V_{CC}=5.0V is used) *2
				1		32		External bus clock (When V_{CC}=3.3V is used)
Internal operating clock cycle time*1	t_{CP}	-	-	12.5	-	500	ns	CPU clock
	t_{CPP}			25		1000		Peripheral bus clock
	t_{CPT}			25		1000		External bus clock (When V_{CC}=5.0V is used)
				31.25		1000		External bus clock (When V_{CC}=3.3V is used)
CAN PLL jitter (during lock)	t_{PJ}	-		-10	-	10	ns	F_{CP}=80MHz (4MHz□Multiplied by 20)
Built-in CR oscillation frequency	F_{CCR}	-		50	100	150	kHz	

*1: The maximum / minimum value is defined when using the main clock and PLL clock.

*2: Please use it with external load capacity 12pF or less for VCC=3.3V±0.3V (40MHz operation).

• X0,X1 clock timing



AC characteristics are specified by the following measurement reference voltage values.

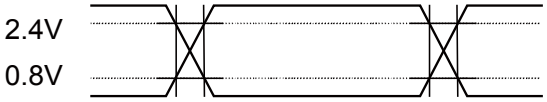
● Input Signal Waveform

Hysteresis Input Pin (Automotive)

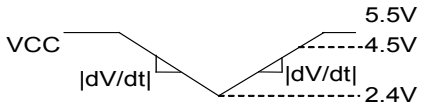
Hysteresis Input Pin (CMOS schmitt)

● Output Signal Waveform

Output Pin



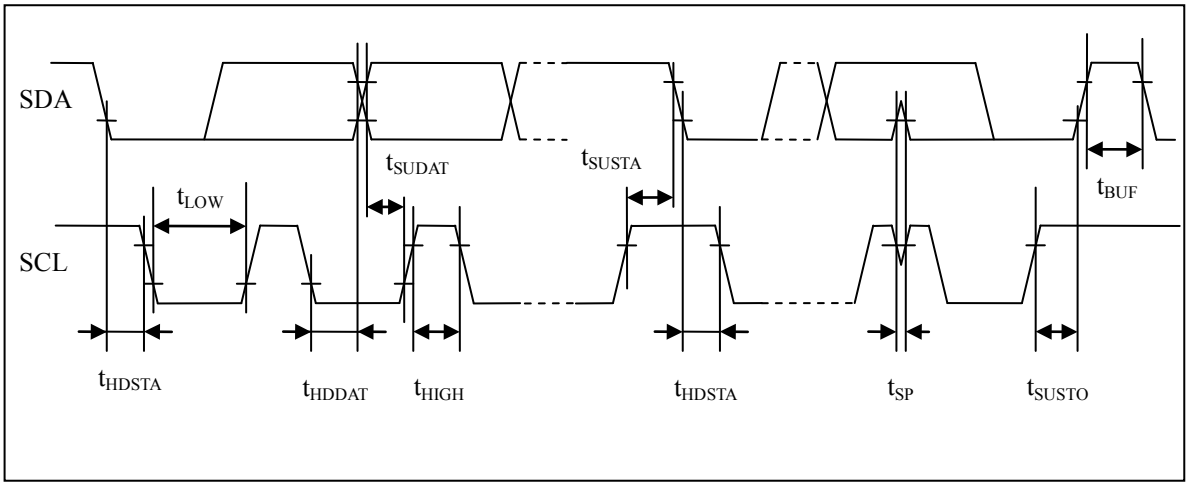
・Maximum ramp rate guaranteed to not generate power-on reset



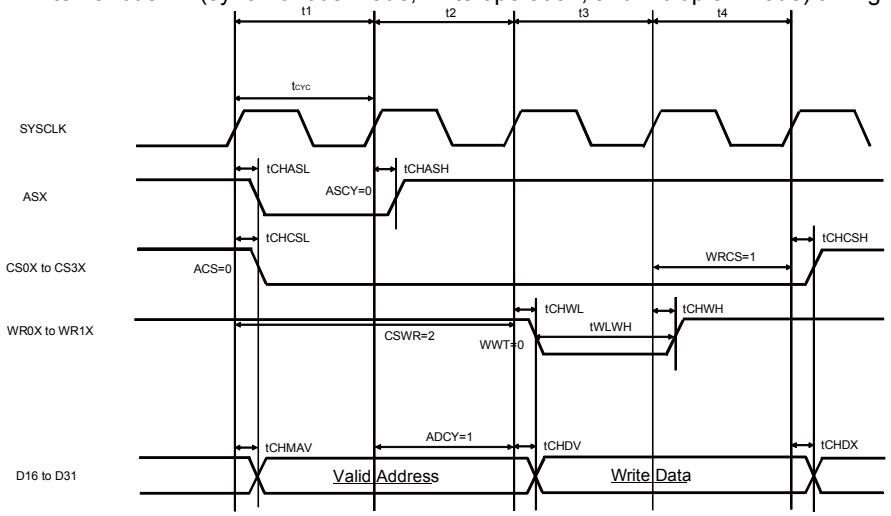
"t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

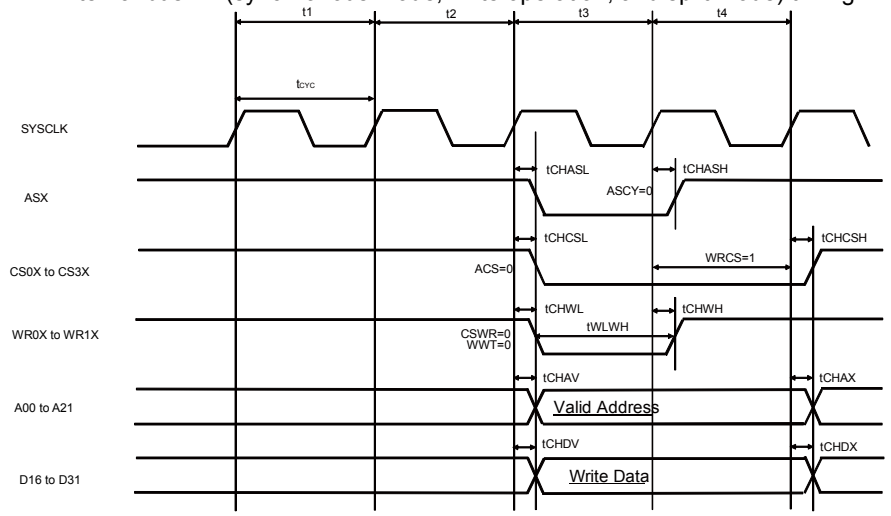
・ I^2C timing



External bus I/F (synchronous mode, write operation, and multiplex mode) timing



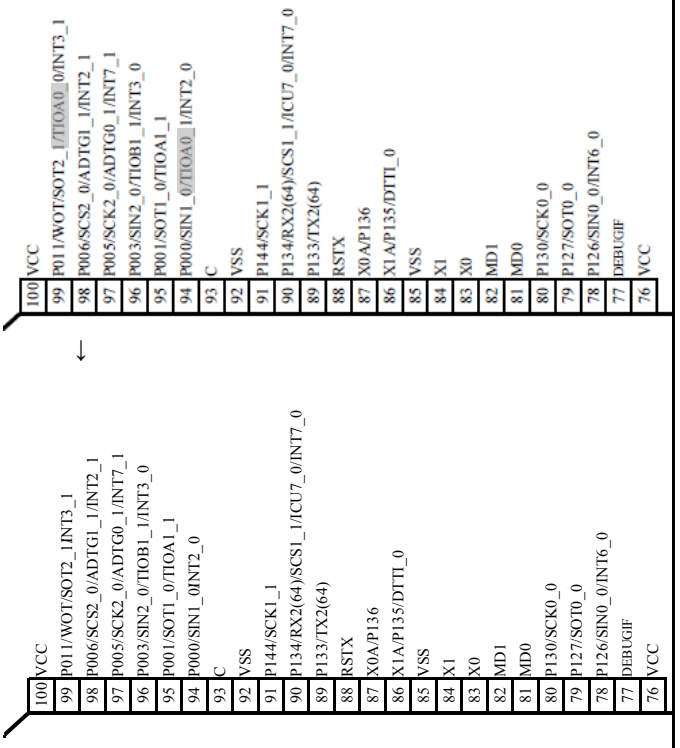
External bus I/F (synchronous mode, write operation, and split mode) timing



15. Ordering Information MB91F52xxxD

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWDPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJDPMC		OFF	ON	
MB91F525LWDPMC		ON	ON	
MB91F525LJDPMC		OFF	ON	
MB91F524LWDPMC		ON	ON	
MB91F524LJDPMC		OFF	ON	
MB91F523LWDPMC		ON	ON	
MB91F523LJDPMC		OFF	ON	
MB91F522LWDPMC		ON	ON	
MB91F522LJDPMC		OFF	ON	
MB91F526LSDPMC	None	ON	ON	
MB91F526LHDPMC		OFF	ON	
MB91F525LSDPMC		ON	ON	
MB91F525LHDPMC		OFF	ON	
MB91F524LSDPMC		ON	ON	
MB91F524LHDPMC		OFF	ON	
MB91F523LSDPMC		ON	ON	
MB91F523LHDPMC		OFF	ON	
MB91F522LSDPMC		ON	ON	
MB91F522LHDPMC		OFF	ON	
MB91F526KWDPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJDPMC		OFF	ON	
MB91F525KWDPMC		ON	ON	
MB91F525KJDPMC		OFF	ON	
MB91F524KWDPMC		ON	ON	
MB91F524KJDPMC		OFF	ON	
MB91F523KWDPMC		ON	ON	
MB91F523KJDPMC		OFF	ON	
MB91F522KWDPMC		ON	ON	
MB91F522KJDPMC		OFF	ON	
MB91F526KSDPMC	None	ON	ON	
MB91F526KHDPMC		OFF	ON	
MB91F525KSDPMC		ON	ON	
MB91F525KHDPMC		OFF	ON	
MB91F524KSDPMC		ON	ON	
MB91F524KHDPMC		OFF	ON	
MB91F523KSDPMC		ON	ON	
MB91F523KHDPMC		OFF	ON	
MB91F522KSDPMC		ON	ON	
MB91F522KHDPMC		OFF	ON	

Page	Section	Change Results
8	■Product Lineup	Corrected the following description for Product lineup comparison(100 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
8	■Product Lineup	Added the following sentences under Product lineup comparison(100 pin) *1: Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
9	■Product Lineup	Corrected the following description for Product lineup comparison(120 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
9	■Product Lineup	Added the following sentences under Product lineup comparison(120 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8 and channel 11 support the I^2C (standard mode).
10	■Product Lineup	Corrected the following description for Product lineup comparison(144 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
10	■Product Lineup	Added the following sentences under Product lineup comparison(144 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).
11	■Product Lineup	Corrected the following description for Product lineup comparison(176 pin). Multi-Function Serial Interface: 12ch ↓ Multi-Function Serial Interface: 12ch*1
11	■Product Lineup	Added the following sentences under Product lineup comparison(176 pin) *1: Only channel 3 and channel 4 support the I^2C (high-speed mode/standard mode). Only channel 5, channel 6, channel 7, channel 8, channel 10 and channel 11 support the I^2C (standard mode).

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	- Top  ↓
15	■Pin Assignment MB91F52xF	The following note added on the bottom left of Figure. * In a single clock product, pin 86 and pin 87 are the general-purpose ports.
16	■Pin Assignment MB91F52xJ	The following note added on the bottom left of Figure. * In a single clock product, pin 102 and pin 103 are the general-purpose ports.
17	■Pin Assignment MB91F52xK	The following note added on the bottom left of Figure. * In a single clock product, pin 121 and pin 122 are the general-purpose ports.
18	■Pin Assignment MB91F52xL	The following note added on the bottom left of Figure. * In a single clock product, pin 149 and pin 150 are the general-purpose ports.
19 to 35	■PIN Description	A List of "Pin Description" modified. I/O Circuit types[*1] | Function[*2] ↓ I/O Circuit types[*8] | Function[*9]