### What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "**Embedded - Microcontrollers**"

| Details | |
| --- | --- |
| Product Status | Obsolete |
| Core Processor | FR81S |
| Core Size | 32-Bit Single-Core |
| Speed | 80MHz |
| Connectivity | CANbus, CSIO, I²C, LINbus, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 76 |
| Program Memory Size | 320KB (320K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 64K x 8 |
| RAM Size | 56K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 37x12b; D/A 2x8b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522fjcpmc-gs-f4e1 |

# 1. Product Lineup

**Product lineup comparison 64 pins**

| | MB91F522B | MB91F523B | MB91F524B | MB91F525B | MB91F526B |
|---|---|---|---|---|---|
| System Clock | On chip PLL Clock multiple method | | | | |
| Minimum instruction execution time | 12.5ns (80MHz) | | | | |
| Flash Capacity (Program) | (256+64)KB | (384+64)KB | (512+64)KB | (768+64)KB | (1024+64)KB |
| Flash Capacity (Data) | 64KB | | | | |
| RAM Capacity | (48+8)KB | | (64+8)KB | (96+8)KB | (128+8)KB |
| External BUS I/F (22address/16data/4cs) | None | | | | |
| DMA Transfer | 16ch | | | | |
| 16-bit Base Timer | None | | | | |
| Free-run Timer | 16bit×3ch, 32bit×1ch | | | | |
| Input capture | 16bit×4ch, 32bit×5ch | | | | |
| Output Compare | 16bit×6ch, 32bit×4ch | | | | |
| 16-bit Reload Timer | 7ch | | | | |
| PPG | 16bit×21ch | | | | |
| Up/down Counter | 2ch | | | | |
| Clock Supervisor | Yes | | | | |
| External Interrupt | 8ch×2units | | | | |
| A/D converter | 12bit×13ch (1unit), 12bit×13ch (1unit) | | | | |
| D/A converter (8bit) | 1ch | | | | |
| Multi-Function Serial Interface | 8ch[*1] | | | | |
| CAN | 64msg×2ch/128msg×1ch | | | | |
| Hardware Watchdog Timer | Yes | | | | |
| CRC Formation | Yes | | | | |
| Low-voltage detection reset | Yes | | | | |
| Flash Security | Yes | | | | |
| ECC Flash/WorkFlash | Yes | | | | |
| ECC RAM | Yes | | | | |
| Memory Protection Function (MPU) | Yes | | | | |
| Floating point arithmetic (FPU) | Yes | | | | |
| Real Time Clock (RTC) | Yes | | | | |
| General-purpose port (#GPIOs) | 44 ports | | | | |
| SSCG | Yes | | | | |
| Sub clock | Yes | | | | |
| CR oscillator | Yes | | | | |
| OCD (On Chip Debug) | Yes | | | | |
| TPU (Timing Protection Unit) | Yes | | | | |
| Key code register | Yes | | | | |
| Waveform generator | 6ch | | | | |
| NMI request function | Yes | | | | |
| Operation guaranteed temperature ($T_A$) | -40°C to +125°C | | | | |
| Power supply | 2.7V to 5.5V [*2] | | | | |
| Package | LQD064 | | | | |

*1: Only channel 5, channel 6 and channel 11 support the I²C (standard mode).

*2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.

**Table for clock supervisor and external low voltage detection reset initial value ON/OFF**

| Clock | CSV Initial value | LVD Initial value | Function |
|---|---|---|---|
| single | ON | ON | S |
| | | OFF | U |
| | OFF | ON | H |
| | | OFF | K |
| Dual | ON | ON | W |
| | | OFF | Y |
| | OFF | ON | J |
| | | OFF | L |

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ＭＢ９１Ｆ５２Ｘ□△○
              │││└→Ｒｅｖｉｓｉｏｎ：Ｂ，Ｃ，Ｄ，Ｅ
              ││└──→Ｆｕｎｃｔｉｏｎ：See the table for clock supervisor and external
              ││               low voltage detection reset initial value ON/OFF.
              │└──→ＰＫＧ Ｔｙｐｅ：Ｂ ６４ｐｉｎ
              │               Ｄ ８０ ｐｉｎ
              │               Ｆ １００ ｐｉｎ
              │               Ｊ １２０ ｐｉｎ
              │               Ｋ １４４ ｐｉｎ
              │               Ｌ １７６ ｐｉｎ
              └──→Ｍｅｍｏｒｙ Ｓｉｚｅ：２ ２５６ＫＢ
                              ３ ３８４ＫＢ
                              ４ ５１２ＫＢ
                              ５ ７６８ＫＢ
                              ６ １ＭＢ
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| Pin no. | | | | | | Pin Name | Polarity | I/O circuit types[8] | Function[9] |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | | | | |
| 3 [1] | 3 [1] | 3 [1] | 6 [1] | 9 | 11 | P024 | - | F | General-purpose I/O port |
| | | | | | | WR0X [2, 3, 4, 5] | - | | External bus/Write strobe 0 output |
| | | | | | | SIN4_1 | - | | Multi-function serial ch.4 serial data input (1) |
| | | | | | | PPG24_0 | - | | PPG ch.24 output (0) |
| | | | | | | TIN1_0 | - | | Reload timer ch.1 event input (0) |
| | | | | | | RTO4_1 | - | | Waveform generator ch.4 output pin (1) |
| | | | | | | INT15_0 | - | | INT15 External interrupt input (0) |
| - | - | 4 [1] | 7 [1] | 10 | 12 | P025 | - | A | General-purpose I/O port |
| | | | | | | WR1X [4, 5] | - | | External bus/Write strobe 1 output |
| | | | | | | SOT4_1 | - | | Multi-function serial ch.4 serial data output (1) |
| | | | | | | PPG25_0 | - | | PPG ch.25 output (0) |
| | | | | | | TIN2_0 | - | | Reload timer ch.2 event input (0) |
| - | - | - | - | - | 13 | P172 | - | A | General-purpose I/O port |
| | | | | | | PPG38_1 | - | | PPG ch.38 output (1) |
| - | 4 [1] | 5 [1] | 8 [1] | 11 | 14 | P026 | - | F | General-purpose I/O port |
| | | | | | | A00 [3, 4, 5] | - | | External bus/Address bit0 output (0) |
| | | | | | | SCK4_1 | - | | Multi-function serial ch.4 clock I/O (1) |
| | | | | | | PPG26_0 | - | | PPG ch.26 output (0) |
| | | | | | | TIN3_0 | - | | Reload timer ch.3 event input (0) |
| 4 [1] | 5 [1] | 6 [1] | 9 [1] | 12 | 15 | P027 | - | A | General-purpose I/O port |
| | | | | | | A01 [2, 3, 4, 5] | - | | External bus/Address bit1 output (0) |
| | | | | | | SCS40_1 | - | | Serial chip select 40 I/O (1) |
| | | | | | | PPG27_0 | - | | PPG ch.27 output (0) |
| | | | | | | TOT0_0 | - | | Reload timer ch.0 output (0) |
| | | | | | | RTO3_1 | - | | Waveform generator ch.3 output pin (1) |
| - | - | - | - | - | 16 | P173 | - | A | General-purpose I/O port |
| | | | | | | PPG39_1 | - | | PPG ch.39 output (1) |
| - | - | 7 [1] | 10 [1] | 13 | 17 | P030 | - | A | General-purpose I/O port |
| | | | | | | A02 [4, 5] | - | | External bus/Address bit2 output (0) |
| | | | | | | SCS41_1 | - | | Serial chip select 41 output (1) |
| | | | | | | PPG28_0 | - | | PPG ch.28 output (0) |
| | | | | | | TOT1_0 | - | | Reload timer ch.1 output (0) |
| - | 6 [1] | 8 [1] | 11 [1] | 14 | 18 | P031 | - | A | General-purpose I/O port |
| | | | | | | A03 [3, 4, 5] | - | | External bus/Address bit3 output (0) |
| | | | | | | SCS42_1 | - | | Serial chip select 42 output (1) |
| | | | | | | PPG29_0 | - | | PPG ch.29 output (0) |
| | | | | | | TOT2_0 [3] | - | | Reload timer ch.2 output (0) |

| Address | Address offset value / Register name | | | | Block |
|---|---|---|---|---|---|
| | **+0** | **+1** | **+2** | **+3** | |
| 000E3C$_H$ | — | — | — | — | Reserved |
| 000E40$_H$ | PDDR00 [R] B,H,W XXXXXXXX | PDDR01 [R] B,H,W XXXXXXXX | PDDR02 [R] B,H,W XXXXXXXX | PDDR03 [R] B,H,W XXXXXXXX | Port Direct Read Register |
| 000E44$_H$ | PDDR04 [R] B,H,W XXXXXXXX | PDDR05 [R] B,H,W XXXXXXXX | PDDR06 [R] B,H,W XXXXXXXX | PDDR07 [R] B,H,W XXXXXXXX | |
| 000E48$_H$ | PDDR08 [R] B,H,W XXXXXXXX | PDDR09 [R] B,H,W XXXXXXXX | PDDR10 [R] B,H,W XXXXXXXX | PDDR11 [R] B,H,W XXXXXXXX | |
| 000E4C$_H$ | PDDR12 [R] B,H,W XXXXXXXX | PDDR13 [R] B,H,W -XXXXXXX | PDDR14 [R] B,H,W ---XXX-- | PDDR15 [R] B,H,W --XXXXXX | |
| 000E50$_H$ | — | — | — | — | |
| 000E54$_H$ | — | — | — | — | |
| 000E58$_H$ | PDDR16 [R] B,H,W XXXXXXXX | PDDR17 [R] B,H,W XXXXXXXX | PDDR18 [R] B,H,W XXXXXXXX | PDDR19 [R] B,H,W XXXXXXXX | |
| 000E5C$_H$ | — | — | — | — | Reserved |
| 000E60$_H$ | EPFR00 [R/W] B,H,W 00000000 | EPFR01 [R/W] B,H,W -0-0-000 | EPFR02 [R/W] B,H,W ----0000 | EPFR03 [R/W] B,H,W ---000-0 | Extended Port Function Register |
| 000E64$_H$ | EPFR04 [R/W] B,H,W ----00-0 | EPFR05 [R/W] B,H,W ----0000 | EPFR06 [R/W] B,H,W ----000- | EPFR07 [R/W] B,H,W ---00000 | |
| 000E68$_H$ | EPFR08 [R/W] B,H,W ---00000 | EPFR09 [R/W] B,H,W -----00- | EPFR10 [R/W] B,H,W ----0000 | EPFR11 [R/W] B,H,W ----0000 | |
| 000E6C$_H$ | EPFR12 [R/W] B,H,W ----0000 | EPFR13 [R/W] B,H,W ------00 | EPFR14 [R/W] B,H,W ------00 | EPFR15 [R/W] B,H,W ----000 | |
| 000E70$_H$ | — | — | — | — | |
| 000E74$_H$ | — | — | — | — | |
| 000E78$_H$ | — | — | EPFR26 [R/W] B,H,W 00000000 | EPFR27 [R/W] B,H,W ---0---- | |
| 000E7C$_H$ | EPFR28 [R/W] B,H,W --000-0- | EPFR29 [R/W] B,H,W 00000000 | — | — | |
| 000E80$_H$ | — | EPFR33 [R/W] B,H,W -----00- | EPFR34 [R/W] B,H,W -----00- | EPFR35 [R/W] B,H,W ---00000 | |
| 000E84$_H$ | EPFR36 [R/W] B,H,W ----000- | — | — | — | |
| 000E88$_H$ | — | — | EPFR42 [R/W] B,H,W ------00 | EPFR43 [R/W] B,H,W 0--0000- | |
| 000E8C$_H$ | EPFR44 [R/W] B,H,W -00---0- | EPFR45 [R/W] B,H,W -0000000 | — | — | |
| 000E90$_H$ | — | — | — | — | |

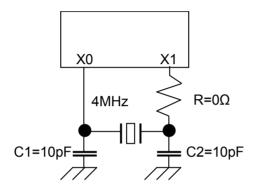| Address | Address offset value / Register name | | | | Block |
|---------|------|------|------|------|-------|
| | **+0** | **+1** | **+2** | **+3** | |
| 0013E8H | ADTECS14[R/W] B,H,W<br>-------0 ---00000 | | ADTECS15[R/W] B,H,W<br>-------0 ---00000 | | 12-bit A/D converter 1/2 unit |
| 0013ECH | ADTECS16[R/W] B,H,W<br>-------0 ---00000 | | ADTECS17[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013F0H | ADTECS18[R/W] B,H,W<br>-------0 ---00000 | | ADTECS19[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013F4H | ADTECS20[R/W] B,H,W<br>-------0 ---00000 | | ADTECS21[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013F8H | ADTECS22[R/W] B,H,W<br>-------0 ---00000 | | ADTECS23[R/W] B,H,W<br>-------0 ---00000 | | |
| 0013FCH | ADTECS24[R/W] B,H,W<br>-------0 ---00000 | | ADTECS25[R/W] B,H,W<br>-------0 ---00000 | | |
| 001400H | ADTECS26[R/W] B,H,W<br>-------0 ---00000 | | ADTECS27[R/W] B,H,W<br>-------0 ---00000 | | |
| 001404H | ADTECS28[R/W] B,H,W<br>-------0 ---00000 | | ADTECS29[R/W] B,H,W<br>-------0 ---00000 | | |
| 001408H | ADTECS30[R/W] B,H,W<br>-------0 ---00000 | | ADTECS31[R/W] B,H,W<br>-------0 ---00000 | | |
| 00140CH | ADRCUT0[R/W] B,H,W<br>----0000 00000000 | | ADRCLT0[R/W] B,H,W<br>----0000 00000000 | | |
| 001410H | ADRCUT1[R/W] B,H,W<br>----0000 00000000 | | ADRCLT1[R/W] B,H,W<br>----0000 00000000 | | |
| 001414H | ADRCUT2[R/W] B,H,W<br>----0000 00000000 | | ADRCLT2[R/W] B,H,W<br>----0000 00000000 | | |
| 001418H | ADRCUT3[R/W] B,H,W<br>----0000 00000000 | | ADRCLT3[R/W] B,H,W<br>----0000 00000000 | | |
| 00141CH | ADRCCS0[R/W]<br>B,H,W<br>00000000 | ADRCCS1[R/W]<br>B,H,W<br>00000000 | ADRCCS2[R/W]<br>B,H,W<br>00000000 | ADRCCS3[R/W]<br>B,H,W<br>00000000 | |
| 001420H | ADRCCS4[R/W]<br>B,H,W<br>00000000 | ADRCCS5[R/W]<br>B,H,W<br>00000000 | ADRCCS6[R/W]<br>B,H,W<br>00000000 | ADRCCS7[R/W]<br>B,H,W<br>00000000 | |
| 001424H | ADRCCS8[R/W]<br>B,H,W<br>00000000 | ADRCCS9[R/W]<br>B,H,W<br>00000000 | ADRCCS10[R/W]<br>B,H,W<br>00000000 | ADRCCS11[R/W]<br>B,H,W<br>00000000 | |
| 001428H | ADRCCS12[R/W]<br>B,H,W<br>00000000 | ADRCCS13[R/W]<br>B,H,W<br>00000000 | ADRCCS14[R/W]<br>B,H,W<br>00000000 | ADRCCS15[R/W]<br>B,H,W<br>00000000 | |
| 00142CH | ADRCCS16[R/W]<br>B,H,W<br>00000000 | ADRCCS17[R/W]<br>B,H,W<br>00000000 | ADRCCS18[R/W]<br>B,H,W<br>00000000 | ADRCCS19[R/W]<br>B,H,W<br>00000000 | |
| 001430H | ADRCCS20[R/W]<br>B,H,W<br>00000000 | ADRCCS21[R/W]<br>B,H,W<br>00000000 | ADRCCS22[R/W]<br>B,H,W<br>00000000 | ADRCCS23[R/W]<br>B,H,W<br>00000000 | |

| Interrupt factor | Interrupt number | | Interrupt level | Offset | Default address for TBR | RN |
|---|---|---|---|---|---|---|
| | Decimal | Hexadecimal | | | | |
| Multi-function serial interface ch.3 (transmission completed) | 27 | 1B | ICR11 | 390$_H$ | 000FFF90$_H$ | 11 |
| Multi-function serial interface ch.4 (reception completed) | 28 | 1C | ICR12 | 38C$_H$ | 000FFF8C$_H$ | 12[*1] |
| Multi-function serial interface ch.4 (status) | | | | | | |
| Multi-function serial interface ch.4 (transmission completed) | 29 | 1D | ICR13 | 388$_H$ | 000FFF88$_H$ | 13 |
| Multi-function serial interface ch.5 (reception completed) | 30 | 1E | ICR14 | 384$_H$ | 000FFF84$_H$ | 14[*1] |
| Multi-function serial interface ch.5 (status) | | | | | | |
| Multi-function serial interface ch.5 (transmission completed) | 31 | 1F | ICR15 | 380$_H$ | 000FFF80$_H$ | 15 |
| Multi-function serial interface ch.6 (reception completed) | 32 | 20 | ICR16 | 37C$_H$ | 000FFF7C$_H$ | 16[*1] |
| Multi-function serial interface ch.6 (status) | | | | | | |
| Multi-function serial interface ch.6 (transmission completed) | 33 | 21 | ICR17 | 378$_H$ | 000FFF78$_H$ | 17 |
| CAN0 | 34 | 22 | ICR18 | 374$_H$ | 000FFF74$_H$ | - |
| CAN1 | 35 | 23 | ICR19 | 370$_H$ | 000FFF70$_H$ | - |
| RAM diagnosis end | | | | | | |
| RAM initialization completion | | | | | | |
| Error generation during RAM diagnosis | | | | | | |
| Backup RAM diagnosis end | | | | | | |
| Backup RAM initialization completion | | | | | | |
| Error generation during Backup RAM diagnosis | | | | | | |
| CAN2 | 36 | 24 | ICR20 | 36C$_H$ | 000FFF6C$_H$ | - |
| Up/down counter 0 | | | | | | |
| Up/down counter 1 | | | | | | |
| Real time clock | 37 | 25 | ICR21 | 368$_H$ | 000FFF68$_H$ | - |
| Multi-function serial interface ch.7 (reception completed) | 38 | 26 | ICR22 | 364$_H$ | 000FFF64$_H$ | 22[*1] |
| Multi-function serial interface ch.7 (status) | | | | | | |
| 16-bit Free-run timer 0 (0 detection) / (compare clear) | 39 | 27 | ICR23 | 360$_H$ | 000FFF60$_H$ | 23 |
| Multi-function serial interface ch.7 (transmission completed) | | | | | | |
| PPG 0/1/10/11/20/21/30/31 | 40 | 28 | ICR24 | 35C$_H$ | 000FFF5C$_H$ | 24[*3] |
| 16-bit Free-run timer 1 (0 detection) / (compare clear) | | | | | | |
| PPG 2/3/12/13/22/23/32/33/43 | 41 | 29 | ICR25 | 358$_H$ | 000FFF58$_H$ | 25[*3] |
| 16-bit Free-run timer 2 (0 detection) / (compare clear) | | | | | | |
| PPG 4/5/14/15/24/25/35/44 | 42 | 2A | ICR26 | 354$_H$ | 000FFF54$_H$ | 26[*3] |
| PPG 6/7/16/17/26/27/37 | 43 | 2B | ICR27 | 350$_H$ | 000FFF50$_H$ | 27[*3] |
| PPG 8/9/18/19/28/29 | 44 | 2C | ICR28 | 34C$_H$ | 000FFF4C$_H$ | 28[*3] |

Oscillation clock frequency vs. Internal operation clock frequency

| | | | Internal operation clock frequency | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | PLL clock | | | | | |
| | | Main Clock | Multiplied by 1 | Multiplied by 2 | Multiplied by 3 | Multiplied by 4 | ... | Multiplied by 19 | Multiplied by 20 |
| Oscillation clock frequency | 4MHz | 2MHz | 4MHz | 8MHz | 12MHz | 16MHz | ... | 76MHz | 80MHz |

· Example of oscillation circuit



**Note:** As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.

Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.
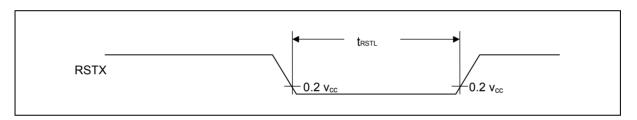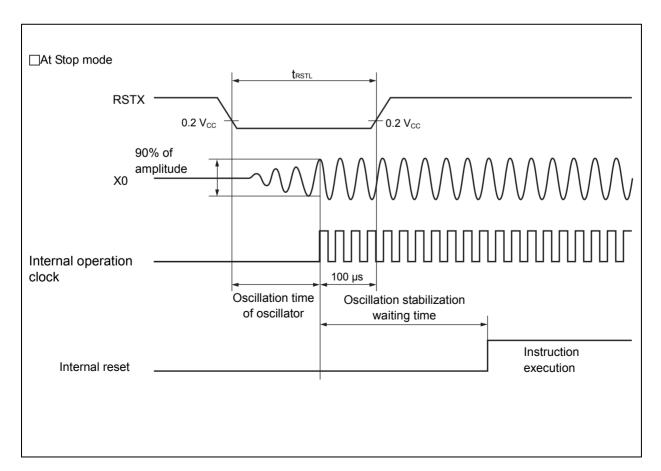
(2) Reset Input

($T_A$: -40°C to +125°C, $V_{CC}$= $AV_{CC}$=5.0V ± 10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | RSTX | – | 10 | – | µs | When normal operation |
| | | | | Oscillation time of oscillator* +100 | – | µs | At Stop mode At Power-on[2] |
| | | | | 100 | – | µs | At Watch mode |
| Width for reset input removal | | | | 1 | – | µs | |

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.

(4) Multi-function Serial

(4-1) CSIO timing

(4-1-1) Bit setting: SMR: MD2=0, SMR: MD1=1, SMR : MD0=0, SMR: SCINV=0, SCR:SPI=0

($T_A$: -40°C to +125°C, $V_{CC}$= $AV_{CC}$=5.0V ± 10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK11 | - | $4t_{CPP}$ | - | ns | Internal shift clock mode output pin : $C_L$=50pF |
| SCK ↓ → SOT delay time | $t_{SLOVI}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | -30 | 30 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | -300 | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHI}$ | SCK0 to SCK2, SCK5 to SCK11 SIN0 to SIN2, SIN5 to SIN11 | | 34 | - | ns | |
| | | SCK3 , SCK4 SIN3 , SIN4 | | 300 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXI}$ | SCK0 to SCK11 SIN0 to SIN11 | | 0 | - | ns | |
| Serial clock "H"pulse width | $t_{SHSL}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| Serial clock "L" pulse width | $t_{SLSH}$ | | | $2t_{CPP}$-10 | - | ns | |
| SCK ↓ → SOT delay time | $t_{SLOVE}$ | SCK0 to SCK2, SCK5 to SCK11 SOT0 to SOT2, SOT5 to SOT11 | | - | 33 | ns | |
| | | SCK3 , SCK4 SOT3 , SOT4 | | - | 300 | ns | |
| Valid SIN → SCK ↑ setup time | $t_{IVSHE}$ | SCK0 to SCK11 SIN0 to SIN11 | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | $t_{SHIXE}$ | | | 20 | - | ns | |
| SCK fall time | $t_F$ | SCK0 to SCK11 | | - | 5 | ns | |
| SCK rise time | $t_R$ | SCK0 to SCK11 | | - | 5 | ns | |

**Notes:**

AC characteristic in CLK synchronized mode.

$C_L$ is the load capacitance applied to pins during testing.

The maximum bard rate is limited by internal operation clock used and other parameters. Please use ch.3 and ch.4 with maximum baud rate 400kbps or less.

See Hardware Manual for details.

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↓→SCK↑ setup time | $t_{CSSE}$ | SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $3t_{CPP}+30$ | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↓→SCS↑ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $3t_{CPP}+30$ | - | ns | |
| SCS↓→SOT delay time | $t_{DSE}$ | SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 , SOT2, SOT5 to SOT11 | | - | 40 | ns | |
| | | SCS3, SCS40 to SCS43 SOT3 , SOT4 | | - | 300 | ns | |
| SCS↑→SOT delay time | $t_{DEE}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↑→SCS↓ clock switch time | $t_{SCC}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $3t_{CPP}-10$ | $3t_{CPP}+50$ | ns | Internal shift clock mode Round operation output pin: $C_L$=50pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $3t_{CPP}-300$ | $3t_{CPP}+50$ | ns | |

*1: $t_{CSSU}$ =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: $t_{CSHD}$=SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: $t_{CSDS}$=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again

Please see the hardware manual for details of above-mentioned *1,*2, and *3

When Serial chip select is used , Serial clock output mark level "H",
Serial chip select Inactive level "L"
Internal shift clock mode , Example of switching clock by round operation (x,y=0,1,2,3)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| SCS↑→SCK↑ setup time | $t_{CSSE}$ | SCK1 to SCK11 SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $3t_{CPP}+30$ | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↓→SCS↓ hold time | $t_{CSHE}$ | | | +0 | - | ns | |
| SCS deselect time | $t_{CSDE}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | | $3t_{CPP}+30$ | - | ns | |
| SCS↑→SOT delay time | $t_{DSE}$ | SCS1 , SCS2, SCS50~SCS53, SCS60~SCS63, SCS70~SCS73, SCS8~SCS11 SOT1 , SOT2, SOT5~SOT11 | | - | 40 | ns | |
| | | SCS3 , SCS40~SCS43 SOT3 ,SOT4 | | - | 300 | ns | |
| SCS↓→SOT delay time | $t_{DEE}$ | SCS1 to SCS3, SCS40 to SCS43, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 SOT1 to SOT11 | - | +0 | - | ns | External shift clock mode output pin: $C_L$=50pF |
| SCK↑→SCS↑ clock switch time | $t_{SCC}$ | SCK1 , SCK2, SCK5 to SCK11 SCS1 , SCS2, SCS50 to SCS53, SCS60 to SCS63, SCS70 to SCS73, SCS8 to SCS11 | - | $3t_{CPP}-10$ | $3t_{CPP}+50$ | ns | Internal shift clock mode Round operation output pin: $C_L$=50pF |
| | | SCK3 , SCK4 SCS3 , SCS40 to SCS43 | | $3t_{CPP}-300$ | $3t_{CPP}+50$ | | |

*1: $t_{CSSU}$ =SCSTR:CSSU7-0×Serial chip select timing operating clock

*2: $t_{CSHD}$=SCSTR:CSHD7-0×Serial chip select timing operating clock

*3: $t_{CSDS}$=SCSTR:CSDS15-0×Serial chip select timing operating clock

Regardless of the deselect time setting, once after the serial chip select pin becomes inactive, it will take at least five peripheral bus clock cycles to be active again
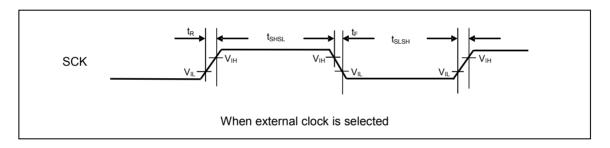
Please see the hardware manual for details of above-mentioned *1,*2, and *3.

(4-3) LIN Interface (v2.1)( Asynchronous Serial Interface for LIN (v2.1)) timing

Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1

($T_A$:-40°C to +125°C, $V_{CC}$=$AV_{CC}$=5.0V±10%/$V_{CC}$=$AV_{CC}$=3.3V±0.3V, $V_{SS}$=$AV_{SS}$=0.0V)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | $t_{SLSH}$ | SCK0 to SCK11 | - | $t_{CPP}$+10 | - | ns | output pin: $C_L$=50pF |
| Serial clock "H"pulse width | $t_{SHSL}$ | | | $t_{CPP}$+10 | - | ns | |
| SCK fall time | $t_F$ | | | - | 5 | ns | |
| SCK rise time | $t_R$ | | | - | 5 | ns | |



When external clock is selected

| Page | Section | Change Results |
|---|---|---|
| 19 | ■PIN Description | (see below) |

A List of "Pin Description" modified.

(Error)

| Pin no. | | | | | | Pin Name |
|---|---|---|---|---|---|---|
| 64 | 80 | 100 | 120 | 144 | 176 | |
| - | - | - | - | 2 | 2 | P015 / D29 / TRG0_0 |
| - | - | - | - | 3 | 3 | P016 / D30 / TRG1_0 |
| - | - | - | - | - | 4 | P170 / PPG36_1 |
| - | - | - | - | 4 | 5 | P017 / D31 / TRG2_0 |
| - | - | - | - | - | 6 | P171 / PPG37_1 |
| 2 | 2 | 2 | 2 | 5 | 7 | P020 / ASX / SIN3_1 / TRG3_0 / TIN0_2 / RTO5_1 |
| - | - | - | 3 | 6 | 8 | P021 / CS0X / SOT3_1 / TRG6_1 / TRG4_0 |
| - | - | - | 4 | 7 | 9 | P022 / CS1X / SCK3_1 / TRG7_1 / TRG5_0 |
| - | - | - | 5 | 8 | 10 | P023 / RDX / SCS3_1 / PPG32_0 / TIN0_0 |
| 3 | 3 | 3 | 6 | 9 | 11 | P024 / WR0X / SIN4_1 / PPG24_0 / TIN1_0 / RTO4_1 / INT15_0 |

| Page | Section | Change Results |
|------|---------|----------------|
| 125 | ■Interrupt Vector Table | The following sentence deleted from Interrupt vector 80pins.<br><br>(Error)<br>\*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error. |
| 129 | ■Interrupt Vector Table | The interrupt factor in Interrupt vector 100pin modified as follows:<br><br>(Error) |

(Error) table (page 129, first):

| Base timer 0 IRQ0 | 60 | 3C | ICR 44 | 30C$_H$ | 000F FF0C$_H$ | 44 |
|---|---|---|---|---|---|---|
| Base timer 0 IRQ1 | | | | | | |

(Correct) table:

| – | 60 | 3C | ICR 44 | 30C$_H$ | 000F FF0C$_H$ | 44 |
|---|---|---|---|---|---|---|
| – | | | | | | |

| Page | Section | Change Results |
|------|---------|----------------|
| 129 | ■Interrupt Vector Table | The interrupt factor in Interrupt vector 100pin modified as follows:<br><br>(Error) |

(Error) table (page 129, second):

| Base timer 1 IRQ0 | 61 | 3D | ICR 45 | 308$_H$ | 000F FF08$_H$ | 45 \*5 |
|---|---|---|---|---|---|---|
| Base timer 1 IRQ1 | | | | | | |
| – | | | | | | |
| – | | | | | | |

(Correct) table:

| Base timer 1 IRQ0 | 61 | 3D | ICR 45 | 308$_H$ | 000F FF08$_H$ | 45 |
|---|---|---|---|---|---|---|
| Base timer 1 IRQ1 | | | | | | |
| – | | | | | | |
| – | | | | | | |

| Page | Section | Change Results |
|------|---------|----------------|
| 129 | ■Interrupt Vector Table | The following sentence deleted from Interrupt vector 100pins.<br><br>(Error)<br>\*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error. |

| Page | Section | Change Results |
|---|---|---|
| 143 | ■Electrical Characteristics<br>1. Absolute Maximum Ratings | The following note added.<br><br>(Correct)<br>*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.<br>*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106. |
| 155 | ■Electrical Characteristics<br>AC Characteristics<br>(2) Reset Input | Added the At power-on[2] condition to the remarks in Reset input time. |
| 156 | ■Electrical Characteristics<br>AC Characteristics<br>(3) Power-on Conditions | Deleted the Slope detection undetected specification.<br>Added the Power ramp rate and C pin voltage at Power-on.<br>*1, *2: Changed the sentence.<br>Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on. |
| 6 to 11,<br>203 to<br>216 | ■Product lineup<br>■Ordering information | Package description modified to JEDEC description. |
| 47 | ■During Power-on | The following sentence modified as fdeleted from Interrupt<br>(Error)<br>To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50μs or longer (between 0.2V and 2.7V) during power-on.<br><br>(Correct)<br>To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on.<br>Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily. |
| 49, 50 | ■Block Diagram | The following Block diagram modified as follows:<br>●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B<br>●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D<br>(Error)<br>CAN (2ch).<br><br>(Correct)<br>CAN (3ch) |
| 217 to<br>220 | ■Ordering Information | Added the following description.<br>■ORDERING INFORMATION MB91F52xxxD |
| 221 to<br>227 | ■Package Dimensions | Package Dimensions modified to JEDEC description. |

| Page | Section | Change Results |
|------|---------|----------------|
| 142,143 | 11. Electrical Characteristics<br>Recommended operating conditions | The following sentence should be modified as follows:<br><br>(Error)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.<br>Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level.<br><br>(Correct)<br>*1: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.<br>The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD. |
| 146 | 11. Electrical Characteristics<br>DC Characteristics | Pin name of $R_{UP3}$ should be modified as follows:<br><br>(Error)<br>Port pin other than P035,041,093,122<br><br>(Correct)<br>Port pin other than P035,041,073,074,076,077,093,122 |
| 187 | 11. Electrical Characteristics<br>(8) Low voltage detection (External low-voltage detection) | Note of Detection voltage should be added as follows:<br><br>(Correct)<br>Detection voltage [3]<br><br>*3: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage (2.7V). Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD. |