Infineon Technologies - MB91F522FWBPMC-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

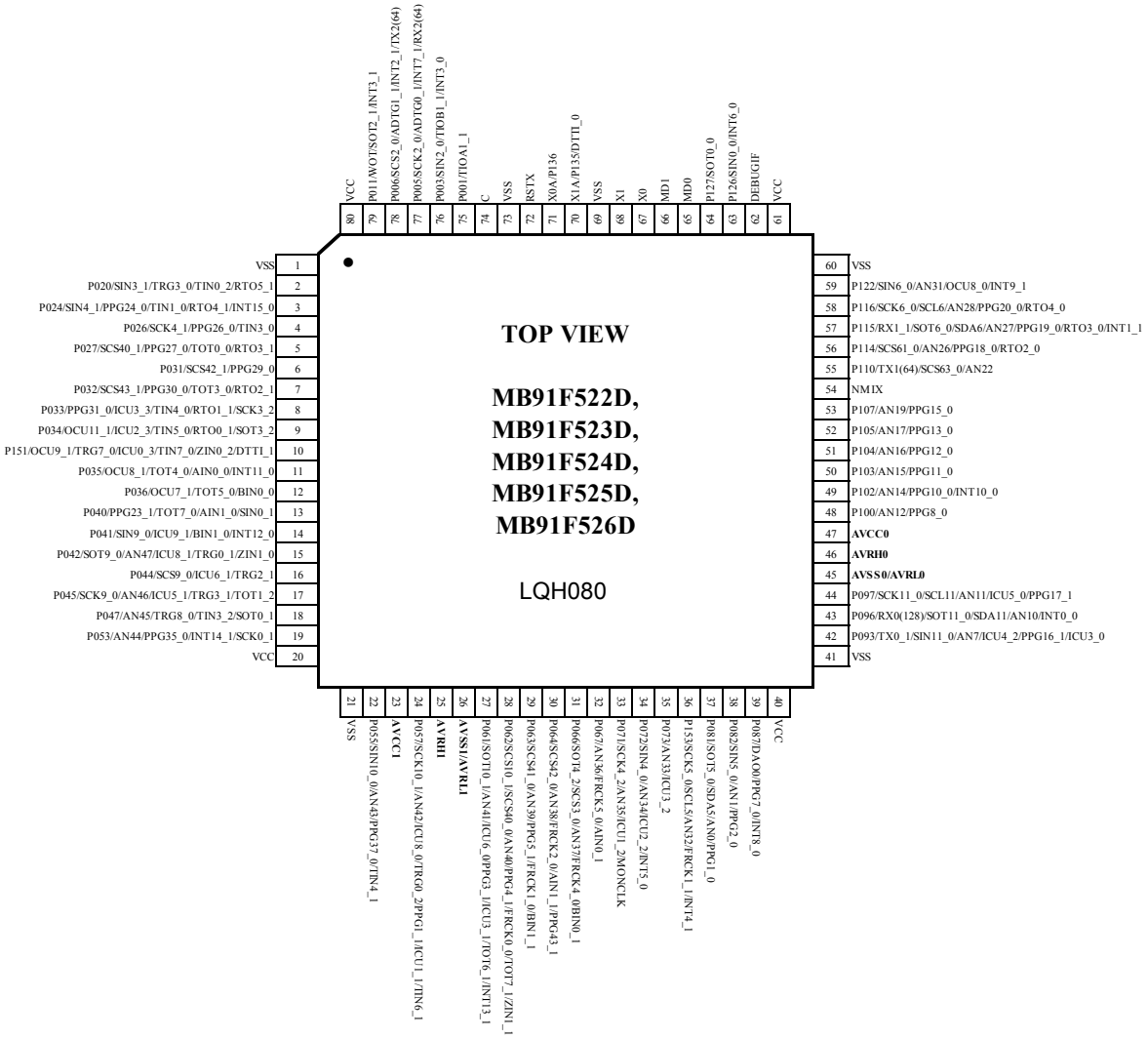
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522fwbpmc-gse1

MB91F52xD

MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D

(TOP VIEW)



* In a single clock product, pin 70 and pin 71 are the general-purpose ports.

MB91F52xK

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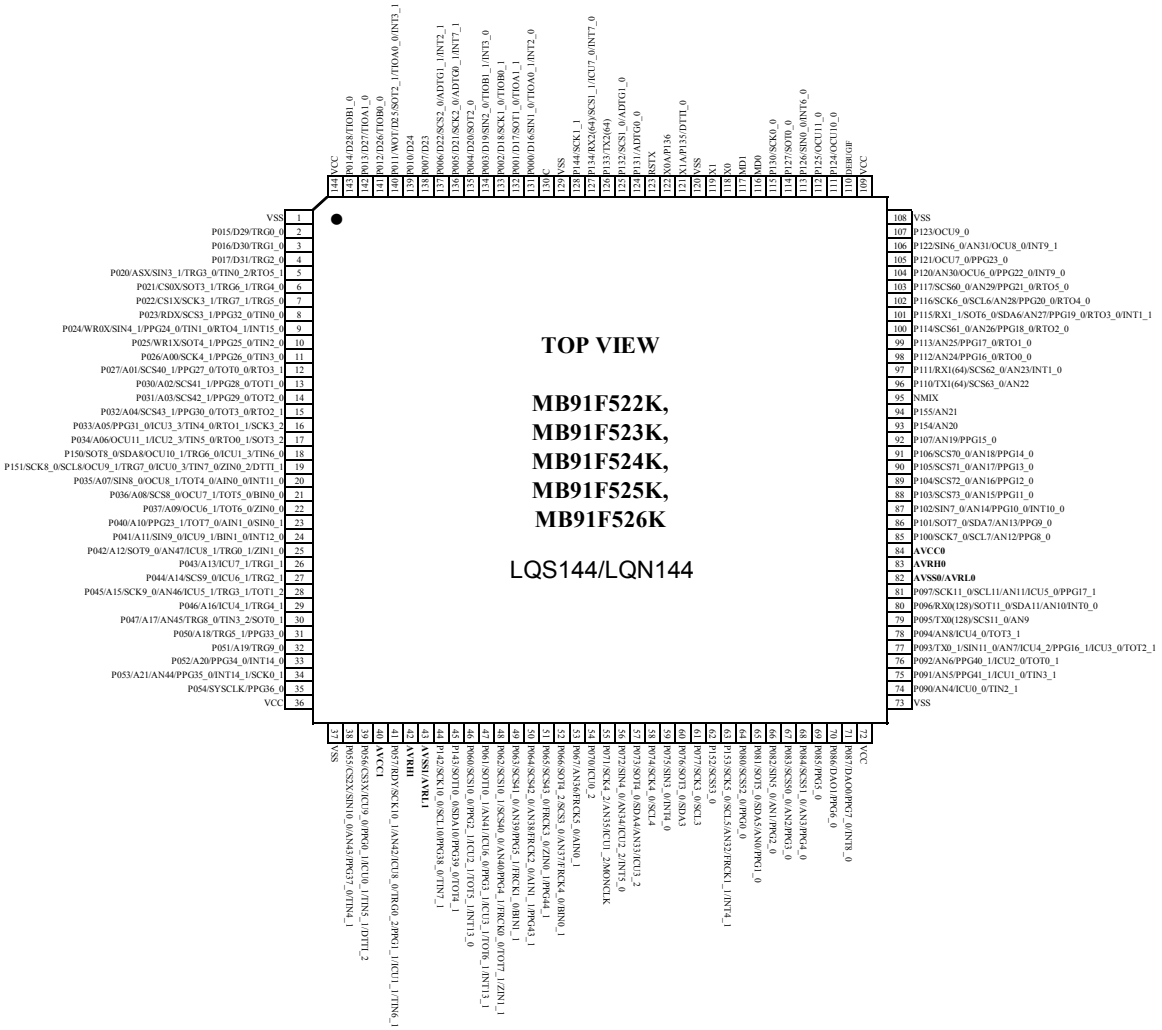
(TOP VIEW)



* In a single clock product, pin 121 and pin 122 are the general-purpose ports.

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	-	-	64	80	P080	-	A	General-purpose I/O port
						SCS52_0	-		Serial chip select 52 output (0)
						PPG0_0	-		PPG ch.0 output (0)
29	37	46	56	65	81	P081	-	G	General-purpose I/O port
						SOT5_0/ SDA5	-		Multi-function serial ch.5 serial data output (0)/I^{2}C bus serial data I/O
						AN0	-		ADC analog 0 input
						PPG1_0	-		PPG ch.1 output (0)
30	38	47	57	66	82	P082	-	G	General-purpose I/O port
						SIN5_0	-		Multi-function serial ch.5 serial data input (0)
						AN1	-		ADC analog 1 input
						PPG2_0	-		PPG ch.2 output (0)
-	-	-	-	67	83	P083	-	B	General-purpose I/O port
						SCS50_0	-		Serial chip select 50 I/O (0)
						AN2	-		ADC analog 2 input
						PPG3_0	-		PPG ch.3 output (0)
-	-	-	-	68	84	P084	-	B	General-purpose I/O port
						SCS51_0	-		Serial chip select 51 output (0)
						AN3	-		ADC analog 3 input
						PPG4_0	-		PPG ch.4 output (0)
-	-	-	-	69	85	P085	-	A	General-purpose I/O port
						PPG5_0	-		PPG ch.5 output (0)
-	-	48	58	70	86	P086	-	C	General-purpose I/O port
						DAO1	-		DAC analog 1 output
						PPG6_0	-		PPG ch.6 output (0)
31	39	49	59	71	87	P087	-	C	General-purpose I/O port
						DAO0	-		DAC analog 0 output
						PPG7_0	-		PPG ch.7 output (0)
						INT8_0	-		INT8 External interrupt input (0)
-	-	-	-	-	90	P190	-	A	General-purpose I/O port
						TIN0_1	-		Reload timer ch.0 event input (1)
-	-	-	-	-	91	P191	-	A	General-purpose I/O port
						TIN1_1	-		Reload timer ch.1 event input (1)
-	-	-	-	74	92	P090	-	B	General-purpose I/O port
						AN4	-		ADC analog 4 input
						ICU0_0	-		Input capture ch.0 input (0)
						TIN2_1	-		Reload timer ch.2 event input (1)
-	-	-	-	75	93	P091	-	B	General-purpose I/O port
						AN5	-		ADC analog 5 input
						PPG41_1	-		PPG ch.41 output (1)
						ICU1_0	-		Input capture ch.1 input (0)
						TIN3_1	-		Reload timer ch.3 event input (1)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
-	-	80	96	115	141	P130	-	F	General-purpose I/O port
						SCK0_0	-		Multi-function serial ch.0 clock I/O (0)
-	-	-	-	-	142	P162	-	A	General-purpose I/O port
						TRG5_2	-		PPG trigger 5 input (2)
-	-	-	-	-	143	P163	-	A	General-purpose I/O port
						TRG6_2	-		PPG trigger 6 input (2)
51	65	81	97	116	144	MD0	-	K	Mode pin 0
52	66	82	98	117	145	MD1	-	K	Mode pin 1
53	67	83	99	118	146	X0	-	N	Main clock oscillation input
54	68	84	100	119	147	X1	-	N	Main clock oscillation output
56	70	86	102	121	149	P135	-	A	General-purpose I/O port
						DTTI_0	-		Waveform generator ch.0-ch.5 input pin (0)
						X1A	-	O	Sub clock oscillation output
57	71	87	103	122	150	P136	-	A	General-purpose I/O port
						X0A	-	O	Sub clock oscillation input
58	72	88	104	123	151	RSTX	N	M	External reset input
-	-	-	-	124	152	P131	-	A	General-purpose I/O port
						ADTG0_0	-		A/D converter external trigger input 0 (0)
-	-	-	105	125	153	P132	-	A	General-purpose I/O port
						SCS1_0	-		Serial chip select 1 I/O (0)
						ADTG1_0	-		A/D converter external trigger input 1 (0)
-	-	89	106	126	154	P133	-	A	General-purpose I/O port
						TX2(64)	-		CAN transmission data 2 output
-	-	90	107	127	155	P134	-	F	General-purpose I/O port
						RX2(64)	-		CAN reception data 2 input
						SCS1_1	-		Serial chip select 1 I/O (1)
						ICU7_0	-		Input capture ch.7 input (0)
						INT7_0	-		INT7 External interrupt input (0)
-	-	91	108	128	156	P144	-	F	General-purpose I/O port
						SCK1_1	-		Multi-function serial ch.1 clock I/O (1)
-	-	94 *1	111 *1	131	159	P000	-	F	General-purpose I/O port
						D16 *4, *5	-		External bus data bit16 I/O (0)
						SIN1_0	-		Multi-function serial ch.1 serial data input (0)
						TIOA0_1 *4	-		TIOA output of Base timer ch.0 (1)
						INT2_0	-		INT2 External interrupt input (0)
-	75 *1	95 *1	112 *1	132	160	P001	-	A	General-purpose I/O port
						D17 *3, *4, *5	-		External bus data bit17 I/O
						SOT1_0 *3	-		Multi-function serial ch.1 serial data output (0)
						TIOA1_1	-		TIOA I/O of Base timer ch.1 (1)

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000CF0_H$	DCCR15 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000CF4_H$	DCSR15 [R/W] H 0------- -----000		DTCR15 [R/W] H 00000000 00000000		
$000CF8_H$	DSAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CFC_H$	DDAR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000D00_H$ to $000DF0_H$	—	—	—	—	Reserved [S]
$000DF4_H$	—	—	DNMIR [R/W] B 0------0	DILVR [R/W] B ---11111	DMA Controller [S]
$000DF8_H$	DMACR[R/W] W 0------- -------- 0------- --------				
$000DFC_H$	—	—	—	—	Reserved [S]
$000E00_H$	DDR00 [R/W] B,H,W 00000000	DDR01 [R/W] B,H,W 00000000	DDR02 [R/W] B,H,W 00000000	DDR03 [R/W] B,H,W 00000000	Data Direction Register
$000E04_H$	DDR04 [R/W] B,H,W 00000000	DDR05 [R/W] B,H,W 00000000	DDR06 [R/W] B,H,W 00000000	DDR07 [R/W] B,H,W 00000000	
$000E08_H$	DDR08 [R/W] B,H,W 00000000	DDR09 [R/W] B,H,W 00000000	DDR10 [R/W] B,H,W 00000000	DDR11 [R/W] B,H,W 00000000	Data Direction Register
$000E0C_H$	DDR12 [R/W] B,H,W 00000000	DDR13 [R/W] B,H,W -0000000	DDR14 [R/W] B,H,W ---000--	DDR15 [R/W] B,H,W --000000	
$000E10_H$	—	—	—	—	
$000E14_H$	—	—	—	—	
$000E18_H$	DDR16 [R/W] B,H,W 00000000	DDR17 [R/W] B,H,W 00000000	DDR18 [R/W] B,H,W 00000000	DDR19 [R/W] B,H,W 00000000	
$000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00 [R/W] B,H,W 00000000	PFR01 [R/W] B,H,W 00000000	PFR02 [R/W] B,H,W 00000000	PFR03 [R/W] B,H,W 00000000	Port Function Register
$000E24_H$	PFR04 [R/W] B,H,W 00000000	PFR05 [R/W] B,H,W 00000000	PFR06 [R/W] B,H,W 00000000	PFR07 [R/W] B,H,W 00000000	
$000E28_H$	PFR08 [R/W] B,H,W 00000000	PFR09 [R/W] B,H,W 00000000	PFR10 [R/W] B,H,W 00000000	PFR11 [R/W] B,H,W 00000000	
$000E2C_H$	PFR12 [R/W] B,H,W 00000000	PFR13 [R/W] B,H,W -0000000	PFR14 [R/W] B,H,W ---000--	PFR15 [R/W] B,H,W --000000	
$000E30_H$	—	—	—	—	
$000E34_H$	—	—	—	—	
$000E38_H$	PFR16 [R/W] B,H,W 00000000	PFR17 [R/W] B,H,W 00000000	PFR18 [R/W] B,H,W 00000000	PFR19 [R/W] B,H,W 00000000	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00125C$_H$	OCCPB4/OCCP4 [R/W] H,W 00000000 00000000		OCCPB5/OCCP5 [R/W] H,W 00000000 00000000		16-bit Output compare 4/5
001260$_H$	OCS45 [R/W] B,H,W -110--00 00001100		—	OCMOD45 [R/W] B,H,W ------00	
001264$_H$ to 001278$_H$	—	—	—	—	Reserved
00127C$_H$	IPCP0 [R] H,W 00000000 00000000		IPCP1 [R] H,W 00000000 00000000		16-bit Input capture 0/1
001280$_H$	ICS01 [R/W] B,H,W ------00 00000000		—	LSYNS [R/W] B,H,W ----0000	
001284$_H$	IPCP2 [R] H,W 00000000 00000000		IPCP3 [R] H,W 00000000 00000000		16-bit Input capture 2/3
001288$_H$	ICS23 [R/W] B,H,W ------00 00000000		—	—	
00128C$_H$ to 001298$_H$	—	—	—	—	Reserved
00129C$_H$	—	—	—	—	Reserved
0012A0$_H$	TMRR0 [R/W] H,W 00000000 00000001		TMRR1 [R/W] H,W 00000000 00000001		Waveform generator 0/1/2
0012A4$_H$	TMRR2 [R/W] H,W 00000000 00000001		—	—	
0012A8$_H$	DTSCR0 [R/W] B,H,W 00000000	DTSCR1 [R/W] B,H,W 00000000	DTSCR2 [R/W] B,H,W 00000000	—	
0012AC$_H$	—	DTIR0 [R/W] B,H,W 000000--	—	DTMNS0 [R/W] B,H,W 00---000	
0012B0$_H$	—	SIGCR10 [R/W] B,H,W 00000000	—	SIGCR20 [R/W] B,H,W 000000-1	
0012B4$_H$	PICS0 [R/W] B,H,W 000000-- -------- -------- --------				
0012B8$_H$ to 0012CC$_H$	—	—	—	—	Reserved
0012D0$_H$	FRS5 [R/W] B,H,W --00--00 --00--00 --00--00 --00--00				16-bit Free-run timer selection A/D activation compare

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001588_H	ADRCCS32[R/W] B,H,W 00000000	ADRCCS33[R/W] B,H,W 00000000	ADRCCS34[R/W] B,H,W 00000000	ADRCCS35[R/W] B,H,W 00000000	12-bit A/D converter 2/2 unit
$00158C_H$	ADRCCS36[R/W] B,H,W 00000000	ADRCCS37[R/W] B,H,W 00000000	ADRCCS38[R/W] B,H,W 00000000	ADRCCS39[R/W] B,H,W 00000000	
001590_H	ADRCCS40[R/W] B,H,W 00000000	ADRCCS41[R/W] B,H,W 00000000	ADRCCS42[R/W] B,H,W 00000000	ADRCCS43[R/W] B,H,W 00000000	
001594_H	ADRCCS44[R/W] B,H,W 00000000	ADRCCS45[R/W] B,H,W 00000000	ADRCCS46[R/W] B,H,W 00000000	ADRCCS47[R/W] B,H,W 00000000	
001598_H to $0015A4_H$	—	—	—	—	Reserved
$0015A8_H$	ADRCOT1 [R] B,H,W -------- -------- 00000000 00000000				12-bit A/D converter 2/2 unit
$0015AC_H$	ADRCIF1 [R,W] B,H,W -------- -------- 00000000 00000000				
$0015B0_H$	ADSCANS1 [R/W] B,H,W 000-----	—	—	—	
$0015B4_H$	ADNCS16 [R/W] B,H,W 0-000-00	ADNCS17 [R/W] B,H,W 0-000-00	ADNCS18 [R/W] B,H,W 0-000-00	ADNCS19 [R/W] B,H,W 0-000-00	
$0015B8_H$	ADNCS20 [R/W] B,H,W 0-000-00	ADNCS21 [R/W] B,H,W 0-000-00	ADNCS22 [R/W] B,H,W 0-000-00	ADNCS23 [R/W] B,H,W 0-000-00	
$0015BC_H$	—	—	—	—	
$0015C0_H$	—	—	—	—	
$0015C4_H$	ADPRTF1 [R] B,H,W -------- -------- 00000000 00000000				12-bit A/D converter 2/2 unit
$0015C8_H$	ADEOCF1 [R] B,H,W -------- -------- 11111111 11111111				
$0015CC_H$	ADCS1 [R] B,H,W 0------- --------		ADCH1 [R] B,H,W ---00000	ADMD1 [R/W] B,H,W 0---0000	
$0015D0_H$	ADSTPCS8 [R/W] B,H,W 00000000	ADSTPCS9 [R/W] B,H,W 00000000	ADSTPCS10 [R/W] B,H,W 00000000	ADSTPCS11 [R/W] B,H,W 00000000	
$0015D4_H$ to $00174C_H$	—	—	—	—	Reserved

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017C8H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CCH	— /(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
0017D0H	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4H	STMCR3[R/W] B,H,W 00000000 00000000		— /(SCSCR3/SFUR3)[R/W] B,H,W -------- -------- *3 *4		
0017D8H	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W -------- *3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W -------- *3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W -------- *3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W -------- *3	
0017DCH	—	— /(SCSFR23) [R/W] B,H,W -------- *3	— /(SCSFR13) [R/W] B,H,W -------- *3	— /(SCSFR03) [R/W] B,H,W -------- *3	
0017E0H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -------- *3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -------- *3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -------- *3	TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000	
0017E4H	BGR3[R/W] H, W 00000000 00000000		— /(ISMK3)[R/W] B,H,W -------- *2	— /(ISBA3)[R/W] B,H,W -------- *2	
0017E8H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017ECH	FTICR3[R/W] B,H,W 00000000 00000000		—	—	
0017F0H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
0017F4H	— /(RDR14/(TDR14))[R/W] B,H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
0017F8H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
0017FCH	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -------- -------- *3 *4		
001800H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -------- *3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -------- *3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W -------- *3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W -------- *3	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	Multi-UART7 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$001D20_H$	PCN43 [R/W] B,H,W 00000000 000000-0		PCSR43 [W] H,W XXXXXXXX XXXXXXXX		PPG43
$001D24_H$	PDUT43 [W] H,W XXXXXXXX XXXXXXXX		PTMR43 [R] H,W 11111111 11111111		
$001D28_H$	PCN243 [R/W] B,H,W --000000 -----110		PSDR43 [R/W] H,W 00000000 00000000		
$001D2C_H$	PTPC43 [R/W] H,W 00000000 00000000		—	—	
$001D30_H$	PCN44 [R/W] B,H,W 00000000 000000-0		PCSR44 [W] H,W XXXXXXXX XXXXXXXX		PPG44
$001D34_H$	PDUT44 [W] H,W XXXXXXXX XXXXXXXX		PTMR44 [R] H,W 11111111 11111111		
$001D38_H$	PCN244 [R/W] B,H,W --000000 -----110		PSDR44 [R/W] H,W 00000000 00000000		
$001D3C_H$	PTPC44 [R/W] H,W 00000000 00000000		—	—	
$001D40_H$	PCN45 [R/W] B,H,W 00000000 000000-0		PCSR45 [W] H,W XXXXXXXX XXXXXXXX		PPG45
$001D44_H$	PDUT45 [W] H,W XXXXXXXX XXXXXXXX		PTMR45 [R] H,W 11111111 11111111		
$001D48_H$	PCN245 [R/W] B,H,W --000000 -----110		PSDR45 [R/W] H,W 00000000 00000000		
$001D4C_H$	PTPC45 [R/W] H,W 00000000 00000000		—	—	
$001D50_H$	PCN46 [R/W] B,H,W 00000000 000000-0		PCSR46 [W] H,W XXXXXXXX XXXXXXXX		PPG46
$001D54_H$	PDUT46 [W] H,W XXXXXXXX XXXXXXXX		PTMR46 [R] H,W 11111111 11111111		
$001D58_H$	PCN246 [R/W] B,H,W --000000 -----110		PSDR46 [R/W] H,W 00000000 00000000		
$001D5C_H$	PTPC46 [R/W] H,W 00000000 00000000		—	—	
$001D60_H$	PCN47 [R/W] B,H,W 00000000 000000-0		PCSR47 [W] H,W XXXXXXXX XXXXXXXX		PPG47
$001D64_H$	PDUT47 [W] H,W XXXXXXXX XXXXXXXX		PTMR47 [R] H,W 11111111 11111111		
$001D68_H$	PCN247 [R/W] B,H,W --000000 -----110		PSDR47 [R/W] H,W 00000000 00000000		
$001D6C_H$	PTPC47 [R/W] H,W 00000000 00000000		—	—	

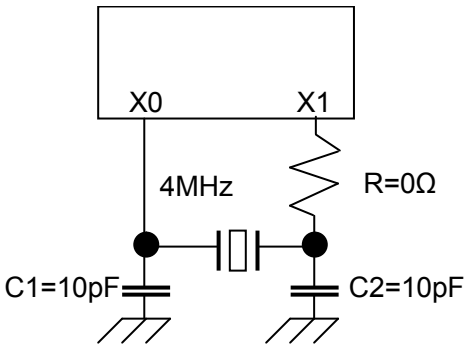
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				
002100$_H$	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104$_H$	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108$_H$	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210C$_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110$_H$	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114$_H$	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118$_H$	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C$_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120$_H$	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124$_H$	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128$_H$	—	—	—	—	
00212C$_H$	—	—	—	—	
002130$_H$, 002134$_H$	Reserved (IF1 data mirror)				CAN1 (64msb)
002138$_H$	—	—	—	—	
00213C$_H$	—	—	—	—	
002140$_H$	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144$_H$	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148$_H$	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (status)						
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (status)						
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (status)						
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
RAM diagnosis end						
RAM initialization completion						
Error generation during RAM diagnosis						
Backup RAM diagnosis end						
Backup RAM initialization completion						
Error generation during Backup RAM diagnosis						
CAN2	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Up/down counter 0						
Up/down counter 1						
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22*1
Multi-function serial interface ch.7 (status)						
16-bit Free-run timer 0 (0 detection) / (compare clear)	39	27	ICR23	360_H	$000FFF60_H$	23
Multi-function serial interface ch.7 (transmission completed)						
PPG 0/1/10/11/20/21/30/31	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
16-bit Free-run timer 1 (0 detection) / (compare clear)						
PPG 2/3/12/13/22/23/32/33/43	41	29	ICR25	358_H	$000FFF58_H$	25*3
16-bit Free-run timer 2 (0 detection) / (compare clear)						
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

Oscillation clock frequency vs. Internal operation clock frequency

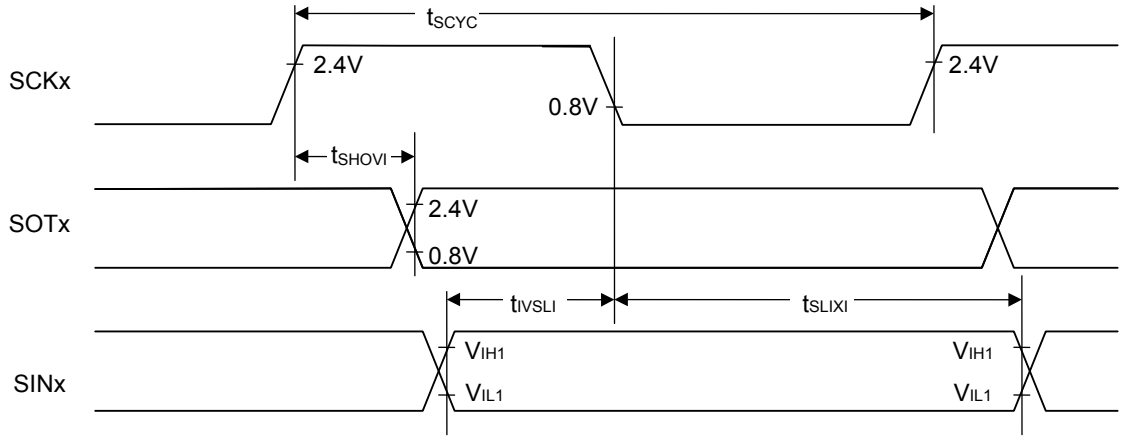
		Internal operation clock frequency							
			PLL clock						
		Main Clock	Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 19	Multiplied by 20
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	76MHz	80MHz

・Example of oscillation circuit

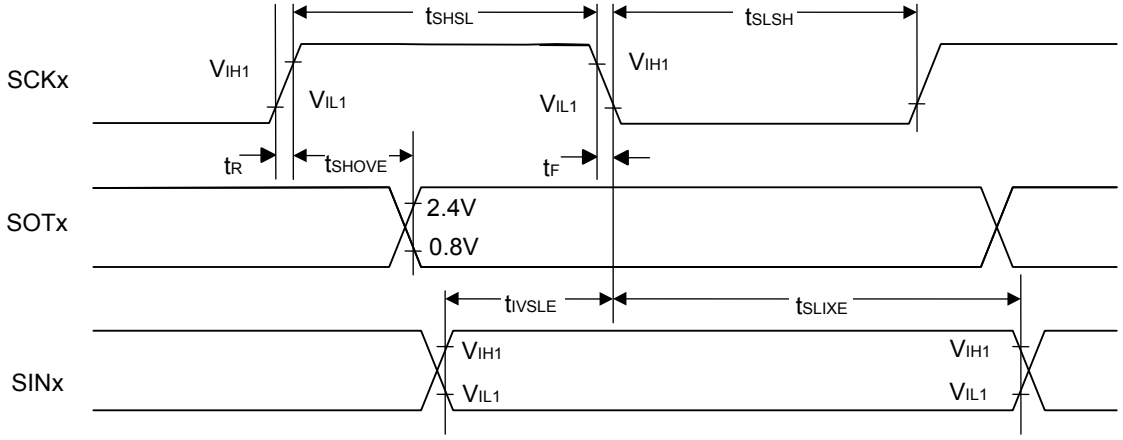


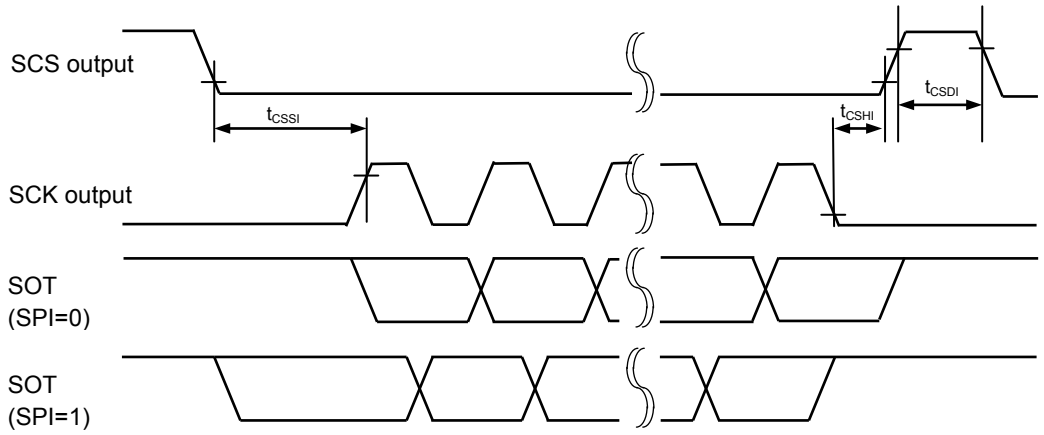
Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your print circuit board so that the oscillator can start oscillation within 20ms. Moreover, it is recommended to be designed after the match evaluation of the circuit is requested to the departure pendulum maker when the oscillation circuit is composed.

☐Internal shift clock mode

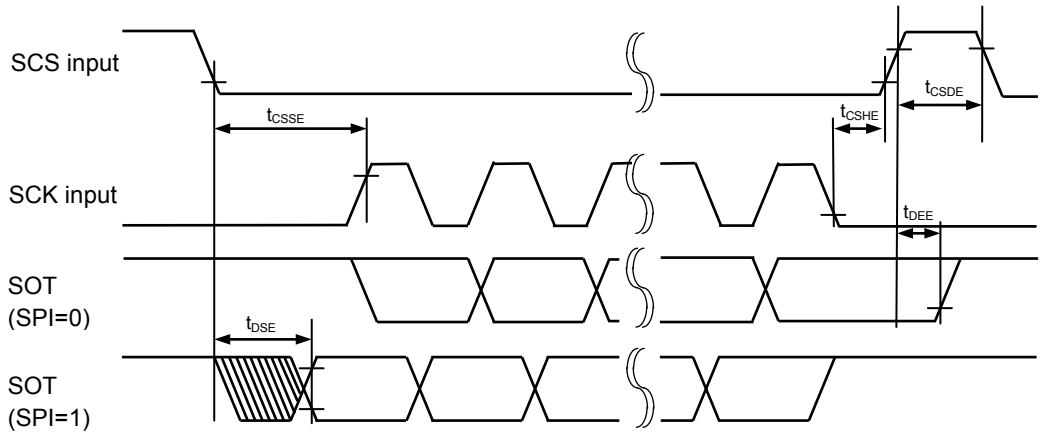


・External shift clock mode

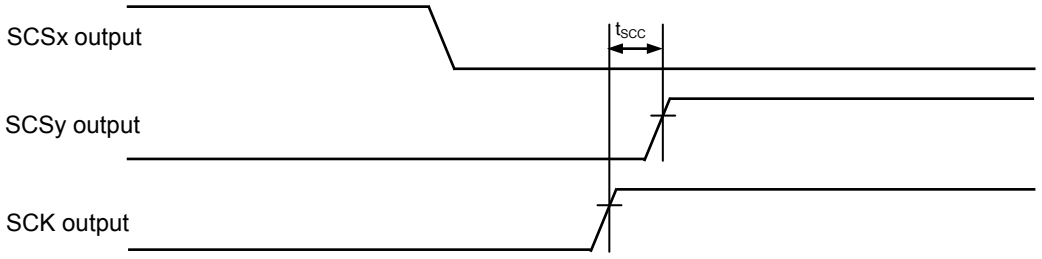




When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
Internal shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "H"
External shift clock mode



When Serial chip select is used , Serial clock output mark level "L",
Serial chip select Inactive level "L"
Master mode, Example of switching clock by round operation (x,y=0,1,2,3)

Page	Section	Change Results
Cypress Document Number: 002-04662		
Rev *B		
1	■Features	Corrected the following description. · Clock generation (equipped with SSCG function) · Main oscillation (4MHz to 16MHz) · Sub oscillation (32kHz to 100kHz) or none sub oscillation · PLL multiplication rate : 1 to 20 times ↓ · Clock generation (equipped with SSCG function) · Main oscillation (4MHz to 16MHz) · Sub oscillation (32kHz) or no sub oscillation · PLL multiplication rate : 1 to 20 times · Equipped with a 100kHz CR oscillator
2	■Features	Corrected the following description. · Base timer : Max. 2 channels ·16-bit timer · Any of four PWM/PPG/PWC/reload timer functions can be selected and used · A 32-bit timer can be used in 2 channels of cascade mode ↓ · Base timer : Max. 2 channels · 16-bit timer · Any of four PWM/PPG/PWC/reload timer functions can be selected and used · As for the PWC function and the reload timer function, a pair of 16-bit timers can be used as one 32-bit timer in the cascaded mode
6	■Product Lineup	Corrected the following description for Product lineup comparison(64 pin). Multi-Function Serial Interface: 8ch ↓ Multi-Function Serial Interface: 8ch*1
6	■Product Lineup	Added the following sentences under Product lineup comparison(64 pin) *1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).
7	■Product Lineup	Corrected the following description for Product lineup comparison(80 pin). Multi-Function Serial Interface: 9ch ↓ Multi-Function Serial Interface: 9ch*1
7	■Product Lineup	Added the following sentences under Product lineup comparison(80 pin) *1: Only channel 5, channel 6 and channel 11 support the I^2C (standard mode).

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>22, 23</td><td>■PIN Description</td><td>(Continued)
(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>28</td><td>P175
TRG9_1</td></tr>
<tr><td>11 *1</td><td>13 *1</td><td>17 *1</td><td>20 *1</td><td>23</td><td>29</td><td>P040
A10 *2, *3, *4, *5
PPG23_1
TOT7_0
AIN1_0
SIN0_1</td></tr>
<tr><td>12 *1</td><td>14 *1</td><td>18 *1</td><td>21 *1</td><td>24</td><td>30</td><td>P041
A11 *2, *3, *4, *5
SIN9_0
ICU9_1
BIN1_0
INT12_0</td></tr>
<tr><td>13 *1</td><td>15 *1</td><td>19 *1</td><td>22 *1</td><td>25</td><td>31</td><td>P042
A12 *2, *3, *4, *5
SOT9_0
AN47
ICU8_1
TRG0_1
ZIN1_0</td></tr>
<tr><td>-</td><td>-</td><td>20 *1</td><td>23 *1</td><td>26</td><td>32</td><td>P043
A13 *4, *5
ICU7_1
TRG1_1</td></tr>
<tr><td>-</td><td>16 *1</td><td>21 *1</td><td>24 *1</td><td>27</td><td>33</td><td>P044
A14 *3, *4, *5
SCS9_0
ICU6_1
TRG2_1</td></tr>
<tr><td>14 *1</td><td>17 *1</td><td>22 *1</td><td>25 *1</td><td>28</td><td>34</td><td>P045
A15 *2, *3, *4, *5
SCK9_0
AN46
ICU5_1
TRG3_1
TOT1_2</td></tr>
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A16 *5
ICU4_1
TRG4_1</td></tr>
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TRG10_0</td></tr>
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A List of "Pin Description" modified.

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<tr><td>SCK7_0/ SCL7</td></tr>
<tr><td>AN12</td></tr>
<tr><td>PPG8_0</td></tr>
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<tr><td rowspan="5">40</td><td rowspan="5">49</td><td rowspan="5">61</td><td rowspan="5">71</td><td rowspan="5">87</td><td rowspan="5">106</td><td>P102</td></tr>
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<tr><td>PPG11_0</td></tr>
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<tr><td>SCS72_0</td></tr>
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<tr><td>PPG12_0</td></tr>
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<tr><td>AN17</td></tr>
<tr><td>PPG13_0</td></tr>
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<tr><td>SCK7_0/ SCL7*3</td></tr>
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