Infineon Technologies - MB91F522FWCPMC-GTE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 37x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522fwcpmc-gte1

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
23	28	34	40	48	59	P062	-	B	General-purpose I/O port
						SCS10_1	-		Serial chip select 10 I/O (1)
						SCS40_0	-		Serial chip select 40 I/O (0)
						AN40	-		ADC analog 40 input
						PPG4_1	-		PPG ch.4 output (1)
						FRCK0_0	-		Free-run timer 0 clock input (0)
						TOT7_1	-		Reload timer ch.7 output (1)
						ZIN1_1	-		U/D counter ch.1 ZIN input (1)
-	29	35	41	49	60	P063	-	B	General-purpose I/O port
						SCS41_0	-		Serial chip select 41 output (0)
						AN39	-		ADC analog 39 input
						PPG5_1	-		PPG ch.5 output (1)
						FRCK1_0	-		Free-run timer 1 clock input (0)
						BIN1_1	-		U/D counter ch.1 BIN input (1)
-	-	-	-	-	61	P183	-	A	General-purpose I/O port
						PPG43_0	-		PPG ch.43 output (0)
24	30	36	42	50	62	P064	-	B	General-purpose I/O port
						SCS42_0	-		Serial chip select 42 output (0)
						AN38	-		ADC analog 38 input
						FRCK2_0	-		Free-run timer 2 clock input (0)
						AIN1_1	-		U/D counter ch.1 AIN input (1)
						PPG43_1	-		PPG ch.43 output (1)
-	-	37	43	51	63	P065	-	A	General-purpose I/O port
						SCS43_0	-		Serial chip select 43 output (0)
						FRCK3_0	-		Free-run timer 3 clock input (0)
						ZIN0_1	-		U/D counter ch.0 ZIN input (1)
						PPG44_1	-		PPG ch.44 output (1)
-	-	-	-	-	64	P184	-	A	General-purpose I/O port
						PPG44_0	-		PPG ch.44 output (0)
-	-	-	-	-	65	P185	-	A	General-purpose I/O port
						PPG45_0	-		PPG ch.45 output (0)
25	31	38	44	52	66	P066	-	B	General-purpose I/O port
						SOT4_2	-		Multi-function serial ch.4 serial data output (2)
						SCS3_0	-		Serial chip select 3 I/O (0)
						AN37	-		ADC analog 37 input
						FRCK4_0	-		Free-run timer 4 clock input (0)
						BIN0_1	-		U/D counter ch.0 BIN input (1)
-	32	39	45	53	67	P067	-	B	General-purpose I/O port
						AN36	-		ADC analog 36 input
						FRCK5_0	-		Free-run timer 5 clock input (0)
						AIN0_1	-		U/D counter ch.0 AIN input (1)

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2. Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■ Surface Mount Type

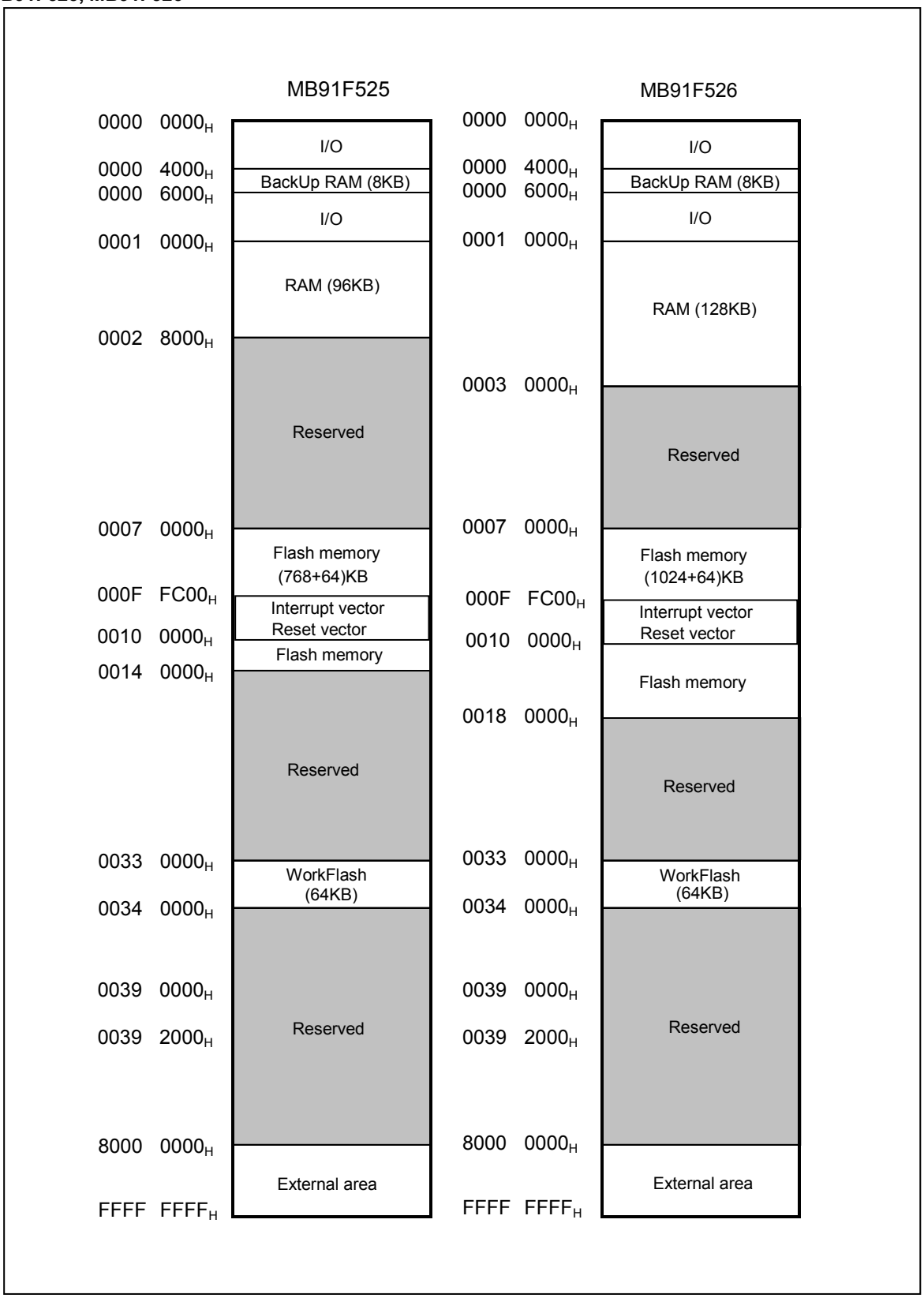
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

MB91F525, MB91F526



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$0008A0_H$	WRAR04 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild Register [S]
$0008A4_H$	WRDR04 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A8_H$	WRAR05 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008AC_H$	WRDR05 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B0_H$	WRAR06 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008B4_H$	WRDR06 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008B8_H$	WRAR07 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008BC_H$	WRDR07 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C0_H$	WRAR08 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008C4_H$	WRDR08 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008C8_H$	WRAR09 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008CC_H$	WRDR09 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D0_H$	WRAR10 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008D4_H$	WRDR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008D8_H$	WRAR11 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008DC_H$	WRDR11 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E0_H$	WRAR12 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008E4_H$	WRDR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008E8_H$	WRAR13 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$0008EC_H$	WRDR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008F0_H$	WRAR14 [R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
000954_H	TPUTCN11 [R/W] B,H,W ---00000	—	—	—	Time Protection Unit [S]
000958_H	TPUTCN12 [R/W] B,H,W ---00000	—	—	—	
$00095C_H$	TPUTCN13 [R/W] B,H,W ---00000	—	—	—	
000960_H	TPUTCN14 [R/W] B,H,W ---00000	—	—	—	
000964_H	TPUTCN15 [R/W] B,H,W ---00000	—	—	—	
000968_H	TPUTCN16 [R/W] B,H,W ---00000	—	—	—	
$00096C_H$	TPUTCN17 [R/W] B,H,W ---00000	—	—	—	
000970_H	TPUTCC0 [R] B,H,W -------- 00000000 00000000 00000000				
000974_H	TPUTCC1 [R] B,H,W -------- 00000000 00000000 00000000				
000978_H	TPUTCC2 [R] B,H,W -------- 00000000 00000000 00000000				
$00097C_H$	TPUTCC3 [R] B,H,W -------- 00000000 00000000 00000000				
000980_H	TPUTCC4 [R] B,H,W -------- 00000000 00000000 00000000				
000984_H	TPUTCC5 [R] B,H,W -------- 00000000 00000000 00000000				
000988_H	TPUTCC6 [R] B,H,W -------- 00000000 00000000 00000000				
$00098C_H$	TPUTCC7 [R] B,H,W -------- 00000000 00000000 00000000				
000990_H to $0009FC_H$	—	—	—	—	
$000A00_H$ to $000BEC_H$	—	—	—	—	Reserved
$000BF0_H$	HSCFR [R/W] B,H,W -------- ------00 00000000 00000000				OCDU
$000BF4_H$	—	—	—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0017C8H	SCR3/(IBCR3) [R/W] B,H,W 0--00000	SMR3[R/W] B,H,W 000-00-0	SSR3[R/W] B,H,W 0-000011	ESCR3/(IBSR3)[R/W] B,H,W 00000000	Multi-UART3 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
0017CCH	— /(RDR13/(TDR13))[R/W] B,H,W -------- -------- *3		RDR03/(TDR03)[R/W] B,H,W -------0 00000000 *1		
0017D0H	SACSR3[R/W] B,H,W 0----000 00000000		STMR3[R] B,H,W 00000000 00000000		
0017D4H	STMCR3[R/W] B,H,W 00000000 00000000		— /(SCSCR3/SFUR3)[R/W] B,H,W -------- -------- *3 *4		
0017D8H	— /(SCSTR33)/ (LAMSR3) [R/W] B,H,W -------- *3	— /(SCSTR23)/ (LAMCR3) [R/W] B,H,W -------- *3	— /(SCSTR13)/ (SFLR13) [R/W] B,H,W -------- *3	— /(SCSTR03)/ (SFLR03) [R/W] B,H,W -------- *3	
0017DCH	—	— /(SCSFR23) [R/W] B,H,W -------- *3	— /(SCSFR13) [R/W] B,H,W -------- *3	— /(SCSFR03) [R/W] B,H,W -------- *3	
0017E0H	—/(TBYTE33)/ (LAMESR3) [R/W] B,H,W -------- *3	—/(TBYTE23)/ (LAMERT3) [R/W] B,H,W -------- *3	—/(TBYTE13)/ (LAMIER3) [R/W] B,H,W -------- *3	TBYTE03/(LAMRID3) / (LAMTID3) [R/W] B,H,W 00000000	
0017E4H	BGR3[R/W] H, W 00000000 00000000		— /(ISMK3)[R/W] B,H,W -------- *2	— /(ISBA3)[R/W] B,H,W -------- *2	
0017E8H	FCR13[R/W] B,H,W ---00100	FCR03[R/W] B,H,W -0000000	FBYTE3[R/W] B,H,W 00000000 00000000		
0017ECH	FTICR3[R/W] B,H,W 00000000 00000000		—	—	
0017F0H	SCR4/(IBCR4) [R/W] B,H,W 0--00000	SMR4[R/W] B,H,W 000-00-0	SSR4[R/W] B,H,W 0-000011	ESCR4/(IBSR4)[R/W] B,H,W 00000000	Multi-UART4 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I2C mode is not set immediately after reset.
0017F4H	— /(RDR14/(TDR14))[R/W] B,H,W -------- -------- *3		RDR04/(TDR04)[R/W] B,H,W -------0 00000000 *1		
0017F8H	SACSR4[R/W] B,H,W 0----000 00000000		STMR4[R] B,H,W 00000000 00000000		
0017FCH	STMCR4[R/W] B,H,W 00000000 00000000		— /(SCSCR4/SFUR4)[R/W] B,H,W -------- -------- *3 *4		
001800H	— /(SCSTR34)/ (LAMSR4) [R/W] B,H,W -------- *3	— /(SCSTR24)/ (LAMCR4) [R/W] B,H,W -------- *3	— /(SCSTR14)/ (SFLR14) [R/W] B,H,W -------- *3	— /(SCSTR04)/ (SFLR04) [R/W] B,H,W -------- *3	

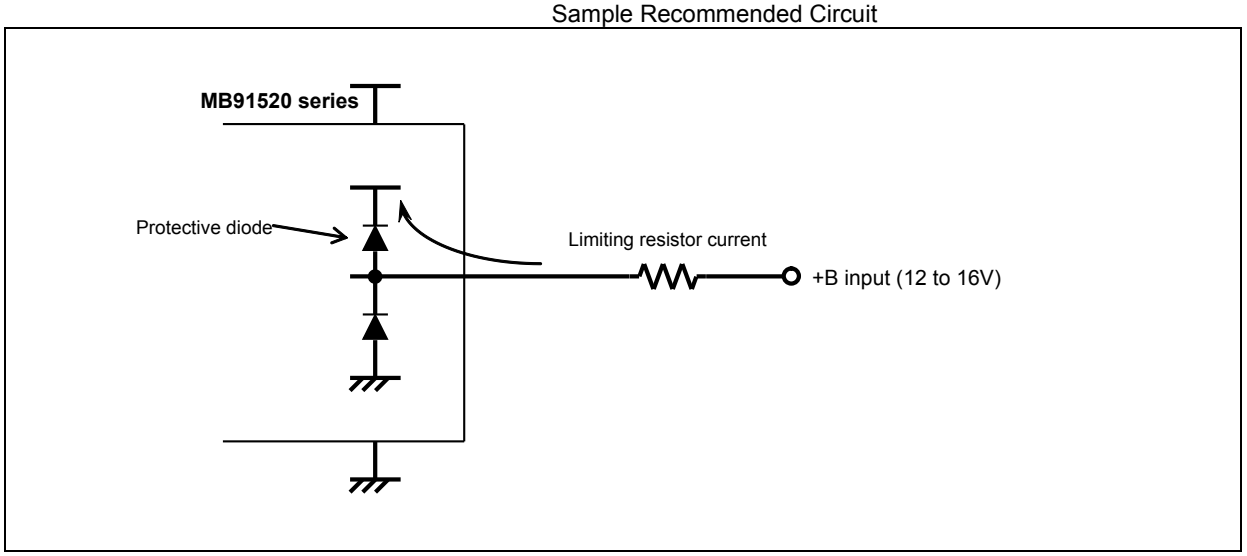
Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
0020BC$_H$	MSGVAL80 [R] B,H,W 00000000 00000000		MSGVAL70 [R] B,H,W 00000000 00000000		CAN0 (128msb)
0020C0$_H$ to 0020FC$_H$	—				
002100$_H$	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1 [R/W] B,H,W -------- 00000000		CAN1 (64msb)
002104$_H$	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1 [R/W] B,H,W -0100011 00000001		
002108$_H$	INTR1 [R] B,H,W 00000000 00000000		TESTR1 [R/W] B,H,W -------- X00000--		
00210C$_H$	BRPER1 [R/W] B,H,W -------- ----0000		—	—	
002110$_H$	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114$_H$	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118$_H$	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211C$_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	
002120$_H$	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124$_H$	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128$_H$	—	—	—	—	
00212C$_H$	—	—	—	—	
002130$_H$, 002134$_H$	Reserved (IF1 data mirror)				CAN1 (64msb)
002138$_H$	—	—	—	—	
00213C$_H$	—	—	—	—	
002140$_H$	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144$_H$	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148$_H$	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
003030_H	TEAR0A[R] B,H,W 000----- -------- -----000 00000000				RAM/ diagnosis Backup RAM
003034_H	TEAR1A[R] B,H,W 000----- -------- -----000 00000000				
003038_H	TEAR2A[R] B,H,W 000----- -------- -----000 00000000				
$00303C_H$	TAEARA[R/W] B,H,W -----111 11111111		TASARA[R/W] B,H,W -----000 00000000		
003040_H	TFECRA [R/W] B,H,W ----0000	TICRA [R/W] B,H,W ----0000	TTCRA [R/W] B,H,W ------00 00001100		RAM/ diagnosis Backup RAM
003044_H	TSRCRA [R/W] B,H,W 0-------	—	—	TKCCRA [R/W] B,H,W 00----00	
003048_H to $0030FC_H$	—				Reserved
003100_H	BUSDIGSR0[R/W] H,W 00000000 0-----00		BUSDIGSR1[R/W] H,W 00000000 0-----00		BUS diagnosis
003104_H	BUSDIGSR2[R/W] H,W 00000000 0-----00		BUSTSTR0[R/W] H,W 00--0000 00000000		
003108_H	BUSADR0 [R] W 00000000 00000000 00000000 00000000				
$00310C_H$	BUSADR1 [R] W 00000000 00000000 00000000 00000000				
003110_H	BUSADR2 [R] W 00000000 00000000 00000000 00000000				
003114_H	—	—	BUSDIGSR3[R/W] H,W 00000000 0-----00		
003118_H	BUSDIGSR4[R/W] H,W 00000000 0-----00		BUSTSTR1[R/W] H,W 00--000- 00000000		
$00311C_H$	—	—	—	—	
003120_H	BUSADR3 [R] W 00000000 00000000 00000000 00000000				
003124_H	BUSADR4 [R] W 00000000 00000000 00000000 00000000				
003128_H to $003FFC_H$	—				Reserved
004000_H to $005FFC_H$	Backup-RAM				Backup RAM area

*8: It is a standard when four-layer substrate is used.

*9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106.
*10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.

Sample Recommended Circuit



<WARNING>

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Recommended operating conditions

(V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}, AV_{CC}	4.5	5.5	V	Recommended operation guarantee range (When 5.0V is used)
		3.0	3.6	V	Recommended operation guarantee range (When 3.3V is used)
		2.7	5.5	V	Operation guarantee range *1
Smoothing capacitor *2	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	
		-40	+125	°C	*3

*1: When it is used outside recommended operation guarantee range (range of the operation guarantee),contact your sales representative.
The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the

(3) Power-on Conditions

(3-1) [MB9152xxxB/MB9152xxxC/MB9152xxxD]

(T_A: -40°C to +125°C, V_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	V_{CC}	–	2.024	2.2	2.376	V	
Level detection hysteresis width	–	V_{CC}	–	–	100	–	mV	
Level detection time	–	–	–	–	–	30	µs	*1
Power off time	t_{OFF}	V_{CC}	–	50	–	–	ms	*2
Power ramp rate	dV/dt	V_{CC}	VCC: 0.2V to 2.376V	–	–	4	mV/µs	*3
C pin voltage at Power-on	–	C	–	–	–	60	mV	*4

*1: This spec is at 4mV/µs of power ramp rate. If the power ramp rate is faster than 4mV/µs, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: Vcc must be held below 0.2V for a minimum period of t_{OFF}.

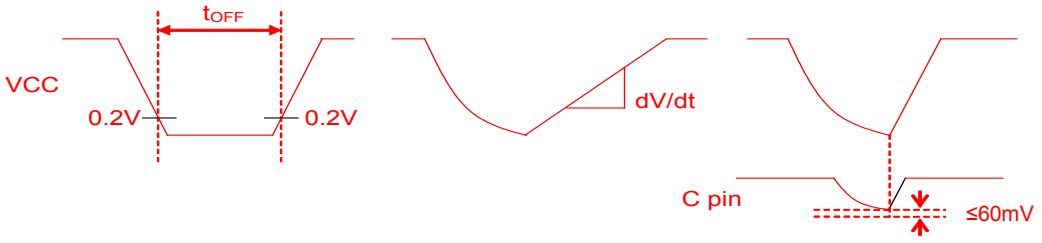
*3: Power-on can detect by satisfying power ramp rate when power off time is not satisfied.

*4: C-pin voltage is below 60 mV when VCC is turned on again.

Note:

When using MB91F52xxxB/C, either *2 or *3 or *4 must be satisfied. When neither *2 nor *3 nor *4 can be satisfied, use MB91F52xxxD and assert external reset (RSTX) at power-up and at any brownout event.

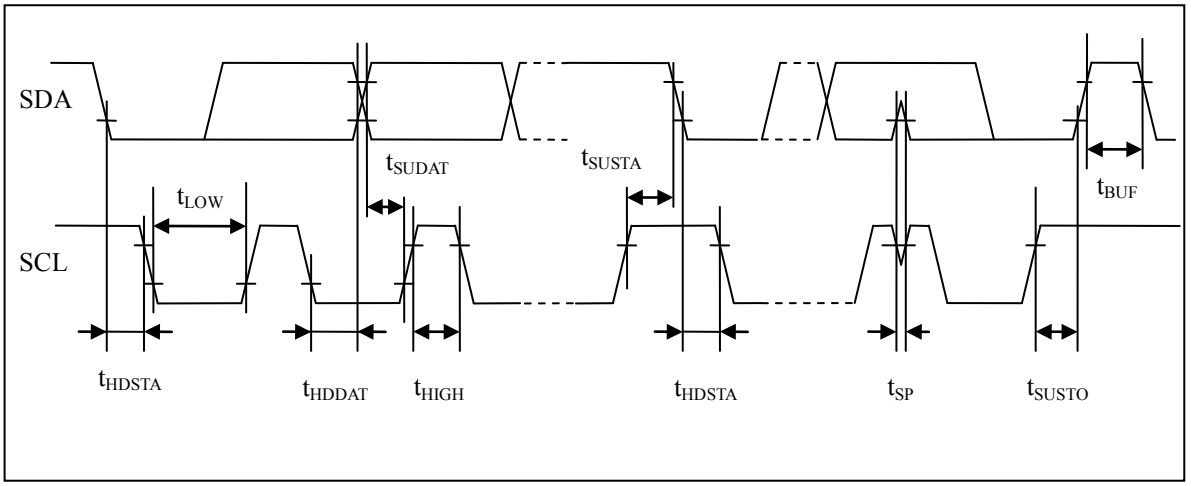
・Power off time, Power ramp rate, C pin voltage at Power-on



"t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the clock of the bus in the surrounding to 8MHz or more when use I^2C.

・ I^2C timing



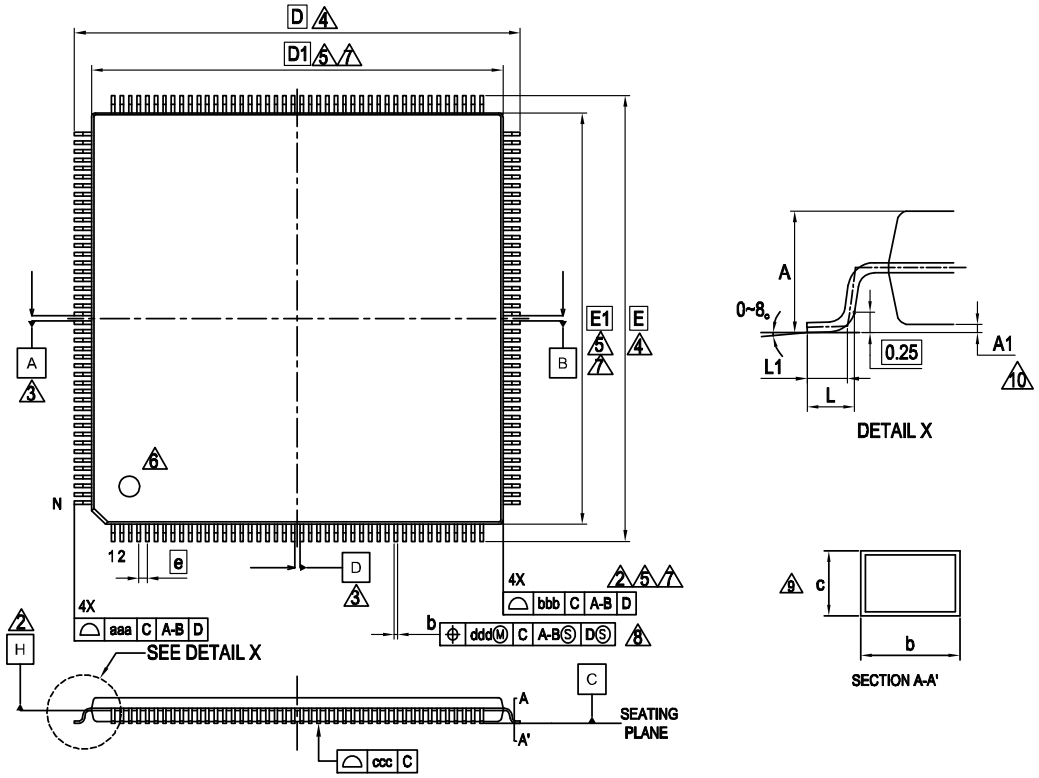
16. Ordering Information MB91F52xxxE

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWEPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJEPMC		OFF	ON	
MB91F525LWEPMC		ON	ON	
MB91F525LJEPMC		OFF	ON	
MB91F524LWEPMC		ON	ON	
MB91F524LJEPMC		OFF	ON	
MB91F523LWEPMC		ON	ON	
MB91F523LJEPMC		OFF	ON	
MB91F522LWEPMC		ON	ON	
MB91F522LJEPMC		OFF	ON	
MB91F526LSEPMC	None	ON	ON	
MB91F526LHEPMC		OFF	ON	
MB91F525LSEPMC		ON	ON	
MB91F525LHEPMC		OFF	ON	
MB91F524LSEPMC		ON	ON	
MB91F524LHEPMC		OFF	ON	
MB91F523LSEPMC		ON	ON	
MB91F523LHEPMC		OFF	ON	
MB91F522LSEPMC		ON	ON	
MB91F522LHEPMC		OFF	ON	
MB91F526KWEPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJEPMC		OFF	ON	
MB91F525KWEPMC		ON	ON	
MB91F525KJEPMC		OFF	ON	
MB91F524KWEPMC		ON	ON	
MB91F524KJEPMC		OFF	ON	
MB91F523KWEPMC		ON	ON	
MB91F523KJEPMC		OFF	ON	
MB91F522KWEPMC		ON	ON	
MB91F522KJEPMC		OFF	ON	
MB91F526KSEPMC	None	ON	ON	
MB91F526KHEPMC		OFF	ON	
MB91F525KSEPMC		ON	ON	
MB91F525KHEPMC		OFF	ON	
MB91F524KSEPMC		ON	ON	
MB91F524KHEPMC		OFF	ON	
MB91F523KSEPMC		ON	ON	
MB91F523KHEPMC		OFF	ON	
MB91F522KSEPMC		ON	ON	
MB91F522KHEPMC		OFF	ON	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526BWEPMC1	Yes	ON	ON	LQE・64 pin, Plastic
MB91F526BJEPMC1		OFF	ON	
MB91F525BWEPMC1		ON	ON	
MB91F525BJEPMC1		OFF	ON	
MB91F524BWEPMC1		ON	ON	
MB91F524BJEPMC1		OFF	ON	
MB91F523BWEPMC1		ON	ON	
MB91F523BJEPMC1		OFF	ON	
MB91F522BWEPMC1		ON	ON	
MB91F522BJEPMC1		OFF	ON	
MB91F526BSEPMC1	None	ON	ON	
MB91F526BHEPMC1		OFF	ON	
MB91F525BSEPMC1		ON	ON	
MB91F525BHEPMC1		OFF	ON	
MB91F524BSEPMC1		ON	ON	
MB91F524BHEPMC1		OFF	ON	
MB91F523BSEPMC1		ON	ON	
MB91F523BHEPMC1		OFF	ON	
MB91F522BSEPMC1		ON	ON	
MB91F522BHEPMC1		OFF	ON	

*: For details of the package, see "■ PACKAGE DIMENSIONS ".

LQP176 , 176 Lead Plastic Low Profile Quad Flat Package

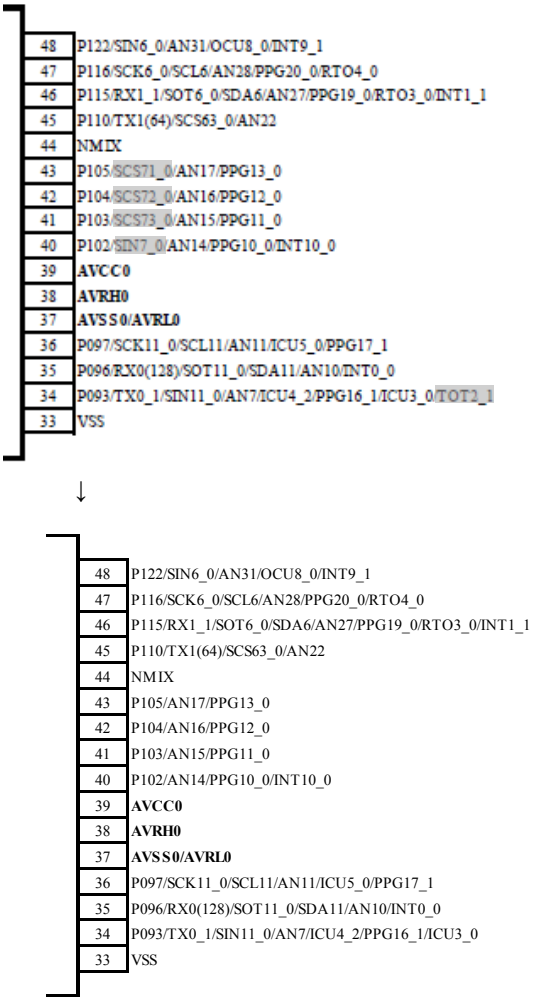


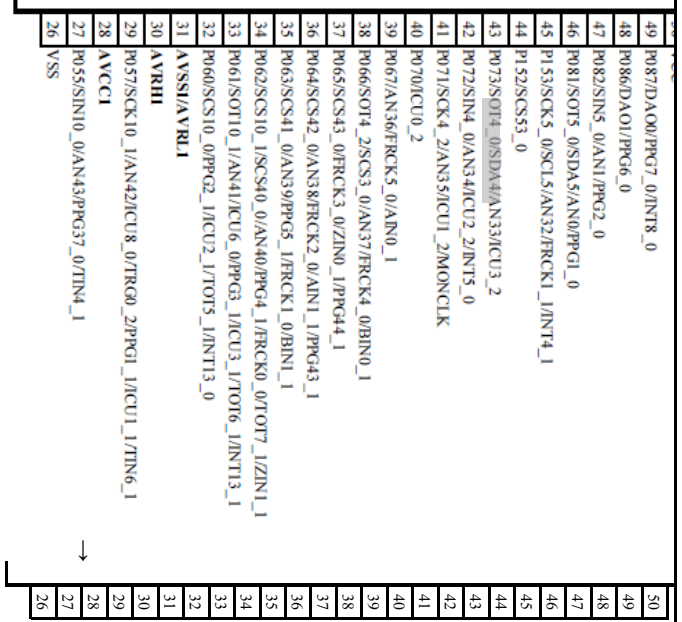
PACKAGE	LQP176		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.50 BSC		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	176		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

Page	Section	Change Results
13	■Pin Assignment MB91F52xB	- Right side  48 P122/SIN6_0/AN31/OCU8_0/INT9_1 47 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0 46 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1 45 P110/TX1(64)/SCS63_0/AN22 44 NMIX 43 P105/SCS71_0/AN17/PPG13_0 42 P104/SCS72_0/AN16/PPG12_0 41 P103/SCS73_0/AN15/PPG11_0 40 P102/SIN7_0/AN14/PPG10_0/INT10_0 39 **AVCC0** 38 **AVRH0** 37 **AVSS0/AVRL0** 36 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1 35 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0 34 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0/TOT2_1 33 VSS ↓ 48 P122/SIN6_0/AN31/OCU8_0/INT9_1 47 P116/SCK6_0/SCL6/AN28/PPG20_0/RTO4_0 46 P115/RX1_1/SOT6_0/SDA6/AN27/PPG19_0/RTO3_0/INT1_1 45 P110/TX1(64)/SCS63_0/AN22 44 NMIX 43 P105/AN17/PPG13_0 42 P104/AN16/PPG12_0 41 P103/AN15/PPG11_0 40 P102/AN14/PPG10_0/INT10_0 39 **AVCC0** 38 **AVRH0** 37 **AVSS0/AVRL0** 36 P097/SCK11_0/SCL11/AN11/ICU5_0/PPG17_1 35 P096/RX0(128)/SOT11_0/SDA11/AN10/INT0_0 34 P093/TX0_1/SIN11_0/AN7/ICU4_2/PPG16_1/ICU3_0 33 VSS

Page	Section	Change Results
15	■Pin Assignment MB91F52xF	Signals indicated by the shading below deleted in Figure. (Error) - Bottom 

Page	Section	Change Results
23, 24	■PIN Description	(Continued) (Correct)

Pin no.						Pin Name
64	80	100	120	144	176	
15 *1	18 *1	23 *1	27 *1	30	37	P047
						A17 *2, *3, *4, *5
						AN45
						TRG8_0
						TIN3_2
						SOT0_1
-	-	-	-	-	38	P177
						TRG11_0
-	-	-	28 *1	31	39	P050
						A18 *5
						TRG5_1
						PPG33_0
-	-	-	-	32	40	P051
						A19
						TRG9_0
-	-	-	-	33	41	P052
						A20
						PPG34_0
						INT14_0
16 *1	19 *1	24 *1	29 *1	34	42	P053
						A21 *2, *3, *4, *5
						AN44
						PPG35_0
						INT14_1
						SCK0_1
-	-	-	-	35	43	P054
						SYSCLK
						PPG36_0
17 *1	22 *1	27 *1	32 *1	38	46	P055
						CS2X *2, *3, *4, *5
						SIN10_0
						AN43
						PPG37_0
						TIN4_1
-	-	-	33 *1	39	49	P056
						CS3X *5
						ICU9_0
						PPG0_1
						ICU0_1
						TIN5_1
						DTTI_2

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type L in "I/O Circuit Types" modified as follows:

(Error)
- Open-drain I/O
- Output 25mA (NOD)
- TTL input

(Correct)
- Open-drain I/O
- Output 25mA (Nch open-drain)
- TTL input</td></tr>
<tr><td>40</td><td>■I/O Circuit Type</td><td>Remarks for Type M in "I/O Circuit Types" modified as follows:

(Error)
- CMOS hysteresis input
- Pull-up resistor 50kΩ (5V cont)

(Correct)
- CMOS hysteresis input
- Pull-up resistor 50kΩ</td></tr>
<tr><td>121</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 64pins.
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
<tr><td>124</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 80pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45*5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308_H</td><td rowspan="4">000F FF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
</table>

Page	Section	Change Results
143	■Electrical Characteristics 1. Absolute Maximum Ratings	The following note added. (Correct) *9: Corresponding pins: General-purpose ports other than those of P103, P104, P105 and P106. *10: Corresponding pins: General-purpose ports of P103, P104, P105 and P106.
155	■Electrical Characteristics AC Characteristics (2) Reset Input	Added the At power-on*2 condition to the remarks in Reset input time.
156	■Electrical Characteristics AC Characteristics (3) Power-on Conditions	Deleted the Slope detection undetected specification. Added the Power ramp rate and C pin voltage at Power-on. *1, *2: Changed the sentence. Added *3, *4, Note, Figure at the Power off time, Power ramp rate, C pin voltage at Power-on.
6 to 11, 203 to 216	■Product lineup ■Ordering information	Package description modified to JEDEC description.
47	■During Power-on	The following sentence modified as fdeleted from Interrupt (Error) To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on. (Correct) To prevent a malfunction of the voltage step-down circuit built in the device, the voltage rising must be monotonic increasing during power-on. Power-on prohibits that the voltage goes up and down and voltage rising stops temporarily.
49, 50	■Block Diagram	The following Block diagram modified as follows: ●MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B ●MB91F522D, MB91F523D, MB91F524D, MB91F525D, MB91F526D (Error) CAN (2ch). (Correct) CAN (3ch)
217 to 220	■Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxD
221 to 227	■Package Dimensions	Package Dimensions modified to JEDEC description.

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>184</td><td>11. Electrical Characteristics
AC Characteristics
(4-4) I2C timing</td><td>The following sentence modified as following:

(Error)
<table><tr><th colspan="2">High-speed mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table>
Notes: Only ch.3 and ch.4 are standard mode/high-speed mode correspondence.

*3: A high-speed mode I2C bus device can be used

(Correct)
<table><tr><th colspan="2">Fast mode*3</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Max</th></tr></table>
Notes: Only ch.3 and ch.4 are standard mode/fast mode correspondence.

*3: A fast mode I2C bus device can be used</td></tr>
<tr><td>187</td><td>11. Electrical Characteristics
(8) Low voltage detection (External low-voltage detection)</td><td>The following sentence modified in the Detection voltage as following:

(Error)
<table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>2.8</td><td>+8%</td><td>V</td><td>When power-supply voltage falls and detection level is set initially</td></tr></table>
(Correct)
<table><tr><th colspan="3">Value</th><th rowspan="2">Unit</th><th rowspan="2">Remarks</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>2.7</td><td>-</td><td>5.5</td><td>V</td><td></td></tr><tr><td>-8%</td><td>LVD5F_SEL [3:0]</td><td>+8%</td><td>V</td><td>LVD5F_SEL[3:0] are programmable. Refer to the hardware manual.</td></tr></table></td></tr>
<tr><td>188</td><td>11. Electrical Characteristics
(9) Low voltage detection (RAM retention low-voltage detection)</td><td>The following sentence modified as following:

(Error)
(9) Low voltage detection (Internal low-voltage detection)

(Correct)
(9) Low voltage detection (RAM retention low-voltage detection)</td></tr>
</table>