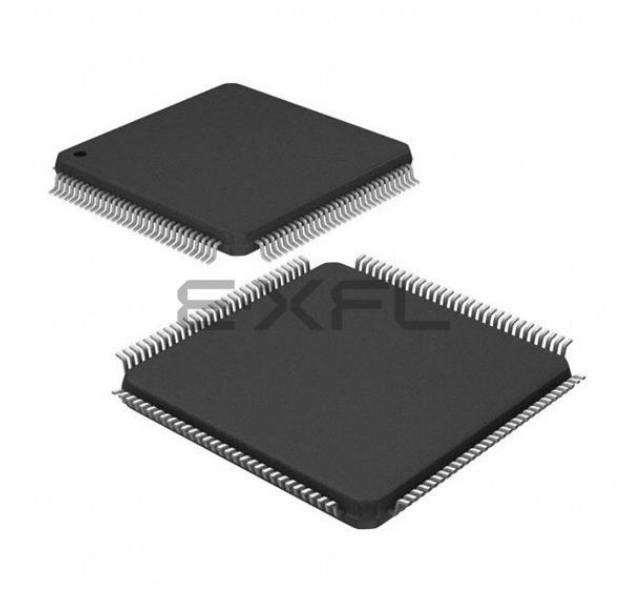

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

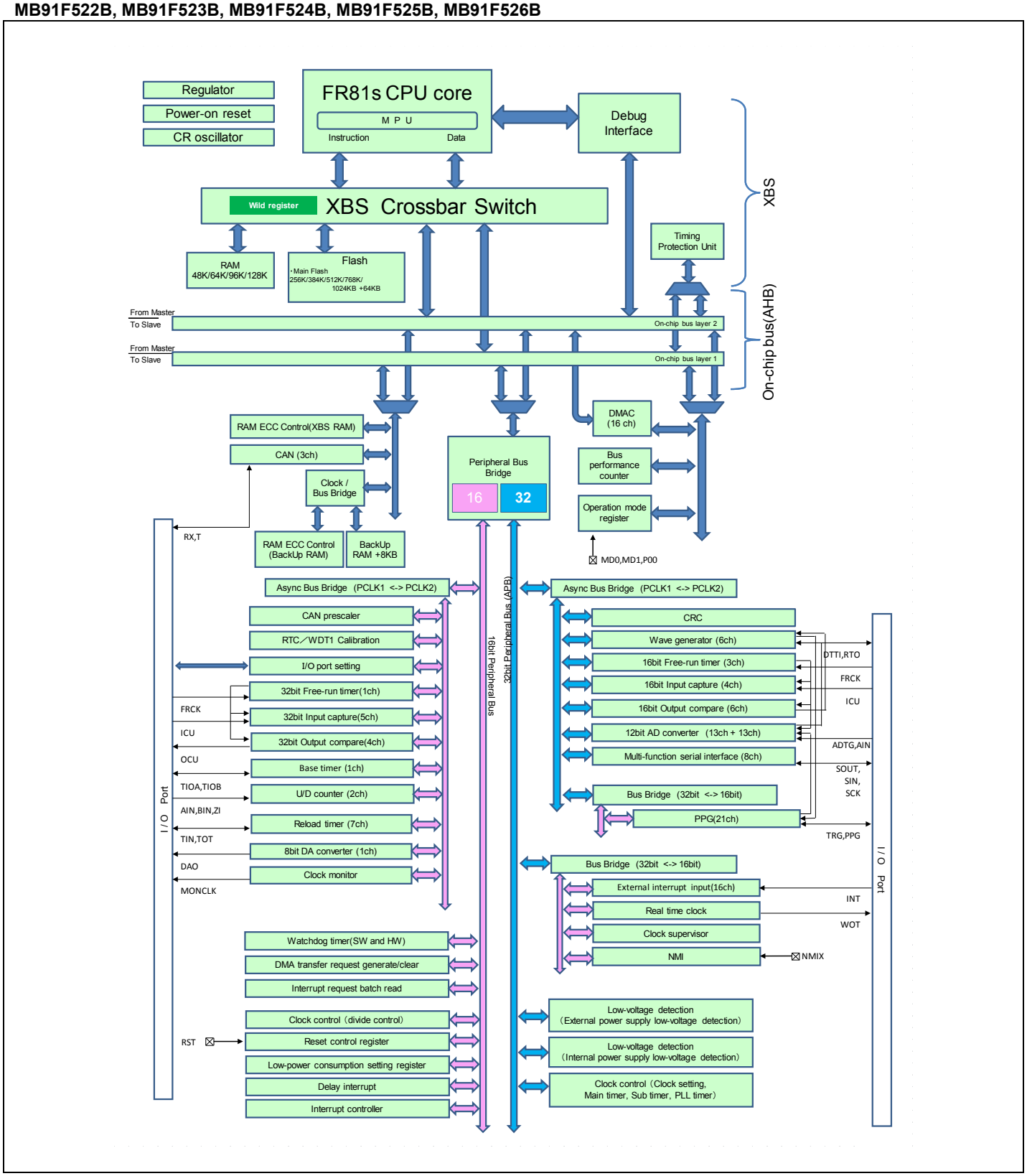
Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, I²C, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	96
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	56K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 42x12b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	120-LQFP
Supplier Device Package	120-LQFP (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f522jscpmc-gte2

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
13 *1	15 *1	19 *1	22 *1	25	31	P042	-	B	General-purpose I/O port
						A12 *2, *3, *4, *5	-		External bus/Address bit12 output
						SOT9_0	-		Multi-function serial ch.9 serial data output (0)
						AN47	-		ADC analog 47 input
						ICU8_1	-		Input capture ch.8 input (1)
						TRG0_1	-		PPG trigger 0 input (1)
						ZIN1_0	-		U/D counter ch.1 ZIN input (0)
-	-	20 *1	23 *1	26	32	P043	-	A	General-purpose I/O port
						A13 *4, *5	-		External bus/Address bit13 output (0)
						ICU7_1	-		Input capture ch.7 input (1)
						TRG1_1	-		PPG trigger 1 input (1)
-	16 *1	21 *1	24 *1	27	33	P044	-	A	General-purpose I/O port
						A14 *3, *4, *5	-		External bus/Address bit14 output (0)
						SCS9_0	-		Serial chip select 9 I/O (0)
						ICU6_1	-		Input capture ch.6 input (1)
						TRG2_1	-		PPG trigger 2 input (1)
14 *1	17 *1	22 *1	25 *1	28	34	P045	-	G	General-purpose I/O port
						A15 *2, *3, *4, *5	-		External bus/Address bit15 output (0)
						SCK9_0	-		Multi-function serial ch.9 clock I/O (0)
						AN46	-		ADC analog 46 input
						ICU5_1	-		Input capture ch.5 input (1)
						TRG3_1	-		PPG trigger 3 input (1)
						TOT1_2	-		Reload timer ch.1 output (2)
-	-	-	26 *1	29	35	P046	-	A	General-purpose I/O port
						A16 *5	-		External bus/Address bit16 output (0)
						ICU4_1	-		Input capture ch.4 input (1)
						TRG4_1	-		PPG trigger 4 input (1)
-	-	-	-	-	36	P176	-	A	General-purpose I/O port
						TRG10_0	-		PPG trigger 10 input (0)
15 *1	18 *1	23 *1	27 *1	30	37	P047	-	B	General-purpose I/O port
						A17 *2, *3, *4, *5	-		External bus/Address bit17 output (0)
						AN45	-		ADC analog 45 input
						TRG8_0	-		PPG trigger 8 input (0)
						TIN3_2	-		Reload timer ch.3 event input (2)
						SOT0_1	-		Multi-function serial ch.0 serial data output (1)
-	-	-	-	-	38	P177	-	A	General-purpose I/O port
						TRG11_0	-		PPG trigger 11 input (0)

Pin no.						Pin Name	Polarity	I/O circuit types*8	Function*9
64	80	100	120	144	176				
44	54	67	79	95	115	NMIX	N	M	Non-masking interrupt input
45	55	68	80	96	116	P110	-	B	General-purpose I/O port
						TX1(64)	-		CAN transmission data 1 output
						SCS63_0	-		Serial chip select 63 output (0)
						AN22	-		ADC analog 22 input
-	-	69	81	97	117	P111	-	G	General-purpose I/O port
						RX1(64)	-		CAN reception data 1 input
						SCS62_0	-		Serial chip select 62 output (0)
						AN23	-		ADC analog 23 input
						INT1_0	-		INT1 External interrupt input (0)
-	-	-	82	98	118	P112	-	B	General-purpose I/O port
						AN24	-		ADC analog 24 input
						PPG16_0	-		PPG ch.16 output (0)
						RTO0_0	-		Waveform generator ch. 0 output pin (0)
-	-	-	83	99	119	P113	-	B	General-purpose I/O port
						AN25	-		ADC analog 25 input
						PPG17_0	-		PPG ch.17 output (0)
						RTO1_0	-		Waveform generator ch. 1 output pin (0)
-	-	-	-	-	120	P194	-	A	General-purpose I/O port
						FRCK5_1	-		Free-run timer 5 clock input (1)
						PPG26_1	-		PPG ch.26 output (1)
-	-	-	-	-	121	P195	-	A	General-purpose I/O port
						FRCK4_1	-		Free-run timer 4 clock input (1)
						PPG27_1	-		PPG ch.27 output (1)
-	56	70	84	100	122	P114	-	B	General-purpose I/O port
						SCS61_0	-		Serial chip select 61 output (0)
						AN26	-		ADC analog 26 input
						PPG18_0	-		PPG ch.18 output (0)
						RTO2_0	-		Waveform generator ch.2 output pin (0)
46	57	71	85	101	123	P115	-	G	General-purpose I/O port
						RX1_1	-		CAN reception data 1 input (1)
						SOT6_0/ SDA6	-		Multi-function serial ch.6 serial data output (0)/I^2C bus serial data I/O
						AN27	-		ADC analog 27 input
						PPG19_0	-		PPG ch.19 output (0)
						RTO3_0	-		Waveform generator ch.3 output pin (0)
						INT1_1	-		INT1 External interrupt input (1)
47	58	72	86	102	124	P116	-	G	General-purpose I/O port
						SCK6_0/ SCL6	-		Multi-function serial ch.6 clock I/O (0)/ I^2C bus serial clock I/O
						AN28	-		ADC analog 28 input
						PPG20_0	-		PPG ch.20 output (0)
						RTO4_0	-		Waveform generator ch.4 output pin (0)

7. Block Diagram

MB91F522B, MB91F523B, MB91F524B, MB91F525B, MB91F526B



Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
$000BF8_H$	—	—	MBR [R/W] B,H,W 00------ XXXXXXXX		OCDU
$000BFC_H$	—	—	UER [W] B,H,W -------- -------X		
$000C00_H$	DCCR0 [R/W] W 0----000 --00--00 00000000 0-000000				DMA Controller [S]
$000C04_H$	DCSR0 [R/W] H 0------- -----000		DTCR0 [R/W] H 00000000 00000000		
$000C08_H$	DSAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C0C_H$	DDAR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C10_H$	DCCR1 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C14_H$	DCSR1 [R/W] H 0------- -----000		DTCR1 [R/W] H 00000000 00000000		
$000C18_H$	DSAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C1C_H$	DDAR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C20_H$	DCCR2 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C24_H$	DCSR2 [R/W] H 0------- -----000		DTCR2 [R/W] H 00000000 00000000		
$000C28_H$	DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C2C_H$	DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C30_H$	DCCR3 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C34_H$	DCSR3 [R/W] H 0------- -----000		DTCR3 [R/W] H 00000000 00000000		
$000C38_H$	DSAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C3C_H$	DDAR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C40_H$	DCCR4 [R/W] W 0----000 --00--00 00000000 0-000000				
$000C44_H$	DCSR4 [R/W] H 0------- -----000		DTCR4 [R/W] H 00000000 00000000		
$000C48_H$	DSAR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
00147C$_H$	ADCOMP34/ADCOMPB34[R/W] H,W 00000000 00000000		ADCOMP35/ADCOMPB35[R/W] H,W 00000000 00000000		12-bit A/D converter 2/2 unit
001480$_H$	ADCOMP36/ADCOMPB36[R/W] H,W 00000000 00000000		ADCOMP37/ADCOMPB37[R/W] H,W 00000000 00000000		
001484$_H$	ADCOMP38/ADCOMPB38[R/W] H,W 00000000 00000000		ADCOMP39/ADCOMPB39[R/W] H,W 00000000 00000000		
001488$_H$	ADCOMP40/ADCOMPB40[R/W] H,W 00000000 00000000		ADCOMP41/ADCOMPB41[R/W] H,W 00000000 00000000		
00148C$_H$	ADCOMP42/ADCOMPB42[R/W] H,W 00000000 00000000		ADCOMP43/ADCOMPB43[R/W] H,W 00000000 00000000		
001490$_H$	ADCOMP44/ADCOMPB44[R/W] H,W 00000000 00000000		ADCOMP45/ADCOMPB45[R/W] H,W 00000000 00000000		
001494$_H$	ADCOMP46/ADCOMPB46[R/W] H,W 00000000 00000000		ADCOMP47/ADCOMPB47[R/W] H,W 00000000 00000000		
001498$_H$ to 0014B4$_H$	—	—	—	—	Reserved
0014B8$_H$	ADTCS32[R/W] B,H,W 00000000 0010----		ADTCS33[R/W] B,H,W 00000000 0010----		12-bit A/D converter 2/2 unit
0014BC$_H$	ADTCS34[R/W] B,H,W 00000000 0010----		ADTCS35[R/W] B,H,W 00000000 0010----		
0014C0$_H$	ADTCS36[R/W] B,H,W 00000000 0010----		ADTCS37[R/W] B,H,W 00000000 0010----		
0014C4$_H$	ADTCS38[R/W] B,H,W 00000000 0010----		ADTCS39[R/W] B,H,W 00000000 0010----		
0014C8$_H$	ADTCS40[R/W] B,H,W 00000000 0010----		ADTCS41[R/W] B,H,W 00000000 0010----		
0014CC$_H$	ADTCS42[R/W] B,H,W 00000000 0010----		ADTCS43[R/W] B,H,W 00000000 0010----		
0014D0$_H$	ADTCS44[R/W] B,H,W 00000000 0010----		ADTCS45[R/W] B,H,W 00000000 0010----		
0014D4$_H$	ADTCS46[R/W] B,H,W 00000000 0010----		ADTCS47[R/W] B,H,W 00000000 0010----		
0014D8$_H$ to 0014F4$_H$	—	—	—	—	Reserved
0014F8$_H$	ADTCD32[R] B,H,W 10--0000 00000000		ADTCD33[R] B,H,W 10--0000 00000000		12-bit A/D converter 2/2 unit
0014FC$_H$	ADTCD34[R] B,H,W 10--0000 00000000		ADTCD35[R] B,H,W 10--0000 00000000		

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001804_H	—	— /(SCSFR24) [R/W] B,H,W -------- *3	— /(SCSFR14) [R/W] B,H,W -------- *3	— /(SCSFR04) [R/W] B,H,W -------- *3	Multi-UART4 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001808_H	—/(TBYTE34)/ (LAMESR4) [R/W] B,H,W -------- *3	—/(TBYTE24)/ (LAMERT4) [R/W] B,H,W -------- *3	—/(TBYTE14)/ (LAMIER4) [R/W] B,H,W -------- *3	TBYTE04/(LAMRID4) / (LAMTID4) [R/W] B,H,W 00000000	
$00180C_H$	BGR4[R/W] H, W 00000000 00000000		— /(ISMK4)[R/W] B,H,W -------- *2	— /(ISBA4)[R/W] B,H,W -------- *2	
001810_H	FCR14[R/W] B,H,W ---00100	FCR04[R/W] B,H,W -0000000	FBYTE4[R/W] B,H,W 00000000 00000000		
001814_H	FTICR4[R/W] B,H,W 00000000 00000000		—	—	
001818_H	SCR5/(IBCR5) [R/W] B,H,W 0--00000	SMR5[R/W] B,H,W 000-00-0	SSR5[R/W] B,H,W 0-000011	ESCR5/(IBSR5)[R/W] B,H,W 00000000	Multi-UART5 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00181C_H$	— /(RDR15/(TDR15))[R/W] B,H,W -------- -------- *3		RDR05/(TDR05)[R/W] B,H,W -------0 00000000 *1		
001820_H	SACSR5[R/W] B,H,W 0----000 00000000		STMR5[R] B,H,W 00000000 00000000		
001824_H	STMCR5[R/W] B,H,W 00000000 00000000		— /(SCSCR5/SFUR5)[R/W] B,H,W -------- -------- *3 *4		
001828_H	— /(SCSTR35)/ (LAMSR5) [R/W] B,H,W -------- *3	— /(SCSTR25)/ (LAMCR5) [R/W] B,H,W -------- *3	— /(SCSTR15)/ (SFLR15) [R/W] B,H,W -------- *3	— /(SCSTR05)/ (SFLR05) [R/W] B,H,W -------- *3	
$00182C_H$	—	— /(SCSFR25) [R/W] B,H,W -------- *3	— /(SCSFR15) [R/W] B,H,W -------- *3	— /(SCSFR05) [R/W] B,H,W -------- *3	
001830_H	—/(TBYTE35)/ (LAMESR5) [R/W] B,H,W -------- *3	—/(TBYTE25)/ (LAMERT5) [R/W] B,H,W -------- *3	—/(TBYTE15)/ (LAMIER5) [R/W] B,H,W -------- *3	TBYTE05/(LAMRID5) / (LAMTID5) [R/W] B,H,W 00000000	
001834_H	BGR5[R/W] H, W 00000000 00000000		— /(ISMK5)[R/W] B,H,W -------- *2	— /(ISBA5)[R/W] B,H,W -------- *2	
001838_H	FCR15[R/W] B,H,W ---00100	FCR05[R/W] B,H,W -0000000	FBYTE5[R/W] B,H,W 00000000 00000000		
$00183C_H$	FTICR5[R/W] B,H,W 00000000 00000000		—	—	

Address	Address offset value / Register name				Block
	+0	+1	+2	+3	
001878_H	— /(SCSTR37)/ (LAMSR7) [R/W] B,H,W -------- *3	— /(SCSTR27)/ (LAMCR7) [R/W] B,H,W -------- *3	— /(SCSTR17)/ (SFLR17) [R/W] B,H,W -------- *3	— /(SCSTR07)/ (SFLR07) [R/W] B,H,W -------- *3	Multi-UART7 *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
$00187C_H$	—	— /(SCSFR27) [R/W] B,H,W -------- *3	— /(SCSFR17) [R/W] B,H,W -------- *3	— /(SCSFR07) [R/W] B,H,W -------- *3	
001880_H	—/(TBYTE37)/ (LAMESR7) [R/W] B,H,W -------- *3	—/(TBYTE27)/ (LAMERT7) [R/W] B,H,W -------- *3	—/(TBYTE17)/ (LAMIER7) [R/W] B,H,W -------- *3	TBYTE07/(LAMRID7) / (LAMTID7) [R/W] B,H,W 00000000	
001884_H	BGR7[R/W] H, W 00000000 00000000		— /(ISMK7)[R/W] B,H,W -------- *2	— /(ISBA7)[R/W] B,H,W -------- *2	Multi-UART7
001888_H	FCR17[R/W] B,H,W ---00100	FCR07[R/W] B,H,W -0000000	FBYTE7[R/W] B,H,W 00000000 00000000		
$00188C_H$	FTICR7[R/W] B,H,W 00000000 00000000		—	—	
001890_H	SCR8/(IBCR8) [R/W] B,H,W 0--00000	SMR8[R/W] B,H,W 000-00-0	SSR8[R/W] B,H,W 0-000011	ESCR8/(IBSR8)[R/W] B,H,W 00000000	Multi-UART8 *1: Byte access is possible only for access to lower 8 bits. *2: Reserved because I^2C mode is not set immediately after reset. *3: Reserved because CSIO mode is not set immediately after reset. *4: Reserved because LIN2.1 mode is not set immediately after reset.
001894_H	— /(RDR18/(TDR18))[R/W] B,H,W -------- -------- *3		RDR08/(TDR08)[R/W] B,H,W -------0 00000000 *1		
001898_H	SACSR8[R/W] B,H,W 0----000 00000000		STMR8[R] B,H,W 00000000 00000000		
$00189C_H$	STMCR8[R/W] B,H,W 00000000 00000000		— /(SCSCR8/SFUR8)[R/W] B,H,W -------- -------- *3 *4		
$0018A0_H$	— /(SCSTR38)/ (LAMSR8) [R/W] B,H,W -------- *3	— /(SCSTR28)/ (LAMCR8) [R/W] B,H,W -------- *3	— /(SCSTR18)/ (SFLR18) [R/W] B,H,W -------- *3	— /(SCSTR08)/ (SFLR08) [R/W] B,H,W -------- *3	
$0018A4_H$	—	— /(SCSFR28) [R/W] B,H,W -------- *3	— /(SCSFR18) [R/W] B,H,W -------- *3	— /(SCSFR08) [R/W] B,H,W -------- *3	
$0018A8_H$	—/(TBYTE38)/ (LAMESR8) [R/W] B,H,W -------- *3	—/(TBYTE28)/ (LAMERT8) [R/W] B,H,W -------- *3	—/(TBYTE18)/ (LAMIER8) [R/W] B,H,W -------- *3	TBYTE08/(LAMRID8) / (LAMTID8) [R/W] B,H,W 00000000	
$0018AC_H$	BGR8[R/W] H,W 00000000 00000000		— /(ISMK8)[R/W] B,H,W -------- *2	— /(ISBA8)[R/W] B,H,W -------- *2	

Interrupt factor	Interrupt number		Interrupt level	Offset	Default address for TBR	RN
	Decimal	Hexadecimal				
Multi-function serial interface ch.3 (transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
Multi-function serial interface ch.4 (reception completed) / Multi-function serial interface ch.4 (status)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12*1
Multi-function serial interface ch.4 (transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
Multi-function serial interface ch.5 (reception completed) / Multi-function serial interface ch.5 (status)	30	1E	ICR14	384_H	$000FFF84_H$	14*1
Multi-function serial interface ch.5 (transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
Multi-function serial interface ch.6 (reception completed) / Multi-function serial interface ch.6 (status)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16*1
Multi-function serial interface ch.6 (transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1 / RAM diagnosis end / RAM initialization completion / Error generation during RAM diagnosis / Backup RAM diagnosis end / Backup RAM initialization completion / Error generation during Backup RAM diagnosis	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2 / Up/down counter 0 / Up/down counter 1	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-
Multi-function serial interface ch.7 (reception completed) / Multi-function serial interface ch.7 (status)	38	26	ICR22	364_H	$000FFF64_H$	22*1
16-bit Free-running timer 0 (0 detection) / (compare clear) / Multi-function serial interface ch.7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG 1/10/11/20/21/30/31 / 16-bit Free-run timer 1 (0 detection) / (compare clear)	40	28	ICR24	$35C_H$	$000FFF5C_H$	24*3
PPG 2/3/12/13/23/32/43 / 16-bit Free-run timer 2 (0 detection) / (compare clear)	41	29	ICR25	358_H	$000FFF58_H$	25*3
PPG 4/5/14/15/24/25/35/44	42	2A	ICR26	354_H	$000FFF54_H$	26*3
PPG 6/7/16/17/26/27/37	43	2B	ICR27	350_H	$000FFF50_H$	27*3
PPG 8/9/18/19/28/29	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28*3

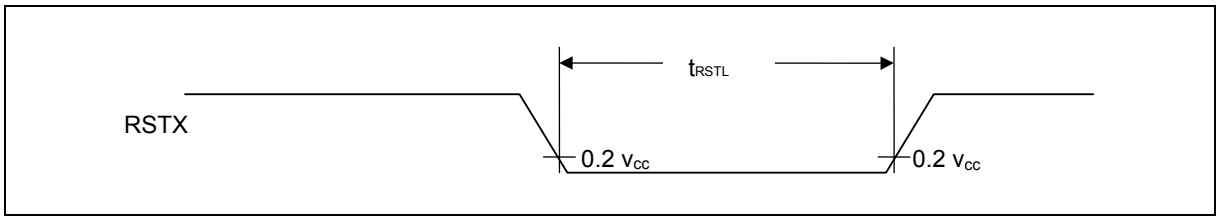
(2) Reset Input

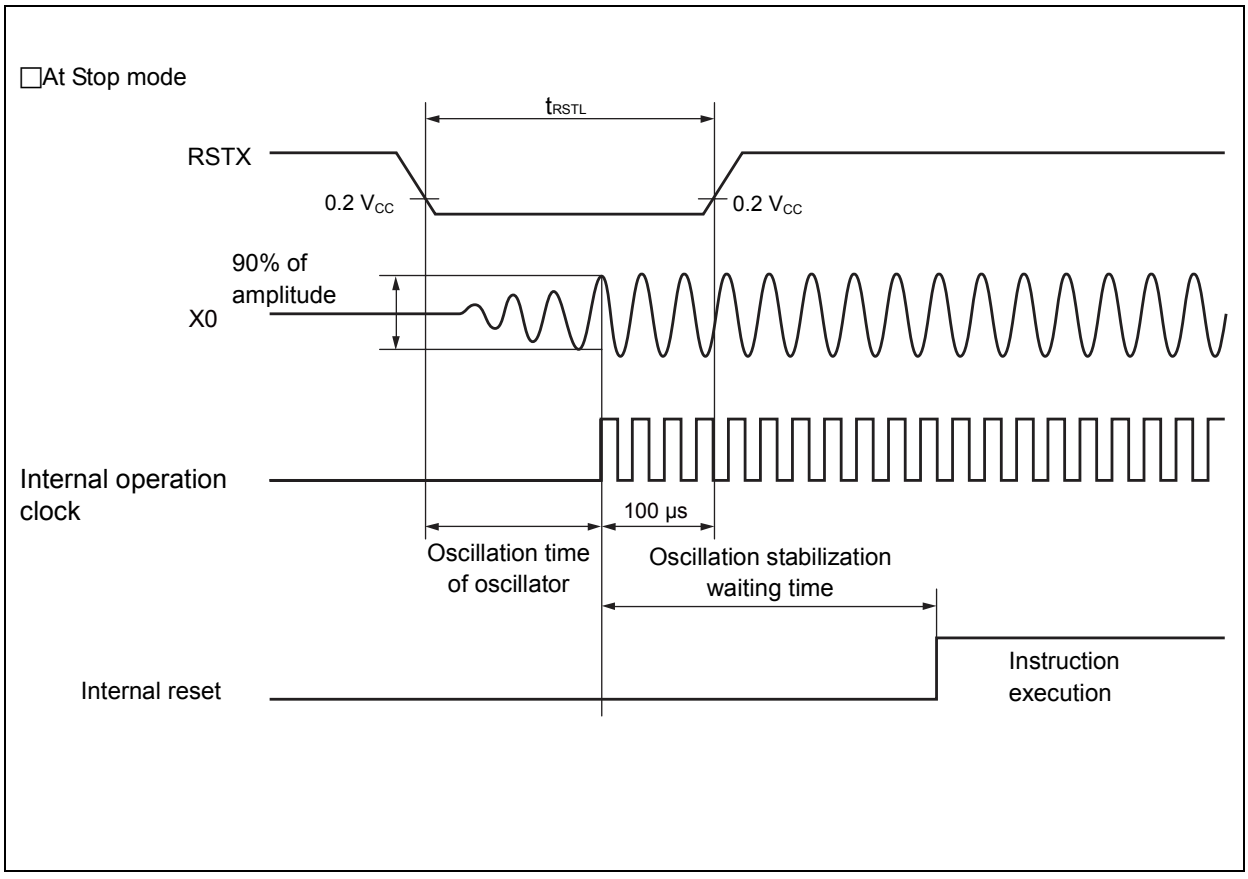
(T_A: -40°C to +125°C, V_{CC}= AV_{CC}=5.0V ± 10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* +100	–	µs	At Stop mode At Power-on*2
				100	–	µs	At Watch mode
Width for reset input removal				1	–	µs	

*1: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.

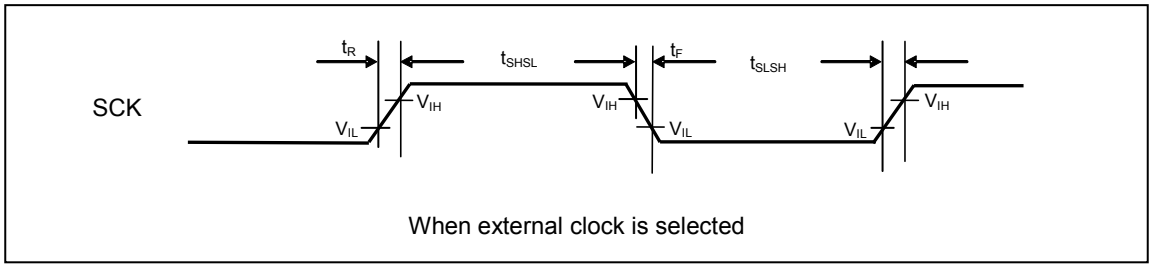
*2: In case of using MB91F52xxxD or MB91F52xxxE and corresponding to note in (3) Power-on Conditions of next subsection, assert RSTX with power-on.





(4-2) UART (Asynchronous serial interface) timing
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=0
Bit setting: SMR : MD2=0, SMR:MD1=0, SMR : MD0=1
When external clock is selected (BGR:EXT=1)
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

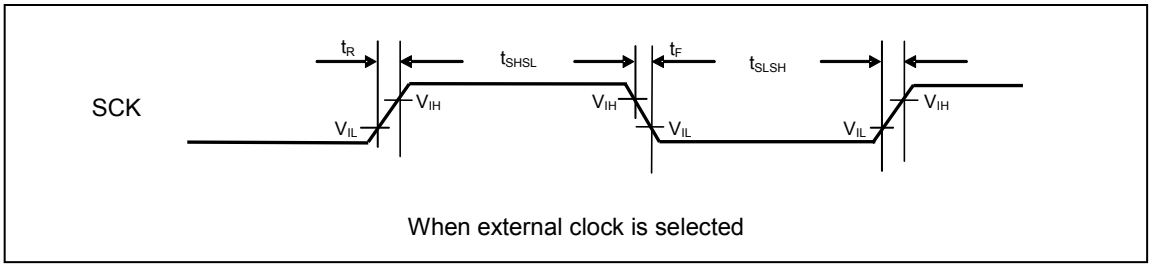
Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

(4-3) LIN Interface (v2.1)(Asynchronous Serial Interface for LIN (v2.1)) timing
Bit setting: SMR : MD2=0, SMR:MD1=1, SMR : MD0=1
(T_A:-40°C to +125°C, V_{CC}=AV_{CC}=5.0V±10%/V_{CC}=AV_{CC}=3.3V±0.3V, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock "L" pulse width	t_{SLSH}	SCK0 to SCK11	-	t_{CPP}+10	-	ns	output pin: C_L=50pF
Serial clock "H"pulse width	t_{SHSL}			t_{CPP}+10	-	ns	
SCK fall time	t_F			-	5	ns	
SCK rise time	t_R			-	5	ns	



When external clock is selected

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526KWBPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KYBPMC			OFF	
MB91F526KJBPMC		OFF	ON	
MB91F526KLBPMC			OFF	
MB91F525KWBPMC		ON	ON	
MB91F525KYBPMC			OFF	
MB91F525KJBPMC		OFF	ON	
MB91F525KLBPMC			OFF	
MB91F524KWBPMC		ON	ON	
MB91F524KYBPMC			OFF	
MB91F524KJBPMC		OFF	ON	
MB91F524KLBPMC			OFF	
MB91F523KWBPMC		ON	ON	
MB91F523KYBPMC			OFF	
MB91F523KJBPMC		OFF	ON	
MB91F523KLBPMC			OFF	
MB91F522KWBPMC		ON	ON	
MB91F522KYBPMC			OFF	
MB91F522KJBPMC		OFF	ON	
MB91F522KLBPMC			OFF	
MB91F526KSBPMC	None	ON	ON	
MB91F526KUBPMC			OFF	
MB91F526KHBPMC		OFF	ON	
MB91F526KKBPMC			OFF	
MB91F525KSBPMC		ON	ON	
MB91F525KUBPMC			OFF	
MB91F525KHBPMC		OFF	ON	
MB91F525KKBPMC			OFF	
MB91F524KSBPMC		ON	ON	
MB91F524KUBPMC			OFF	
MB91F524KHBPMC		OFF	ON	
MB91F524KKBPMC			OFF	
MB91F523KSBPMC		ON	ON	
MB91F523KUBPMC			OFF	
MB91F523KHBPMC		OFF	ON	
MB91F523KKBPMC			OFF	
MB91F522KSBPMC		ON	ON	
MB91F522KUBPMC			OFF	
MB91F522KHBPMC		OFF	ON	
MB91F522KKBPMC			OFF	

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWBPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FYBPMC			OFF	
MB91F526FJBPMC		OFF	ON	
MB91F526FLBPMC			OFF	
MB91F525FWBPMC		ON	ON	
MB91F525FYBPMC			OFF	
MB91F525FJBPMC		OFF	ON	
MB91F525FLBPMC			OFF	
MB91F524FWBPMC		ON	ON	
MB91F524FYBPMC			OFF	
MB91F524FJBPMC		OFF	ON	
MB91F524FLBPMC			OFF	
MB91F523FWBPMC		ON	ON	
MB91F523FYBPMC			OFF	
MB91F523FJBPMC		OFF	ON	
MB91F523FLBPMC			OFF	
MB91F522FWBPMC		ON	ON	
MB91F522FYBPMC			OFF	
MB91F522FJBPMC		OFF	ON	
MB91F522FLBPMC			OFF	
MB91F526FSBPMC	None	ON	ON	
MB91F526FUBPMC			OFF	
MB91F526FHBPMC		OFF	ON	
MB91F526FKBPMC			OFF	
MB91F525FSBPMC		ON	ON	
MB91F525FUBPMC			OFF	
MB91F525FHBPMC		OFF	ON	
MB91F525FKBPMC			OFF	
MB91F524FSBPMC		ON	ON	
MB91F524FUBPMC			OFF	
MB91F524FHBPMC		OFF	ON	
MB91F524FKBPMC			OFF	
MB91F523FSBPMC		ON	ON	
MB91F523FUBPMC			OFF	
MB91F523FHBPMC		OFF	ON	
MB91F523FKBPMC			OFF	
MB91F522FSBPMC		ON	ON	
MB91F522FUBPMC			OFF	
MB91F522FHBPMC		OFF	ON	
MB91F522FKBPMC			OFF	

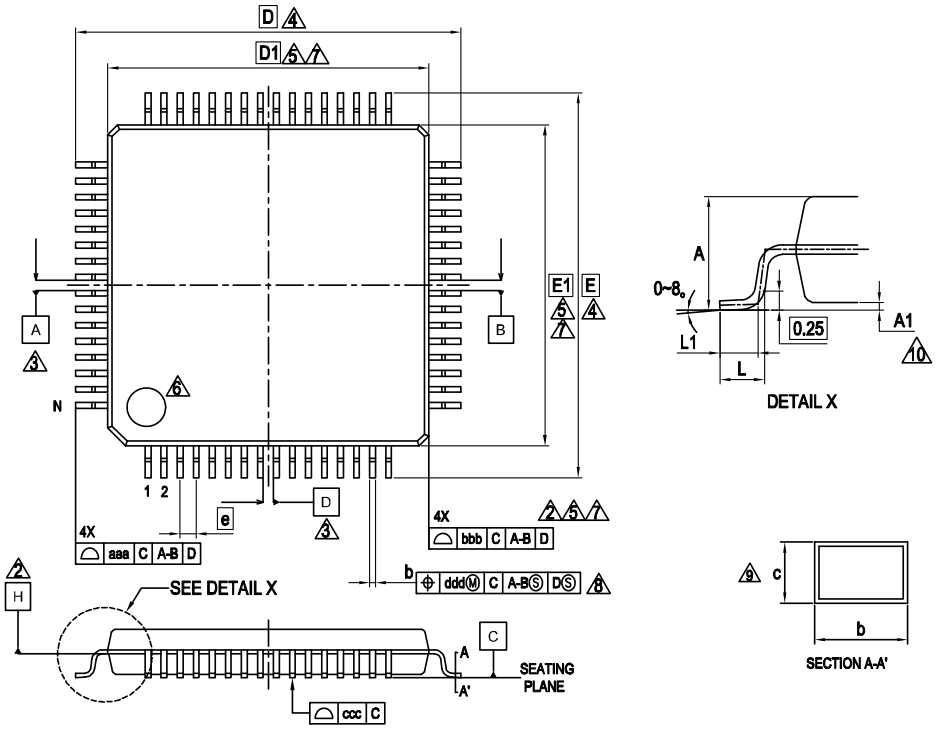
Part number	Sub clock	CSV Initial value	LVD Initial value	Package*2
MB91F526FWCPMC	Yes	ON	ON	LQI・100 pin, Plastic
MB91F526FYCPMC			OFF	
MB91F526FJCPMC		OFF	ON	
MB91F526FLCPMC			OFF	
MB91F525FWCPMC		ON	ON	
MB91F525FYCPMC			OFF	
MB91F525FJCPMC		OFF	ON	
MB91F525FLCPMC			OFF	
MB91F524FWCPMC		ON	ON	
MB91F524FYCPMC			OFF	
MB91F524FJCPMC		OFF	ON	
MB91F524FLCPMC			OFF	
MB91F523FWCPMC		ON	ON	
MB91F523FYCPMC			OFF	
MB91F523FJCPMC		OFF	ON	
MB91F523FLCPMC			OFF	
MB91F522FWCPMC		ON	ON	
MB91F522FYCPMC			OFF	
MB91F522FJCPMC		OFF	ON	
MB91F522FLCPMC			OFF	
MB91F526FSCPMC	None	ON	ON	
MB91F526FUCPMC			OFF	
MB91F526FHCPMC		OFF	ON	
MB91F526FKCPMC			OFF	
MB91F525FSCPMC		ON	ON	
MB91F525FUCPMC			OFF	
MB91F525FHCPMC		OFF	ON	
MB91F525FKCPMC			OFF	
MB91F524FSCPMC		ON	ON	
MB91F524FUCPMC			OFF	
MB91F524FHCPMC		OFF	ON	
MB91F524FKCPMC			OFF	
MB91F523FSCPMC		ON	ON	
MB91F523FUCPMC			OFF	
MB91F523FHCPMC		OFF	ON	
MB91F523FKCPMC			OFF	
MB91F522FSCPMC		ON	ON	
MB91F522FUCPMC			OFF	
MB91F522FHCPMC		OFF	ON	
MB91F522FKCPMC			OFF	

16. Ordering Information MB91F52xxxE

Part number	Sub clock	CSV Initial value	LVD Initial value	Package*
MB91F526LWEPMC	Yes	ON	ON	LQP・176 pin, Plastic
MB91F526LJEPMC		OFF	ON	
MB91F525LWEPMC		ON	ON	
MB91F525LJEPMC		OFF	ON	
MB91F524LWEPMC		ON	ON	
MB91F524LJEPMC		OFF	ON	
MB91F523LWEPMC		ON	ON	
MB91F523LJEPMC		OFF	ON	
MB91F522LWEPMC		ON	ON	
MB91F522LJEPMC		OFF	ON	
MB91F526LSEPMC	None	ON	ON	
MB91F526LHEPMC		OFF	ON	
MB91F525LSEPMC		ON	ON	
MB91F525LHEPMC		OFF	ON	
MB91F524LSEPMC		ON	ON	
MB91F524LHEPMC		OFF	ON	
MB91F523LSEPMC		ON	ON	
MB91F523LHEPMC		OFF	ON	
MB91F522LSEPMC		ON	ON	
MB91F522LHEPMC		OFF	ON	
MB91F526KWEPMC	Yes	ON	ON	LQS・144 pin, (Lead pitch 0.5mm) Plastic
MB91F526KJEPMC		OFF	ON	
MB91F525KWEPMC		ON	ON	
MB91F525KJEPMC		OFF	ON	
MB91F524KWEPMC		ON	ON	
MB91F524KJEPMC		OFF	ON	
MB91F523KWEPMC		ON	ON	
MB91F523KJEPMC		OFF	ON	
MB91F522KWEPMC		ON	ON	
MB91F522KJEPMC		OFF	ON	
MB91F526KSEPMC	None	ON	ON	
MB91F526KHEPMC		OFF	ON	
MB91F525KSEPMC		ON	ON	
MB91F525KHEPMC		OFF	ON	
MB91F524KSEPMC		ON	ON	
MB91F524KHEPMC		OFF	ON	
MB91F523KSEPMC		ON	ON	
MB91F523KHEPMC		OFF	ON	
MB91F522KSEPMC		ON	ON	
MB91F522KHEPMC		OFF	ON	

17. Package Dimensions

LQD064 , 64 Lead Plastic Low Profile Quad Flat Package



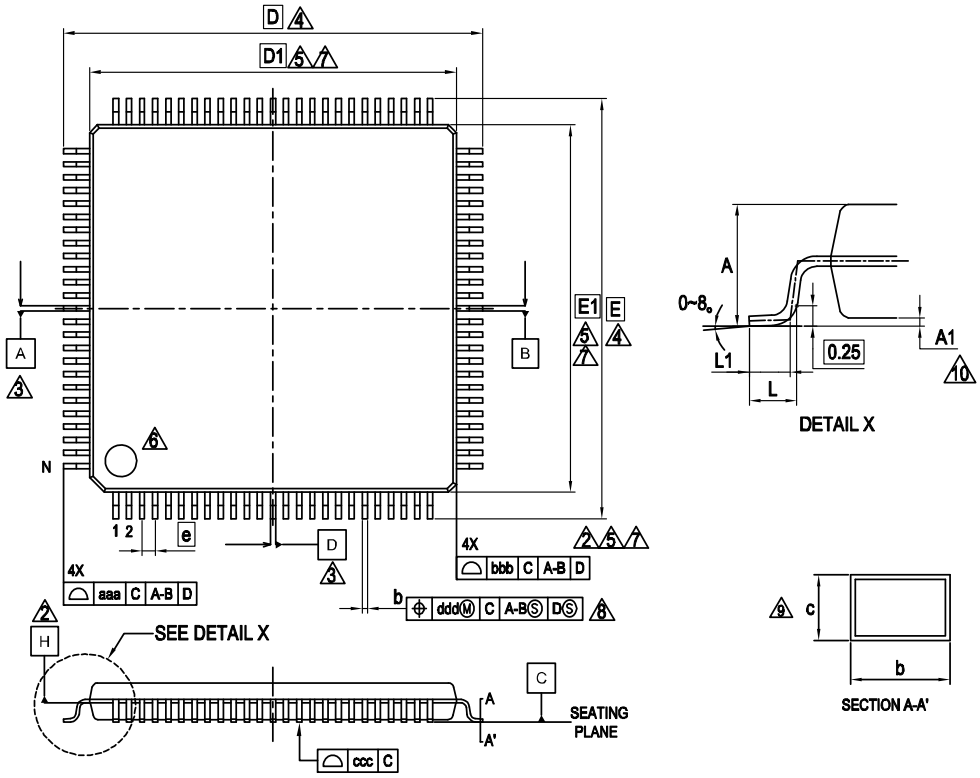
PACKAGE	LQD64		
SYMBOL	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	0.20	0.25
c	0.09	—	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	—	—	0.20
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.08
N	64		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

LQI100 , 100 Lead Plastic Low Profile Quad Flat Package



PACKAGE	LQI100		
SYMBOL	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.15	0.20	0.25
c	0.09	——	0.20
D	16.00 BSC.		
D1	14.00 BSC.		
e	0.50 BSC		
E	16.00 BSC.		
E1	14.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
aaa	——	——	0.20
bbb	——	——	0.10
ccc	——	——	0.08
ddd	——	——	0.08
N	100		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Rev. A

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>33</td><td>■PIN Description</td><td>
A List of "Pin Description" modified.

(Error)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94</td><td rowspan="5">111</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75</td><td rowspan="4">95</td><td rowspan="4">112</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17</td></tr>
<tr><td>SOT1_0</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>

(Correct)
<table>
<tr><th colspan="6">Pin no.</th><th rowspan="2">Pin Name</th></tr>
<tr><th>64</th><th>80</th><th>100</th><th>120</th><th>144</th><th>176</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td rowspan="5">-</td><td rowspan="5">-</td><td rowspan="5">94 *1</td><td rowspan="5">111 *1</td><td rowspan="5">131</td><td rowspan="5">159</td><td>P000</td></tr>
<tr><td>D16 *4, *5</td></tr>
<tr><td>SIN1_0</td></tr>
<tr><td>TIOA0_1 *4</td></tr>
<tr><td>INT2_0</td></tr>
<tr><td rowspan="4">-</td><td rowspan="4">75 *1</td><td rowspan="4">95 *1</td><td rowspan="4">112 *1</td><td rowspan="4">132</td><td rowspan="4">160</td><td>P001</td></tr>
<tr><td>D17 *3, *4, *5</td></tr>
<tr><td>SOT1_0 *3</td></tr>
<tr><td>TIOA1_1</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Page</th><th>Section</th><th>Change Results</th></tr>
<tr><td>135</td><td>■Interrupt Vector Table</td><td>"42" is deleted as shown below from the interrupt factor in Interrupt vector 144pin.

(Error)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/42/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25*3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>

(Correct)
<table>
<tr><td>PPG2/3/12/13/22/23/32/33/43</td><td rowspan="2">41</td><td rowspan="2">29</td><td rowspan="2">ICR 25</td><td rowspan="2">358 H</td><td rowspan="2">000FFF58 H</td><td rowspan="2">25*3</td></tr>
<tr><td>16-bit free-run timer 2 (0 detection) / (compare clear)</td></tr>
</table>
</td></tr>
<tr><td>137</td><td>■Interrupt Vector Table</td><td>The interrupt factor in Interrupt vector 144pin modified as follows:

(Error)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45*5</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>

(Correct)
<table>
<tr><td>Base timer 1 IRQ0</td><td rowspan="4">61</td><td rowspan="4">3D</td><td rowspan="4">ICR 45</td><td rowspan="4">308 H</td><td rowspan="4">000FFF08 H</td><td rowspan="4">45</td></tr>
<tr><td>Base timer 1 IRQ1</td></tr>
<tr><td>–</td></tr>
<tr><td>–</td></tr>
</table>
</td></tr>
<tr><td>137</td><td>■Interrupt Vector Table</td><td>The following sentence deleted from Interrupt vector 144pins.

(Error)
*5: It does not support the DMA transfer by the interrupt because of the RAM ECC bit error.</td></tr>
</table>

Page	Section	Change Results
220 to 223	16. Ordering Information	Added the following description. ■ORDERING INFORMATION MB91F52xxxE
Rev *D		
1	Features	The following sentence should be modified as follows: (Error) Conversion time : 1µs (Correct) Conversion time : 1.4µs
5,6,7,8,9,10	1. Product Lineup	The following sentence should be modified as follows: (Error) *2: Detection voltage of the external low voltage detection reset (initial) is 2.8V±8% (2.576V to 3.024V). This detection voltage (2.576V) is below the minimum operation guarantee voltage (2.7V). Between this detection voltage and the minimum operation guarantee voltage, MCU functions are not guaranteed except for the low voltage detector. Note that although the detection level is below the minimum operation guarantee voltage, the LVD reset factor flag is set as the voltage drops below the detection level. (Correct) *2: The initial detection voltage of the external low voltage detection is 2.8V±8% (2.576V to 3.024V). This LVD setting and internal LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage. Below the minimum guaranteed MCU operation voltage, MCU operations are not guaranteed with the exception of LVD.